DESIGNING A PHASE-LOCKED LOOP FOR A WEATHER SATELLITE IMAGE RECEIVER

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Abstract – **This paper presents design of a phase-locked loop (PLL) at operating frequencies from 46 MHz to 48 MHz for a weather satellite image receiver. The main objective of the designed PLL is to assist the receiver system to track a radio frequency (RF) signal transmitted from the National Oceanic and Atmospheric Administration (NOAA) satellite which has been down-converted to frequency modulation (FM) frequency 90.7 MHz. The PLL is part of a low cost ground receiving system for Automatic Picture Transmission (APT) image reception. The PLL software was designed and compiled using CCS C compiler and used Peripheral Interface Controller 16F84A (PIC16F84A) as the microcontroller while the PLL hardware was designed and then fabricated on a printed circuit board (PCB) using Protel DXP 2004. The PCB design layout for the PLL was also constructed by using Protel DXP 2004. For the practical testing of the PLL a 12V DC supply, a 9V DC supply and a spectrum analyzer are used to verify the functionality of the designed PLL. From the measurement, the PLL is recorded to operate at the desired frequencies.**

Keywords: **Phase-Locked Loop (PLL), Automatic Picture Transmission (APT), Peripheral Interface Controller (PIC), satellite weather image**

I. INTRODUCTION

One of the ways to improve severe weather forecasts and warnings is by doing the research programs focus on observation and study of the weather image processing by the weather satellites such as NOAA weather satellite. Those weather images received from the NOAA weather satellites could be use to forecast for weather and water cycle events, including storms, droughts, and floods. Weather satellite image also helped in monitoring the weather, climate, and ecosystem information to make sure individual and commercial transportation is safe, efficient, and ./environmentally sound.

In this project, the focus was placed on the PLL as part of the system for weather satellite image receiver. This PLL which is one of the component in the NOAA satellite receiver system will be assist the receiver in forecasting for the unexpected changes in weather over satellite's coverage of UiTM Shah Alam and nearby area. The Automatic Picture Transmission (APT) system is analog image transmission system developed for use on weather satellites. It was introduced in the 1960s and over four decades has provided image data to relatively low-cost user stations at locations in most countries of the world, giving many professional and other users their first introduction to real-time satellite imagery. The APT system provides a reduced resolution data stream from the Advanced Very High Resolution Radiometer (AVHRR) instrument [1].

For a brief introduction, NOAA is actually a scientific agency within the United States Department of Commerce focused on the conditions of the oceans and the atmosphere. NOAA warns of dangerous weather, charts seas and skies, guides the use and protection of ocean and coastal resources, and conducts research to improve understanding and stewardship of the environment. The NOAA support several weather satellites in Low Earth Orbit. Currently there are three NOAA APT weather satellites in operation, which are the NOAA-15, NOAA-17 and NOAA-18 [2]. All three satellites scan the Earth continuously in circular polar orbits at around 850 km altitude and transmit radio frequency (RF) in the 137 MHz to 138 MHz band which makes them relatively easy to receive with a simple antenna.

The image data is regularly transmitted to the earth via Automatic Picture Transmission (APT) as an analog broadcast. Inexpensive and unsophisticated earth satellite ground station equipment can be constructed to receive the NOAA satellite's signal in real-time while the satellite's transmitted signal is within radio range. The weather satellite receiver consists of several components and one of the components was PLL which is the main focus of this paper. The configuration of the weather satellite image receiver system is shown in Figure 1.

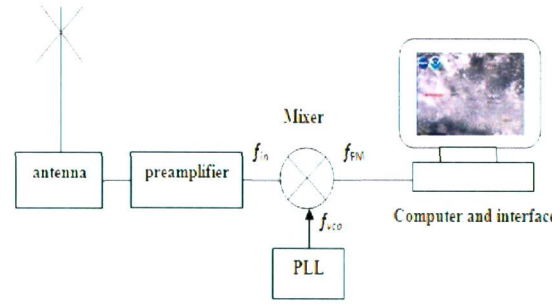


Figure 1: Weather satellite image receiver system configuration.

A PLL is an electronic circuit that controls an oscillator so that it maintains a constant phase angle thus lock on the frequency of an input or reference signal. A PLL ensures that a communication signal is locked on a specific frequency desired by the receiver system. PLL is used often in wireless communications where the oscillator is usually at the receiver and the input signal is extracted from the signal received from the remote transmitter. A basic block diagram of a PLL system is shown as in Figure 2.

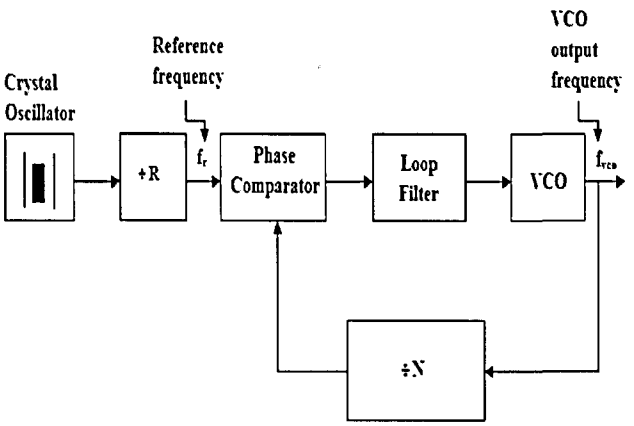


Figure 2: Basic block diagram of a PLL system

Generally a PLL comprise a voltage-controlled oscillator (VCO), a reference crystal oscillator, a frequency synthesizer chip or PLL chip, a loop filter and a phase comparator. The VCO is tuned using a special semiconductor diode called a varactor. Initially the oscillator in the VCO is at nearly the same frequency as the reference signal. Then, if the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator, so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. The phase detector will always maintain the controlled-voltage oscillator in the VCO so that the frequency output will always the same with the reference input frequency. A low-pass filter smooth out abrupt changes in the control voltage.

The problems arise in the NOAA receiver system when the signal received at the preamplifier of the ground receiver station usually not stable and may change due to noise during reception. With the implementation of a PLL system in the receiver system, it will track any instabilities in signals transmissions and effectively filter out noise. Another problem is that there are also several different channels being received at the receiver's antenna from the NOAA satellites, each one with a unique frequency. The PLL in the receiver is tuned so that the output from the mixer is a constant frequency which means that it is in "locked" condition. The signal is then easier to deal with since it is a fixed frequency from this point onwards. The PLL is located close to the preamplifier as it will assist the preamplifier by lock onto the desired frequency, based on the output of a crystal-controlled reference oscillator.

This PLL is designed to operate at the frequency range of 46 MHz to 48 MHz so the receiver will always stay in track with the receiver's operating frequency for NOAA satellites which is a down-convert FM frequency 90.7 MHz. The PLL used LMX2306 as the PLL Integrated Circuit (IC) and the microcontroller used was PIC16F84A. The software of the PLL was designed by using C programming language and PIC assembly language. The hardware of the PLL is designed and printed on a printed circuit board (PCB) using Protel DXP 2004. The practical measurement was done in the laboratory to verify the PLL functionality at the desired set of discrete frequencies.

II. METHODOLOGY

A. Process Flow

The process flow of the procedures conducted in completing this project is summarized as in Figure 3. The most important step in a PLL design is to determine the suitable frequency synthesizer chip for attaining the project desired output. Examination of a datasheet is a good starting point in a frequency synthesizer chip evaluation.

In this PLL project, low power frequency synthesizer LMX2306 has been chosen to fulfill the project's requirements. One of the reasons why it was selected because it has low power consumption therefore could optimize the power utilization in the PLL system. As for the transistor, dual-gate BF998 MOSFET has been chosen for the VCO application because it features low-noise, high gain and easy to match while maintaining a good noise behavior.

The Protel DXP 2004 is used to draw the schematic circuit of the PLL. Figure 4 shows the drawn schematic of the PLL circuit. An LC circuit is a variety of resonant circuit or tuned circuit which consists of an inductor (L) and a capacitor (C). An electric current can alternate between them at the circuit's resonant frequency. The LC network at the input stage of the VCO is purposely to ensure the VCO oscillates at a resonance frequency which is a set of desired discrete frequencies in a range of 46 MHz to 48 MHz.

The resonant circuit at the input of the PLL requires the use of capacitors and air coil inductors to build the tuned circuits. Air coil inductors used in the PLL is actually just a coil of copper wire. Where else capacitors are used to block direct current (DC) and oppose alternating current (AC). In the other hand, inductors are used to allow direct current to

flow but oppose alternating current. Inductors are passive devices used in electronic circuits to store energy in the form of a magnetic field [3]. The air coil inductors are constructed by using Wheeler's Formula as in equation (1).

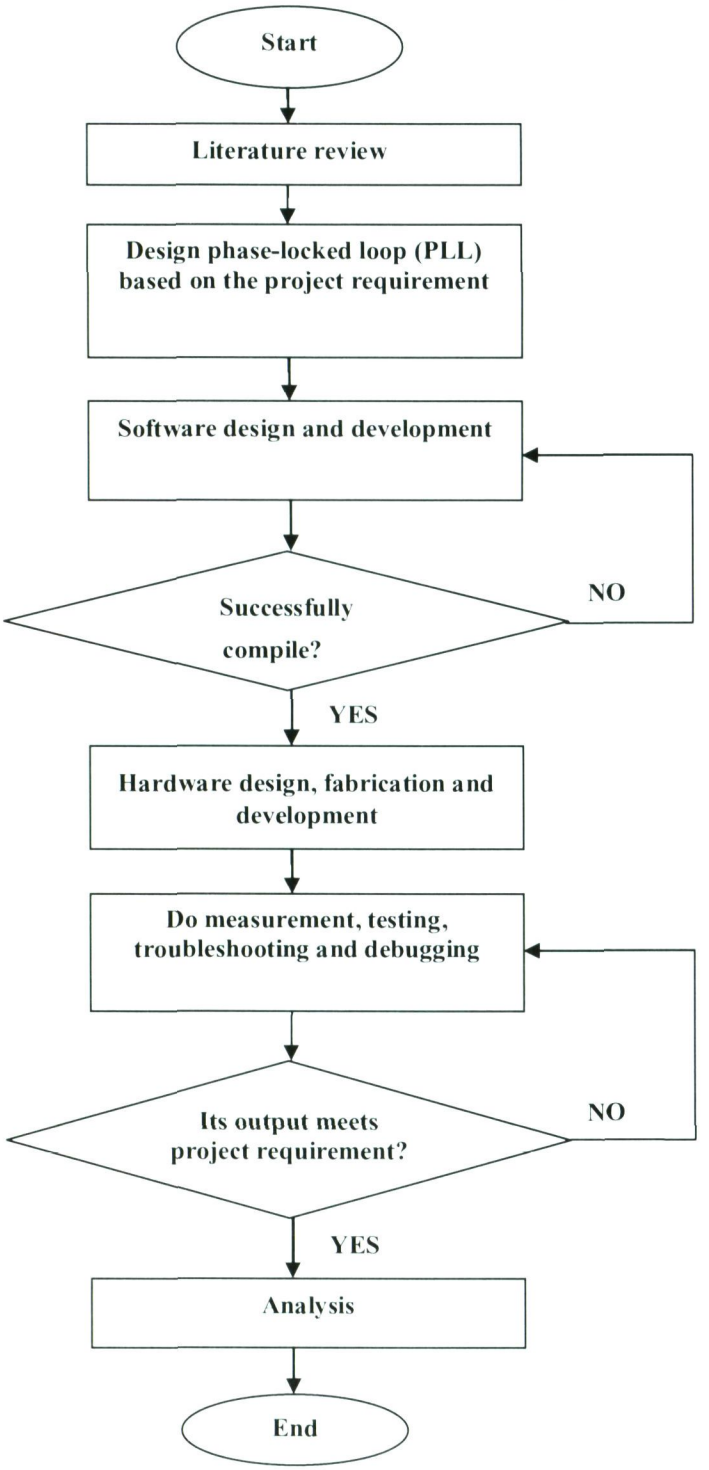


Figure 3: Flowchart of the procedures conducted

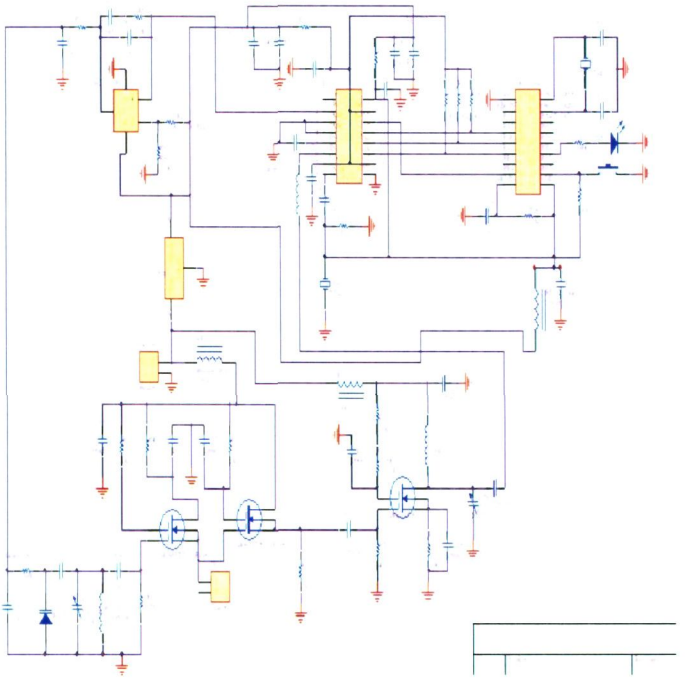
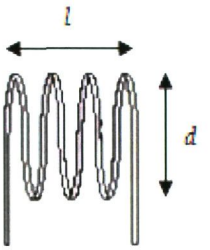


Figure 4: Schematic circuit of the PLL



Wheeler's Formula:

$$L\,(\mu H) = \frac{d^2 n^2}{18d + 40l} \qquad (1)$$

Where:
L = value of air coil inductor (in μH)
n = number of turns of the air coil (in inches)
d = length of the air coil (in inches)

Inductors used in tuning circuits are commonly referred to as coils [4]. When they are connected in series or parallel with a capacitor they resonate, electrically, at the frequency at which the inductive and capacitive reactances are equal. At resonance, the coil/capacitor combination magnifies signal voltages [5]. The LC circuit including the varactor diode is set at resonance for the particular desired frequency of the PLL system. For example, when tuning a radio to a

particular station frequency, the LC circuits are set at resonance for that particular carrier frequency.

Resonant frequency:

$$fo = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

Where:
C = capacitance (Farad)
L = inductance (Henry)
f_o = resonant frequency (Hz)

B. Software Development

The flowchart of the programming code is generally as in Figure 5. The PLL was programmed to generate a set of discrete frequencies within the range of 46 MHz to 48 MHz which will then track a RF signal transmitted from the NOAA satellites which have been down-converted to FM frequency. For the software part of the PLL, the CCS C compiler was used to compile the C and assembly language of the programming codes. CCS is a name of a company that sells a C compiler for the Peripheral Interface Controller (PIC).

The PLL used PIC16F84A as the microcontroller as it has the Flash technology. This type of PIC which can re-program electrically was the latest version manufactured by Microchip. The Flash technology makes customization of application programs extremely fast and convenient. The devices with Flash memory also allow the same device package to be used for prototyping and production. This is useful in the development of many applications where the device may not be easily accessible, but the prototype may require code updates. This special feature is therefore make this PIC16F84A match perfectly to be used in the educational field such as for student's project as it allows correction of the codes without the need to replace the device with the new one.

In the firmware, an 8 bit count is used as the "channel" number. There are four number of channels which are 0 for 46.4 MHz, 1 for 46.92 MHz, 2 for 46.8 MHz and 3 for 47.2125 MHz. Tuning of the PLL is done by a single push-button which is used for tuning the frequency up. The button will be alternately switchable to the one and another output of the desired frequencies at the VCO circuit. When the output voltage from the phase comparator moved the VCO frequency very close to the reference frequency which therefore means that the PLL succeed to "locked" the reference input frequency, the current detected frequency is obtained at the output of the VCO.

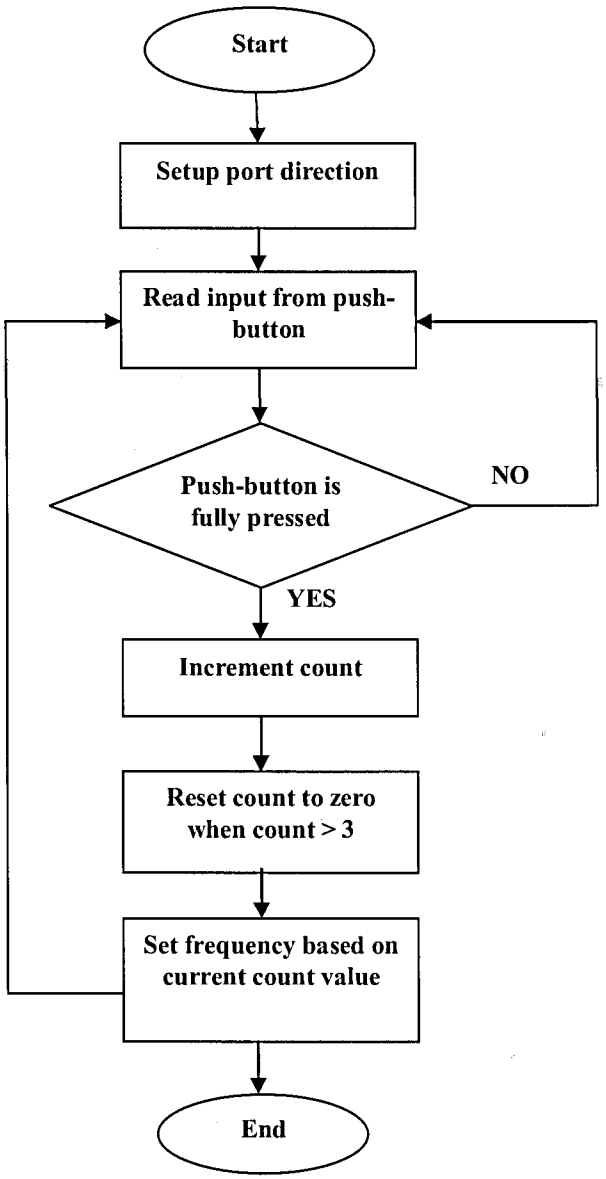


Figure 5: Flowchart of the PLL source code

C. Hardware Development

There are two inductors 772.1345 nH and 110 nH required to be constructed (L1 and L3) respectively based on requirement of the designed PLL. By using equation (1), a 772.1345 nH inductor which equal to seven turns of air coil inductor was constructed by winding the 0.6 mm diameter of copper wire tightly around 11 mm diameter drill bit. As for the 110 nH inductor, 0.6 mm diameter copper wire and 7.2 mm drill bit was used to construct the four turns of air coil inductor by using the same procedure as constructing

the 772.1345 nH inductor. Figure 6 shows the seven turns air coil inductor that has been constructed.

The inductance value for the air coil inductors constructed can be measured by using Inductance/Capacitance/Resistance (LCR) Meter. The PCB layout of the PLL is then designed by using Protel DXP 2004 as shown in Figure 7.

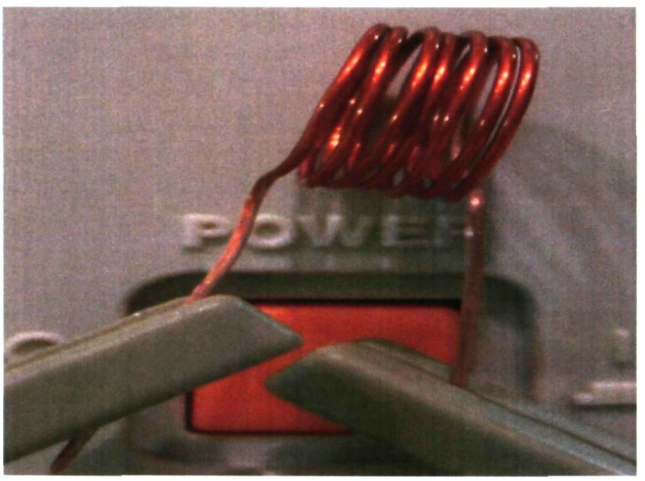


Figure 6: Seven turns air coil inductor

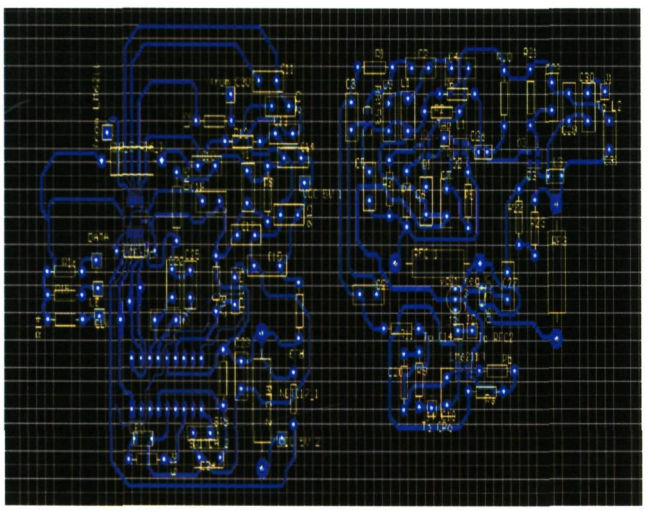


Figure 7: PCB Layout of the PLL

As shown in Figure 8, the VCO of the PLL oscillates at a resonance frequency determined by a resonant circuit composed of variable capacitance diode or varactor diode BB153, an air coil inductor L1 and a trimmer capacitor C1. The VCO is a frequency modulator controlled by a set of discrete frequencies. These discrete frequencies are 46.4000 MHz, 46.8000 MHz, 46.9200 MHz and 47.2125 MHz. The PLL ensure that all the RF frequencies transmitted from NOAA satellites are locked on a down-converted FM frequency desired by the weather satellite image receiver. The receiver system is desired to operate at 90.7 MHz.

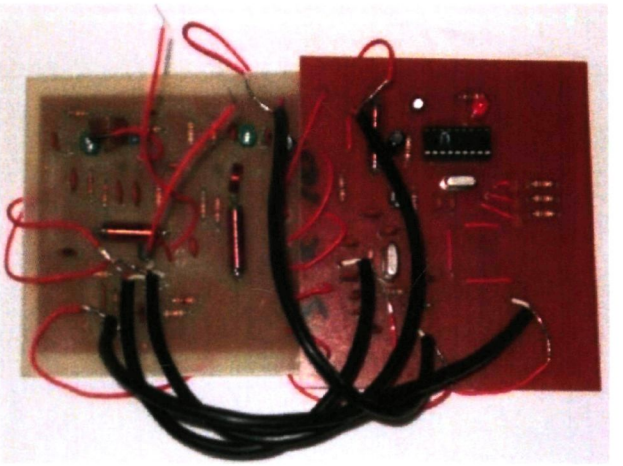


Figure 8: The prototype PLL (top view)

The small inductance's reduction of the air coil inductors L1 and L3 can be obtained by pulling the air coil turns slightly apart. It also will reduce self-resonance in the inductors. The coil inductance can be varied by widening or narrowing the winding gaps of the air-core coil thus the oscillation frequency therefore could be adjusted so that the VCO oscillates at the frequency of the reference input frequency. There are five surface mount devices (SMD) components used in the PLL which are BF998, BF991, LMX2306, LM6211 and BB153. The PLL used a 10 MHz crystal clock oscillator as the frequency reference for the PLL system. All these SMD components is soldered at the bottom of the PLL board. Figure 9 shows the bottom view of the PLL prototype.

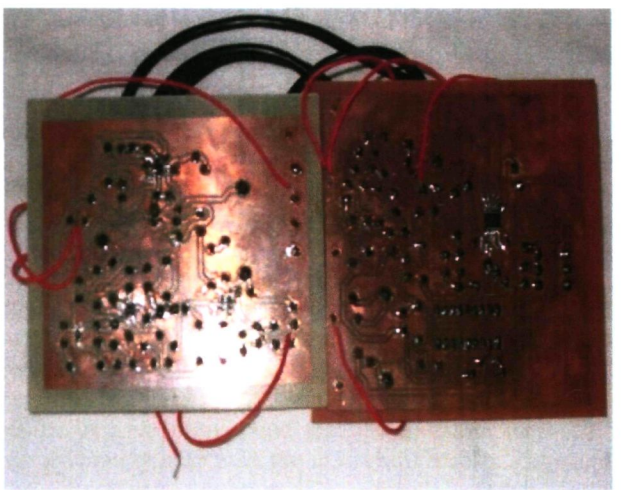


Figure 9: Bottom view of PLL prototype

III. Results & Discussions

A. Theoretical Results

The PLL was designed to generate a set of discrete frequencies and assist the receiver in tracking a RF frequency which has been down-converted to FM frequency 90.7 MHz. The desired frequencies were obtained at the VCO output..The theoretical results that should be obtained by the PLL are tabulated in Table 1.

Table 1: The theoretical results should be obtained by the PLL

Weather Satellite	RF Frequency Signal (MHz), f_{in}	Output Frequency at VCO (MHz), f_{vco}
NOAA 18	137.1000	46.4000
NOAA 17	137.6200	46.9200
NOAA 15	137.5000	46.8000
NOAA 18	137.9125	47.2125

The VCO output frequency f_{vco} was calculated by using equation (3).

VCO output frequency, f_{vco}:

$$f_{vco} = f_{in} - f_{FM} \tag{3}$$

Where:
f_{vco} = Output frequency at VCO (MHz)
f_{in} = RF signal transmitted from NOAA satellites
f_{FM} = Operating frequency of the receiver in electrical engineering faculty of UiTM Shah Alam (90.7 MHz)

Where f_{FM} is 90.7 MHz which is the most silence FM frequency generally in Universiti Teknologi MARA (UiTM), Shah Alam and specifically at the Faculty of Electrical Engineering. The frequency was down-converted to FM frequency because the operating frequency of the receiver system is within radio range.

B. Measurement Results

The built prototype of the PLL was tested in the laboratory to verify its functionality. By using a 12V DC supply, a 9V DC supply and a spectrum analyzer, the measurement setup is constructed as shown in Figure 10.

The 12V DC supply is connected to the input of the VCO at input of the VCO circuit and the voltage is varies between 0V to 12V. The spectrum analyzer will show the output signal in the frequency domain. The 9V DC supply is used as bias voltage to drive the transistor. The results obtained from the spectrum analyzer were shown in the following figures.

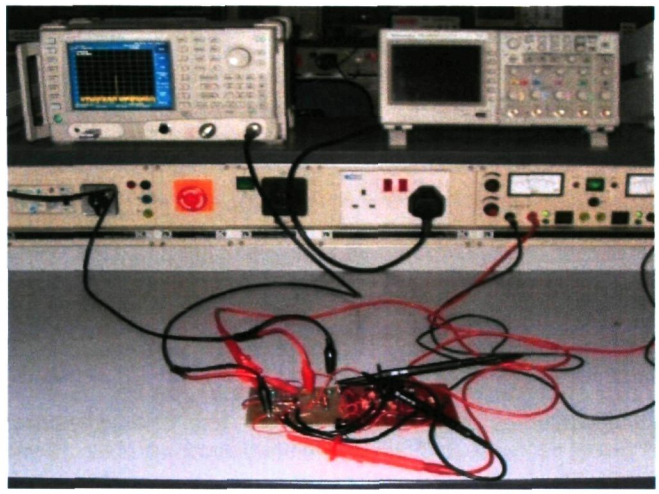


Figure 10: Equipment setup for measurement

Figure 11, 12, 13 and 14 show the results on the spectrum analyzer which display the VCO output frequency measured at 46.40 MHz, 46.92 MHz, 46.80 MHz and 47.2125 MHz respectively.

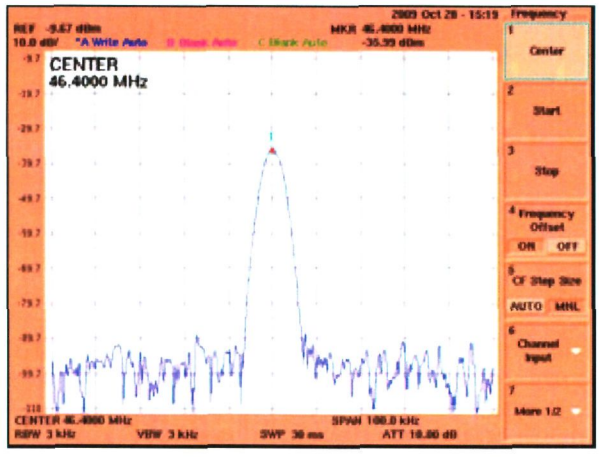


Figure 11: Measured VCO output at 46.40 MHz

The results obtained from the measurements were compared with the results tabulated in Table 1. From the comparison done between the measurements and theoretical results, it have been found that the measurements results was accurately tally with the theoretical results. The results also show this PLL system will ensure the weather satellite system receiver will always stay in track with the receiver system operating frequency which is 90.7 MHz.

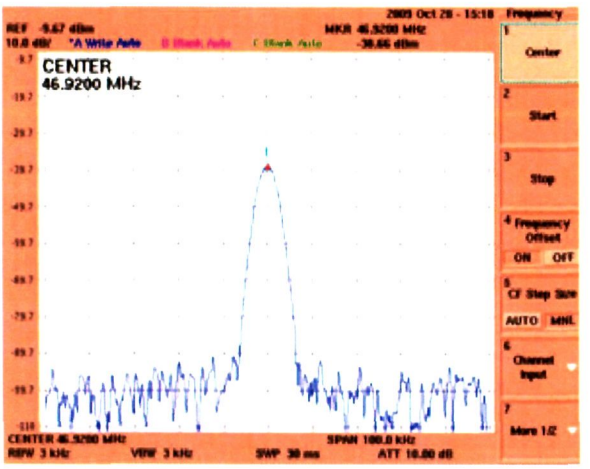


Figure 12: Measured VCO output at 46.92 MHz

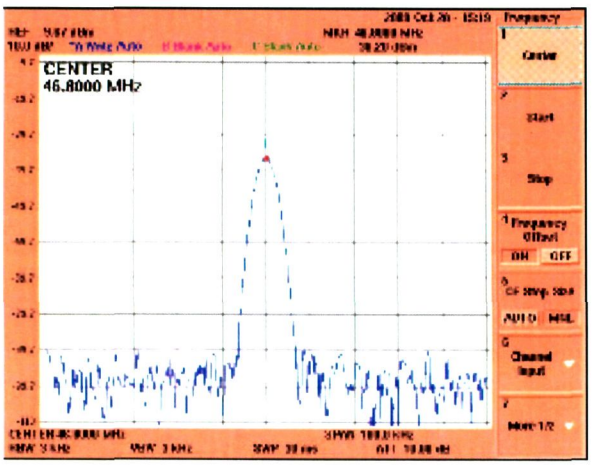


Figure 13: Measured VCO output at 46.80 MHz

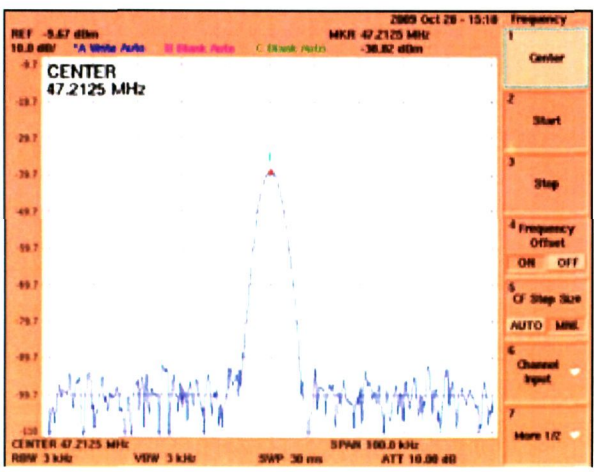


Figure 14: Measured VCO output at 47.2125MHz

IV. Conclusion

It can be concluded that the PLL is successfully designed to operate at desired frequencies. Besides that, it is also easier to develop the firmware of the PLL by using C programming language rather than using others programming language because of its simplicity and easy to debug. It was found that the VCO oscillates at the center of desired frequencies and therefore effectively locked the PLL to match the frequency of an input signal. The input signal frequency is actually a set of discrete frequencies. It was also finally found that the PLL is a basic building block that can be used in just about any application where a frequency needs to be synthesized.

V. Future Development

For future research and development, some recommendations and improvement can be taken. A squelch circuit could be implemented into the PLL as it can detect the presence of an RF input signal and therefore could improve the performance of the PLL. It is also recommended to use one LED for each channel to display the current channel being locked by the PLL at a particular time as it would enhance the readability of the frequency being detected.

It also recommended that the PLL may enclose with a weather proof die cast aluminum enclosure as to enhance RF insusceptibility. To reduce the size of the PLL board, it is recommended to use as much as possible surface mount devices (SMD) components. It also would allow much more components to be placed on the board and reduce the copper pour areas which will lead to lower the resistance and inductance at the connection. Consequently it would lead to a better performance of the high frequency components.

VI. Acknowledgment

The author would like to express gratitude to all the people who have given a lot of guidance and supports throughout completing this project. I would like to thank Puan Robiatun Adayiah Bt Awang and Mr. Mohd Fadhil B. Sayuti as the supervisor of this project for their invaluable guidance, patience, suggestions, encouragements and supports throughout the entire project. I also feel grateful to the laboratory instructor for the technical supports in measurement and equipment setups. Last but not least, my deepest appreciation goes to my beloved family for their moral support, motivation and understanding towards finishing this project.

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