IMPLEMENTATION AND SIMPLIFICATION OF AN OUTPUT SHIFTED CODING MODULATION (OSCM) ON A HIGH SPEED DSP PROCESSOR.

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ABSTRACT

Forward error correction (FEC) codes are a subclass of error correcting codes, have become an invaluable tool in 'closing' the link budget of wireless-based digital communications systems. The disadvantage of FEC is the tradeoff between error performance and the decoding complexity resides on the choice of the code constraint length. A solution to this problem was provided by Ungerboeck, who presented a technique which is called Trellis Coded Modulation (TCM). However, there is still a trade-off at work; trellis coded modulation achieves coding gain at the expense of decoder complexity. Due to this problem, a new coded modulation which is a combination of forward error correction codes (convolutional and Viterbi codes) and $\pi/4$-shift DQPSK is discussed in this research. The new coded modulation is called as Output Shifted Coding Modulation (OSCM). This algorithm also shows that by using low constraint length convolutional component codes, it can outperform the convolutional codes using Viterbi decoders with much higher constraint lengths. It is capable of reducing the bandwidth expansion by using $\pi/4$-shift DQPSK. This is achieved through fine tuning the set of rules for the mapping of coded bits and also with modifying error detection and correction techniques in trellis diagram.

The research work continues with the implementation of digital baseband signal processing with OSCM function on Digital Signal Processor (DSP) Kit TMS320C6711. Single DSP chip is used to implement the baseband processing function due to compactness, low-power consumption and flexibility. C6711 is a member of the high performance DSP family from Texas Instruments (TI) that incorporated the real-time kernel known as DSP/BIOS. The design environment is based on Code Composer Studio IDE (Integrated Development Environment) and the DSP functions are simulated on 150MHz clock C6700 DSP simulator.

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CHAPTER 1 : INTRODUCTION TO OUTPUT SHIFTED CODING MODULATION (OSCM)

1.1 OSCM Encoder

OSCM encoder consists of modified convolutional encoder (CE) and $\pi/4$-shift DQPSK modulator as shown in Figure 1.1. This encoder consists of G (7, 5), K=3 CE, which located in the left of the OSCM encoder, while in the right side consist of $\pi/4$-shift DQPSK modulator with lookup table systems. OSCM encoder starts with CE operation. The information sequence $b_k = (b_0, b_1, b_2, \ldots, b_n)$ enters the encoder one bit at a time. Since the encoder is a linear, two encoder output sequences $c_k^{(1)} = (c_0^{(1)}, c_1^{(1)}, c_2^{(1)}, \ldots)$ and $c_k^{(2)} = (c_0^{(2)}, c_1^{(2)}, c_2^{(2)}, \ldots)$ can be obtained as the convolution of the input sequence b_k with the two encoder "impulse responses". The impulse responses are obtained by letting $b_k = (1\ 0\ 0\ \ldots)$ and observing the two output sequences.

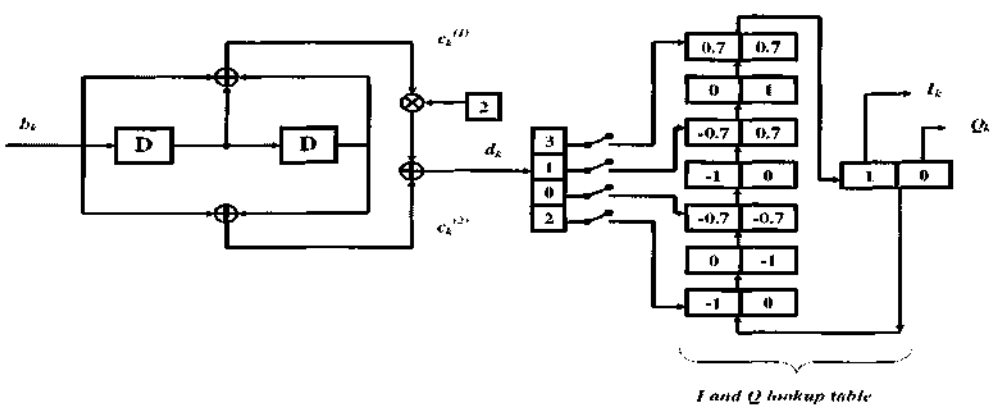

Figure 1.1 Output shifted coding modulation encoder.

Lets the input bit is defined as

$$b(D) = b_0, b_1, b_2, \ldots, b_n \tag{1.1}$$

From trellis diagram for G (7, 5), two lookup table are developed which are next state lookup table (Table 1.1) and output lookup table (Table 1.2). From Table 1.1, the possible transition of state can be written as: