DESIGNING A PHASE-LOCKED LOOP FOR A WEATHER SATELLITE IMAGE RECEIVER

This thesis is presented in partial fulfillment for the award of the

Bachelor of Electrical Engineering (Hons)

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AKNOWLEDGEMENT

All praise is to Allah S.W.T, The Most Gracious and Most Merciful who has given me the strength, ability and patience to finish this project successfully. I would like to thank my friends for all the continuous encouragement and support for me.

First and foremost, I would like to express my sincere gratitude and appreciation to my project's supervisor, Puan Robia'tun Adayiah Bt Awang for her invaluable guidance, patience and encouragement throughout the development of this project. I also would like to express my highest gratitude to Mr. Mohd Fadhil B. Sayuti ATSB for his numerous technical comments, advices and ideas throughout the entire project. Besides that, I also feel grateful to the laboratory instructor for the technical supports in measurement and equipment setups. I greatly want to express my best gratitude to all the people who have given a lot of guidance and support towards completion of this project.

Last but not least, my deepest appreciation goes to my beloved family. I am grateful to my parents for their love and support in my whole life. Their confidence in me and their high expectation of me are the driving forces for completion of this work.

ABSTRACT

This thesis presents design of a phase-locked loop (PLL) at operating frequencies from 46 MHz to 48 MHz for a weather satellite image receiver. The main objective of the designed PLL is to assist the receiver system to track a radio frequency (RF) signal transmitted from the National Oceanic and Atmospheric Administration (NOAA) satellite which has been down-converted to frequency modulation (FM) frequency 90.7 MHz. The PLL is part of a low cost ground receiving system for Automatic Picture Transmission (APT) image reception. The PLL software was designed and compiled using CCS C compiler and used Peripheral Interface Controller 16F84A (PIC16F84A) as the microcontroller while the PLL hardware was designed and then fabricated on a printed circuit board (PCB) using Protel DXP 2004. The PCB design layout for the PLL was also constructed by using Protel DXP 2004. For the practical testing of the PLL a 12V DC supply, a 9V DC supply and a spectrum analyzer are used to verify the functionality of the designed PLL. From the measurement, the PLL is recorded to operate at the desired frequencies.

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