DYNAMIC RECONFIGURABLE BPSK MODULATION SCHEME USING VHDL

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ABSTRACT

This thesis presents the simulation of a BPSK (Binary Phase Shift Keying) modulation using a Xilinx ISE (Integrated Synthesis Environment) and a Xilinx System Generator development tool and implementation in a FPGA Xilinx Spartan-3 FPGA (Field Programmable Gate Array) development board. This thesis describes a methodology for top-down design, modeling, synthesize and simulation of BPSK modulation using (VHDL) Very High Speed Integrated Circuit Hardware Description Language.

TABLE OF CONTENTS