UNIVERSITI
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MARA

THE EFFECT(S) OF MASK ALIGNMENT TO P-N JUNCTION

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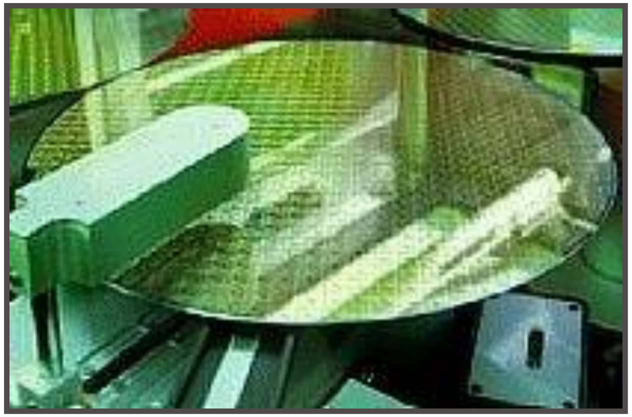
INTRODUCTION

Semiconductor

- **Definition** : Materials that have an electrical conductivity between a conductor and insulator.



- Important properties of semiconductor is the ability to change its electrical conductivity that make it suitable in making devices.

- The process to change its electrical conductivity is called diffusion process.

[1,2]

Diffusion process

- **Definition**: One of doping process method where controlled amount of impurity being added into the semiconductor , that can be classified as n-type semiconductor and p-type semiconductor.

N-type semiconductor

Donor impurity atoms have been added. The density of electrons is greater than the density of holes.

P-type semiconductor

Acceptor impurity atoms have been added. The density of holes is greater than the density of electrons.

[1,2]

Photolithography

- ❑ Photolithography is a patterning process that transfers the pattern on the mask or reticle to the photoresist on the wafer surface.

❑ Mask

Mask is an image that coat the wafer surface. The image on the mask normally designed using software from the computer. The pattern in designing the mask depends on the circuit requirements.

❑ Photoresist (PR)

Photosensitive materials used to temporary coat the wafer and to transfer the optical image of the device design on the mask to the wafer surface. Photoresists are sensitive to UV light and for this reason, photolithography process should be done in a yellow room.

Problem statement

- Mask alignment is one of the critical processes in producing a simple p-n junction. If the mask used is not align with the previous mask design circuit failure could occur. [1,2]

- The mask alignment is depending on the design of the mask and the dimension of the device created on the mask. Different mask designs would have different kind of device. In order to fabricate a simple p-n junction, the design of the mask and the dimension of the device is important in determination of the functionality of the p-n junction.

Significance of study

- This study simplify the mask alignment process in fabrication of a simple p-n junction .

- Optimize the dimension of the device where the pattern is easy to be transfer on the wafer in fabricating a simple p-n junction.

- To design a suitable mask that is easy to transfer the pattern on the wafer to fabricate p-n junction.

Objectives of study

- To study the effect of mask alignment to the p-n junction.

- To create the most suitable mask to fabricate a simple p-n junction.

- Determine the effect of the different mask design and different dimension of device to the p-n junction.

LITERATURE OF REVIEW

P-N junction

- ❑ A p–n junction is a junction formed by joining p-type and n-type semiconductors together in very close contact. The term junction refers to the region where the two regions of the semiconductor meet.

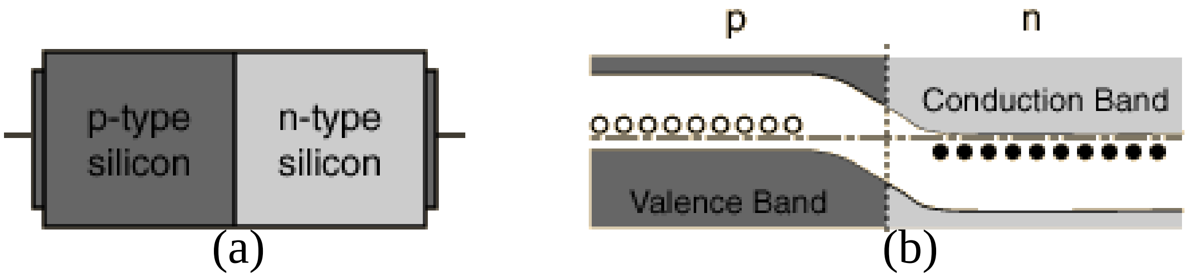


Figure 1 : (a) P-N junction. (b) Energy band at equilibrium

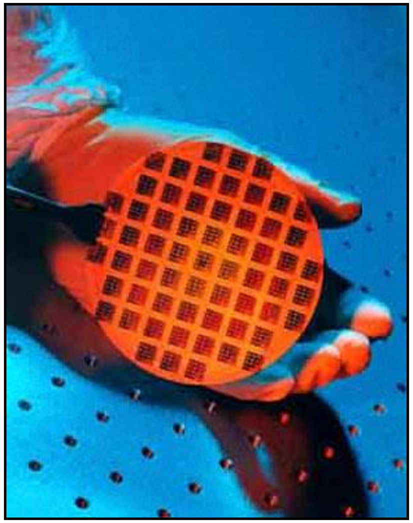
Mask and mask alignment

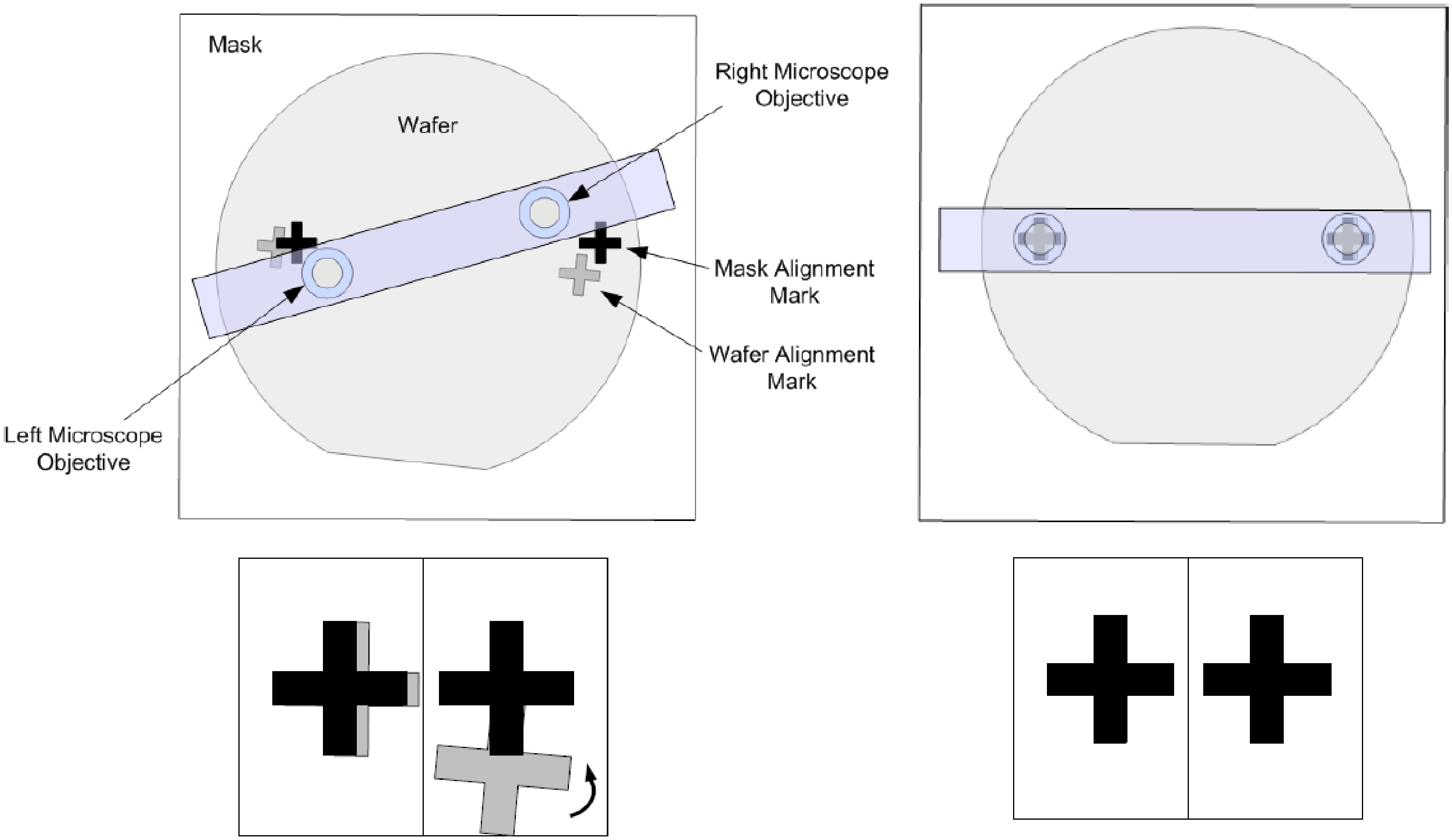
❑ Mask design

A computer aided design (CAD) system used in which designers can completely describe the circuit patterns electrically. [5]

TURBO CAD is a suite of CAD software products for 2-dimensional design and drafting.

- ❑ One of the steps in photolithography is mask alignment. Mask alignment is a process to align every mask that is used. The mask design for the pattern of the device and the alignment mark play a very important role.



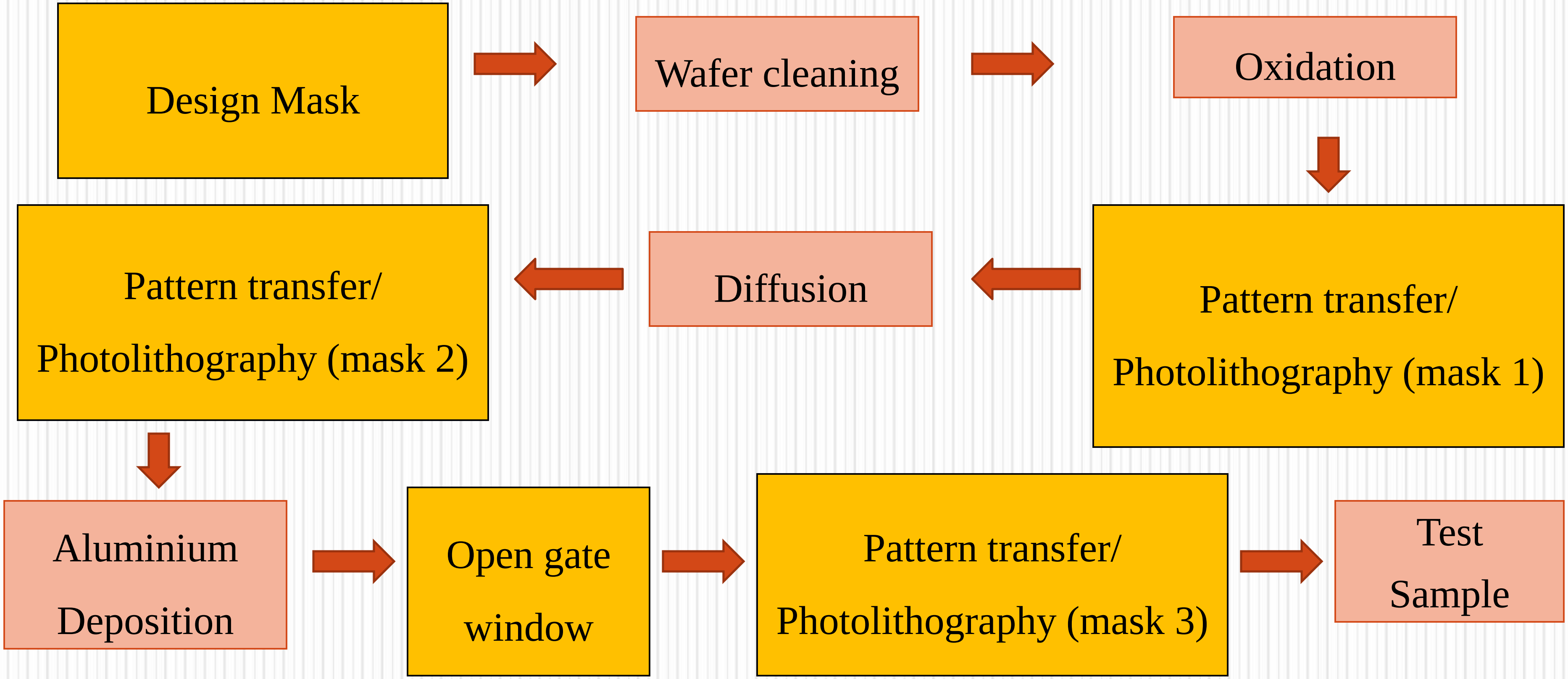


(a)

(b)

Figure 2 : (a) Example of how to align alignment mark and the view of the mark . (b) Example of the align mask. Adapted from [4]

METHODOLOGY



Design Mask

Wafer cleaning

Oxidation

Pattern transfer/ Photolithography (mask 1)

Diffusion

Pattern transfer/ Photolithography (mask 2)

Aluminium Deposition

Open gate window

Pattern transfer/ Photolithography (mask 3)

Test Sample

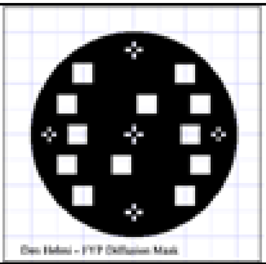
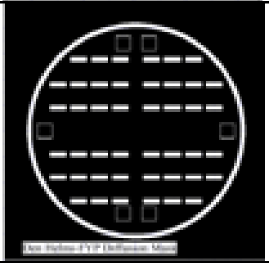
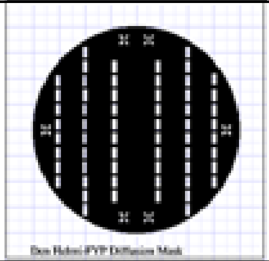
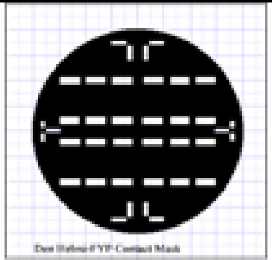
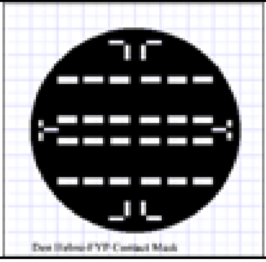
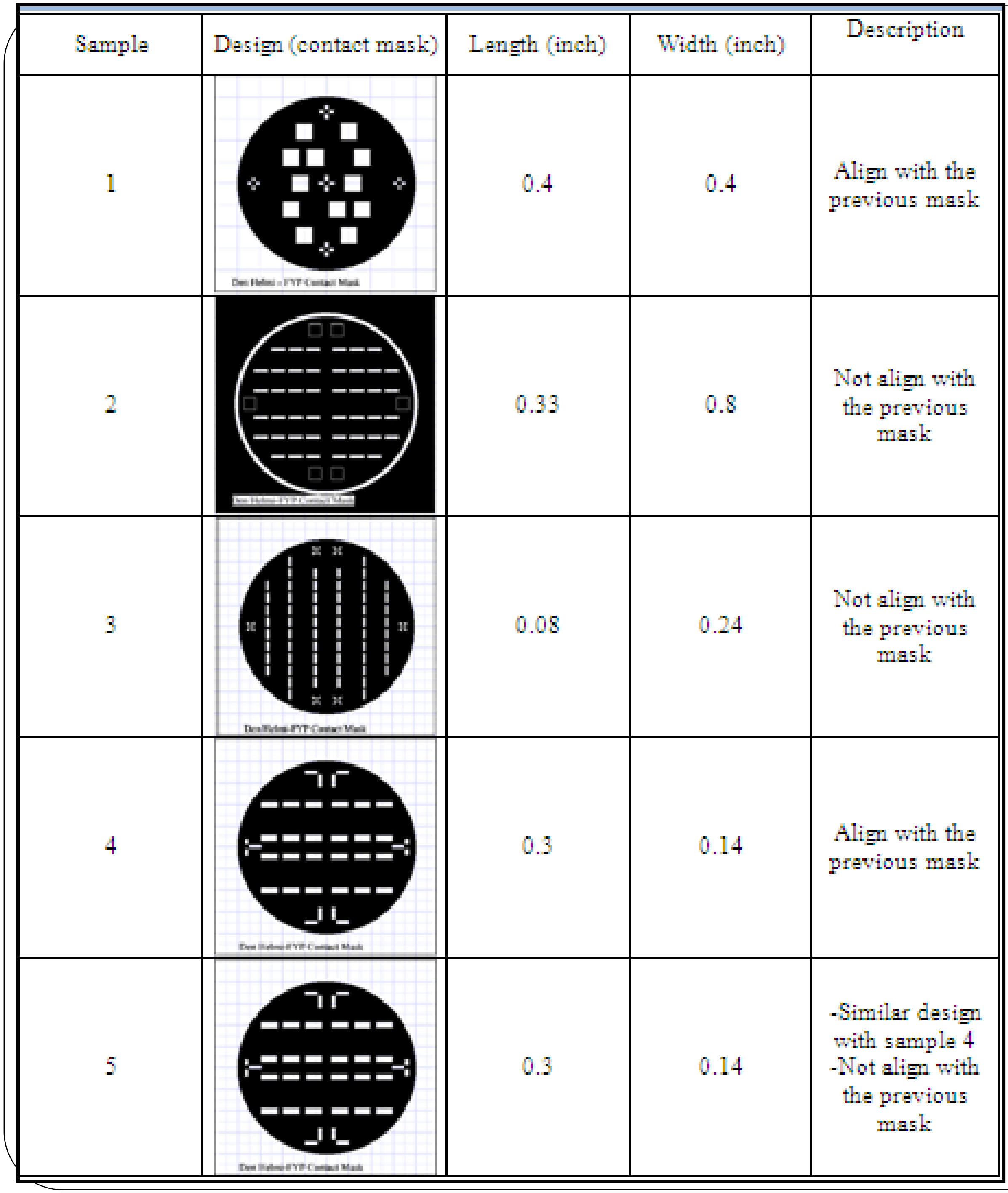
Sample	Design (diffusion mask)	Length (inch)	Width (inch)	Description
1		0.4	0.4	-
2		0.33	0.1	-
3		0.1	0.24	-
4		0.4	0.15	-
5		0.4	0.15	Similar design with sample 4

Table 1 : Diffusion mask

- ❑ Diffusion mask used to define the area of diffusion.

- ❑ This mask is important so that the area that will be doped with the dopant could be verified.

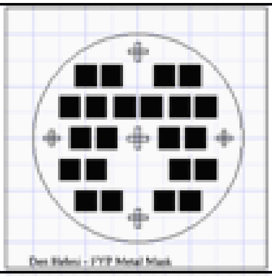
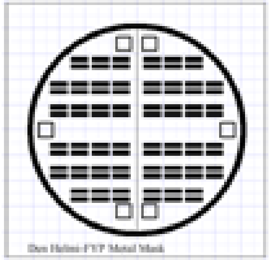
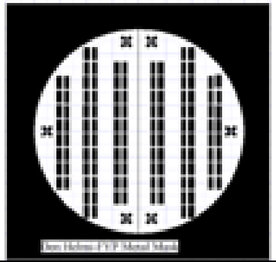
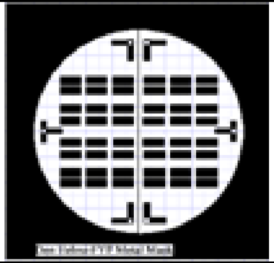
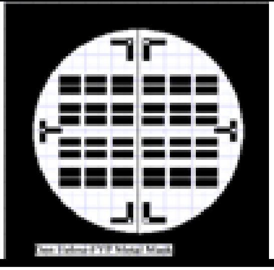
Table 2 : Contact mask



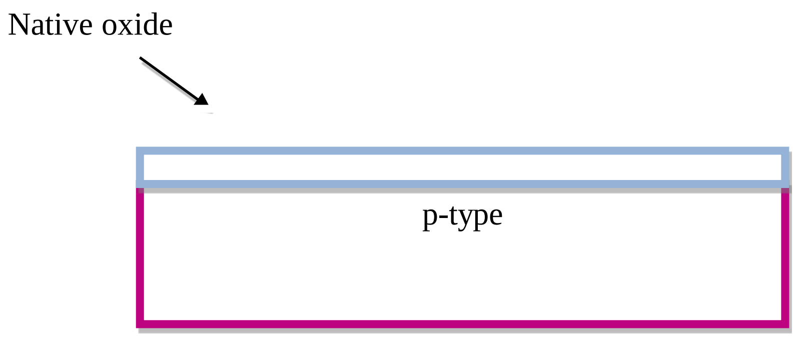
Sample	Design (contact mask)	Length (inch)	Width (inch)	Description
1		0.4	0.4	Align with the previous mask
2		0.33	0.8	Not align with the previous mask
3		0.08	0.24	Not align with the previous mask
4		0.3	0.14	Align with the previous mask
5		0.3	0.14	-Similar design with sample 4 -Not align with the previous mask

- ❑ Contact mask used to define the area of contact between p-type and n-type silicon wafer after diffusion process.

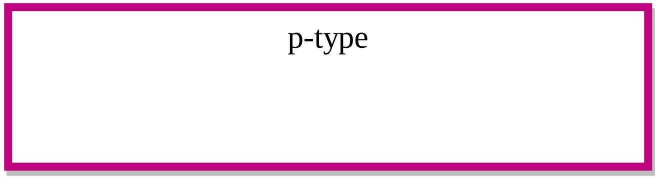
Table 3 : Metal mask

Sample	Design (metal mask)	Length (inch)	Width (inch)	Description
1		n = 0.4 p = 0.4	n = 0.4 p = 0.4	Align with the previous mask
2		n =0.33 p = 0.1	n =0.33 p = 0.8	Not align with the previous mask
3		n = 0.1 p = 0.08	n = 0.24 p = 0.24	Not align with the previous mask
4		n = 0.4 p = 0.3	n = 0.15 p = 0.14	Align with the previous mask
5		n = 0.4 p = 0.3	n = 0.15 p = 0.14	Not align with the previous mask

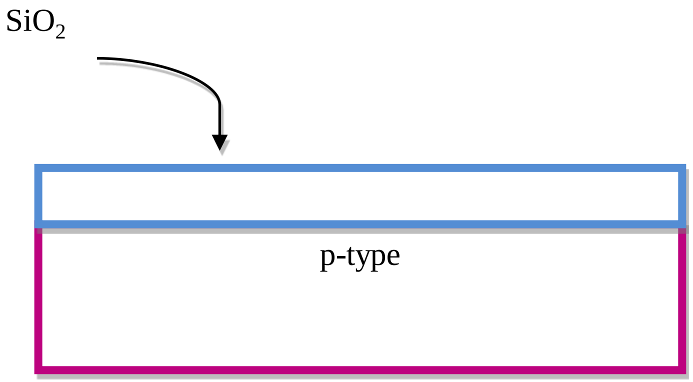
❑ Metal mask used to define the area that required metal on the wafer surface.



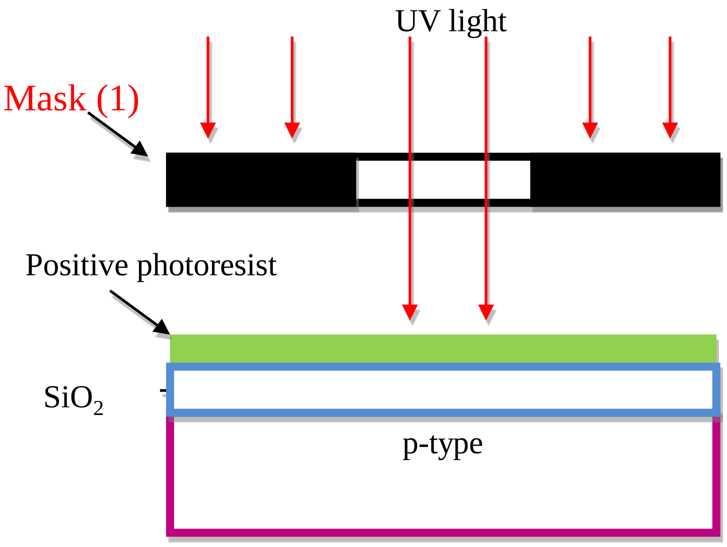
- Start with p-type silicon wafer
- The native oxide may growth on the wafer surface



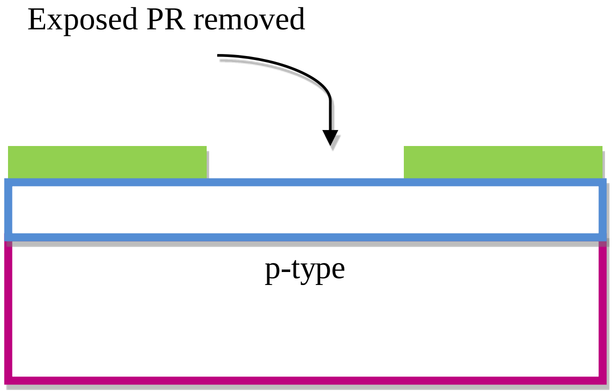
- The native oxide removed by using Buffer Oxide Etch (BOE).



- The wafer undergo oxidation process for half an hour.

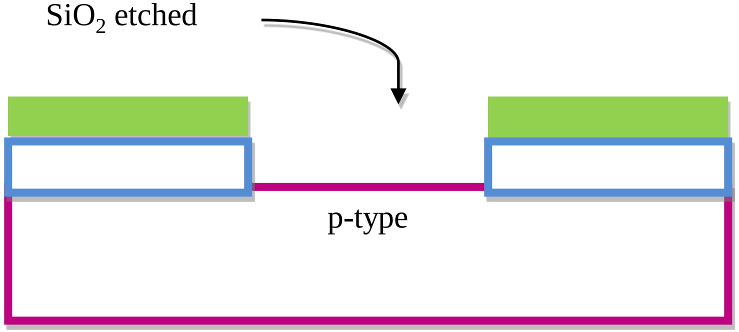


- Coat the wafer with photoresist (PR) .
- PR layer being exposed through mask (1), diffusion mask, for 50 seconds



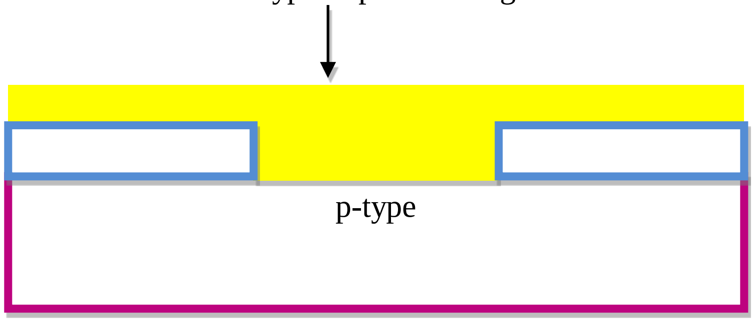
- The exposed PR removed using resist developer.

SiO$_2$ etched



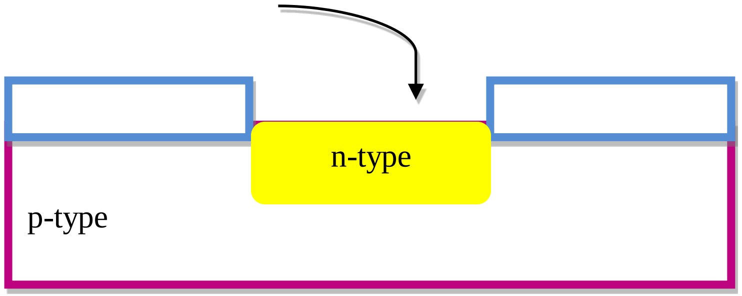
- The uncover SiO$_2$ layer removed using BOE solution. This process take about 3 minutes 30 seconds.

N-type dopant coating

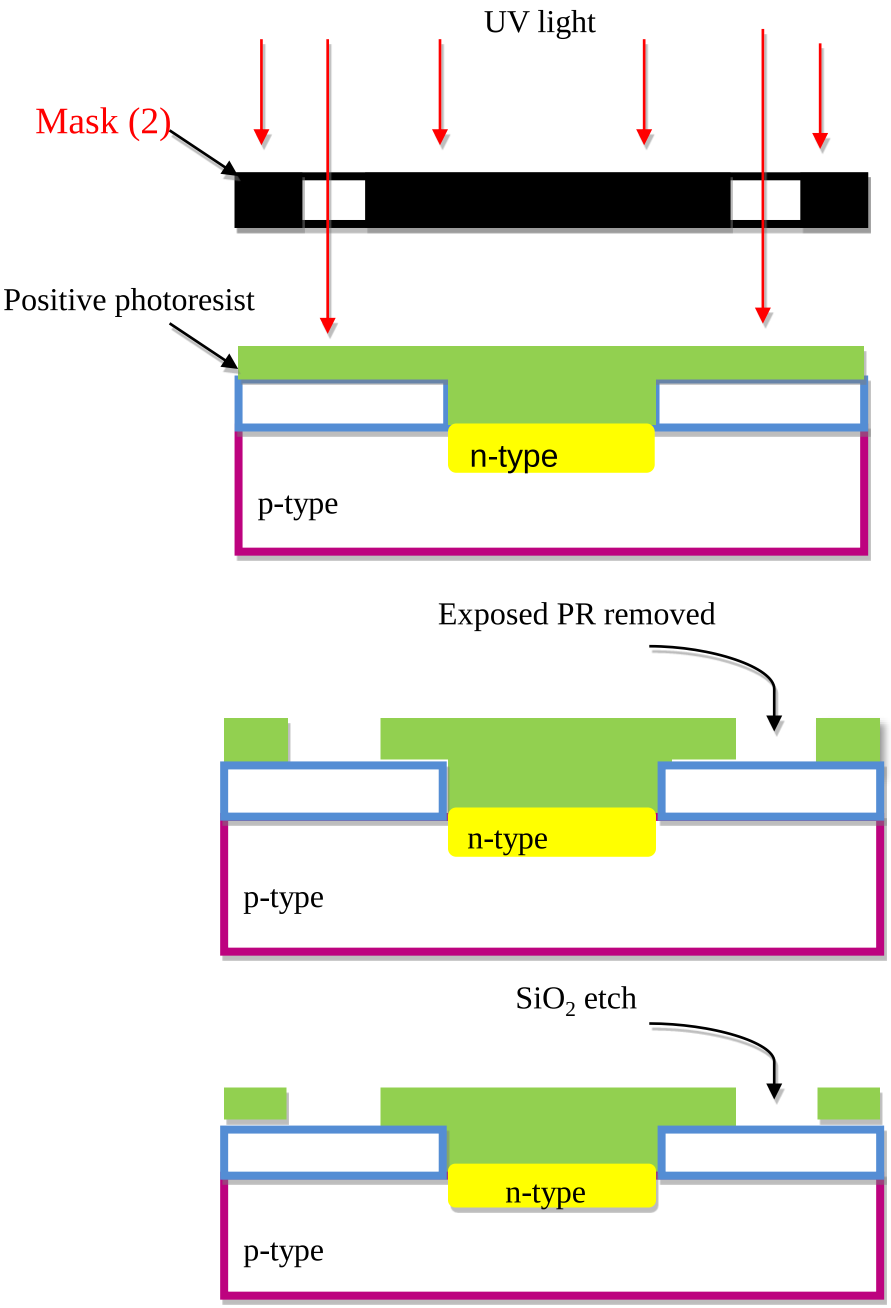


- The n-type dopant (phosporus) applied on the wafer surface.

Diffusion of dopant



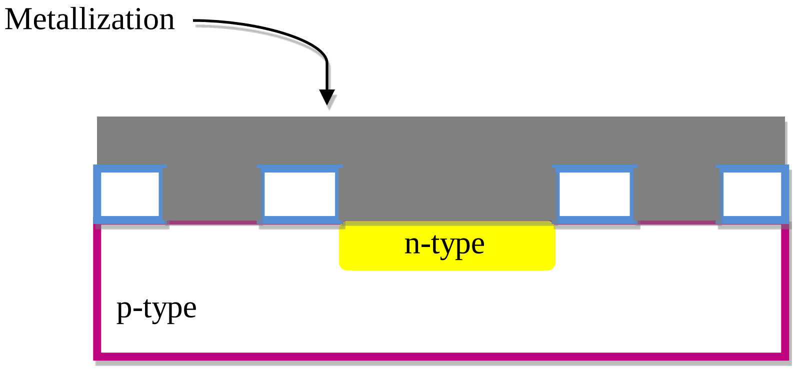
- Undergo the diffusion process for 1 hour.

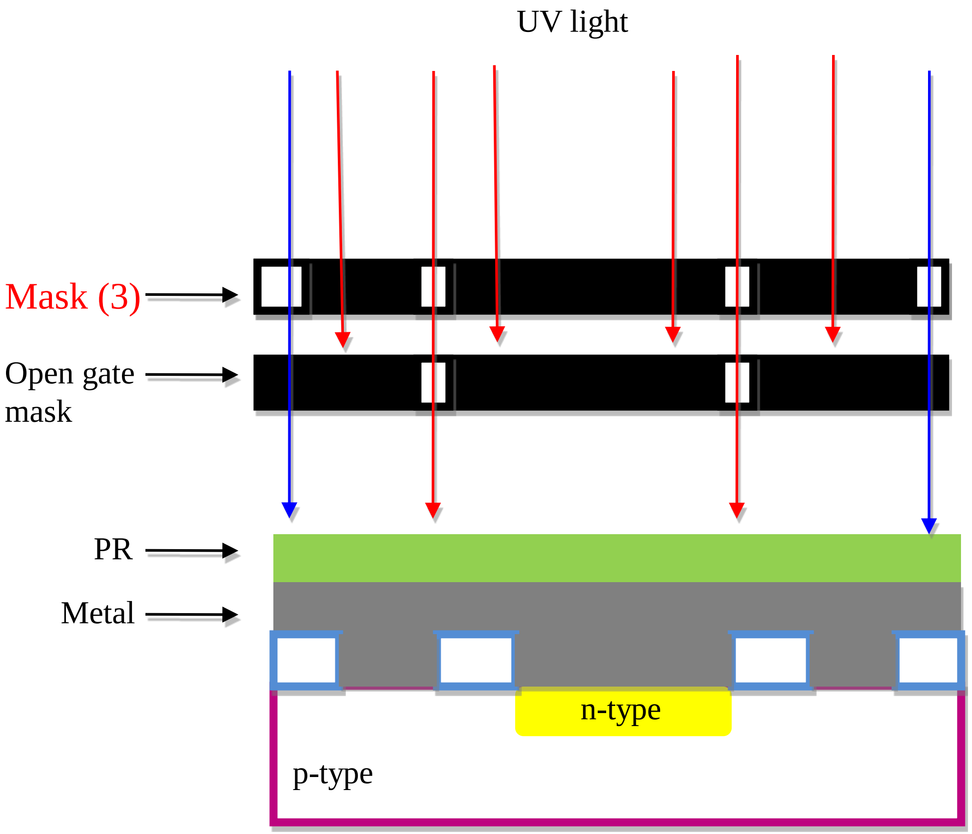


- PR coating on the wafer surface
- The PR exposed through mask (2), contact mask.

- The exposed PR removed by using developer.

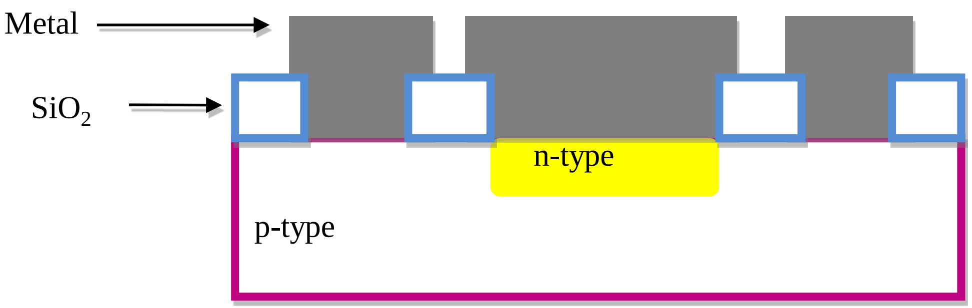
- SiO_2 etched by using BOE.
- The uncover layer removed.





- Metal deposition process.
- Metal layer added on the wafer surface.

- The alignment mark opened using the open gate mask.
- After that, mask (3), metal mask, used to define the area of metal.



- The PR removed and then undergo the metal etch process.
- Testing

RESULTS

SHEET RESISTANCE, R_S

- Sheet resistance is a measure of resistance of thin films that have a uniform thickness.
- For this project sheet resistance measured before and after doping process for every samples.
- All samples go through diffusion process for 1 hour at 900°C in temperature.
- $R_S = \rho / t$ where t = sheet thickness,

  R_S = sheet resistance,

  ρ = resistivity

Table 4

Average sheet resistance, R_s for different samples before and after undergoing diffusion process for 1 hour at temperature of 900℃

Sample	Average Sheet resistance (Ω/□)	
	Before diffusion	After diffusion
1	258.72	244.91
2	259.95	558.57
3	319.18	578.64
4	241.37	265.14
5	231.82	293.42

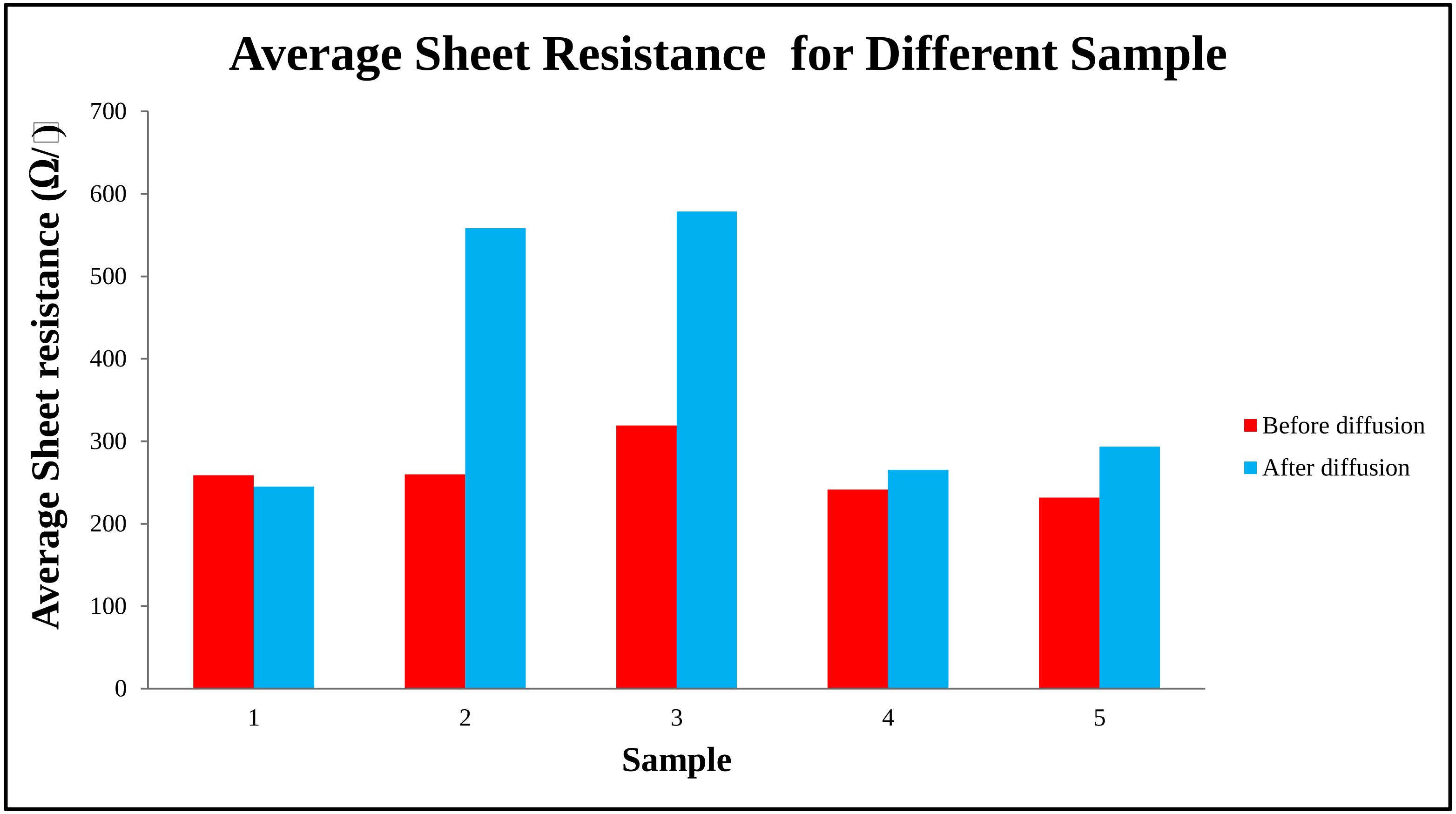


Figure 3: Bar chart of average sheet resistance, R_s for different samples before and after undergoing diffusion process for 1 hour at temperature of 900°C

Table 5
The percentage of increase of sheet resistance for different sample with different length and width per device

Sample	Length (inch)	Width (inch)	Percentage increase (%)
2	0.33	0.10	114.88
3	0.10	0.24	81.29
4	0.40	0.15	9.85
5	0.40	0.15	25.57

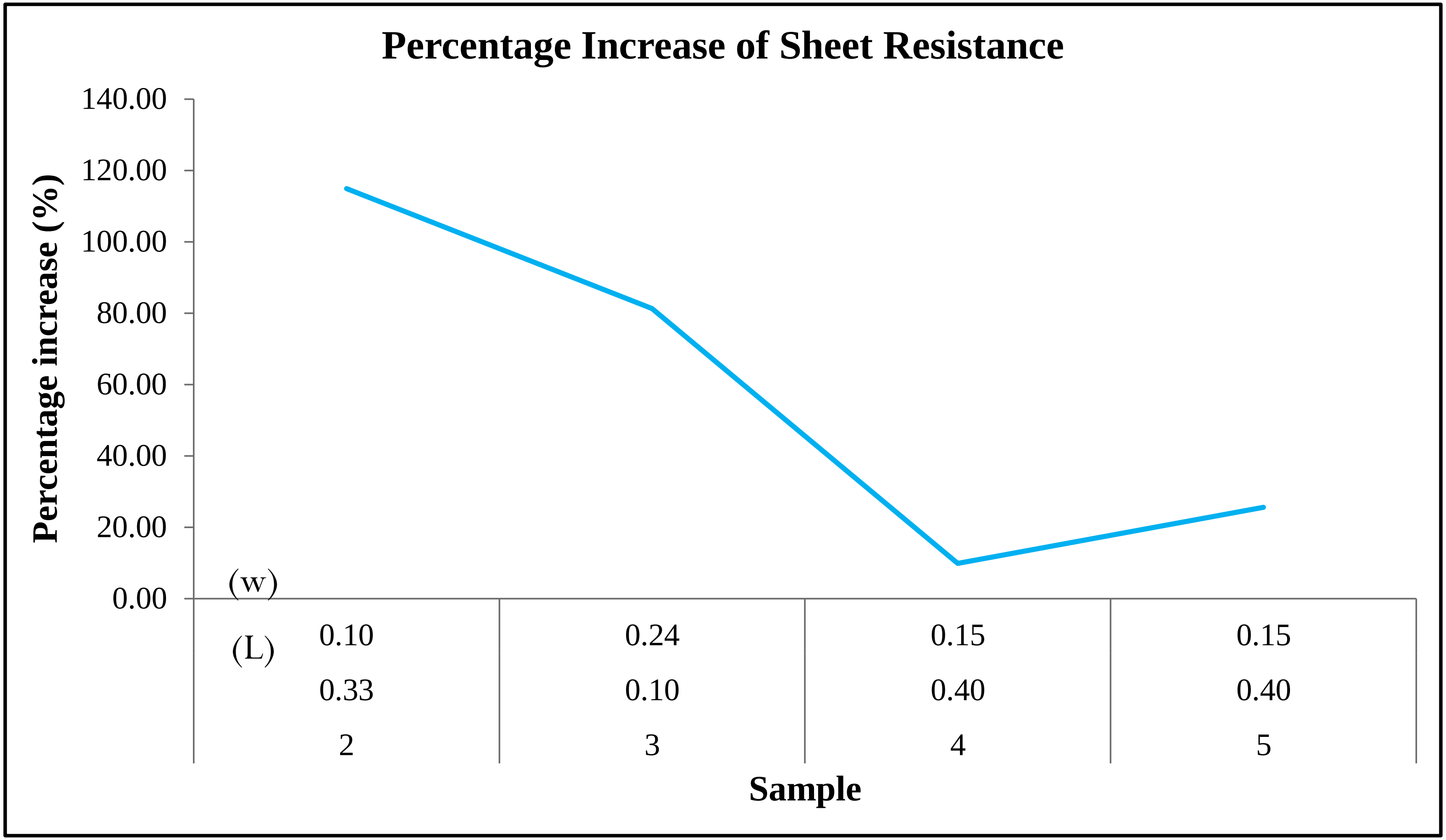


Figure 4: Graph of percentage increase of sheet resistance for different sample with different width and length per device

I-V CHARACTERISTICS

- A current-voltage characteristics is a relationship, typically represented as a chart or graph, between electric current and a corresponding voltage, or potential different.
- I-V characterization machine used.

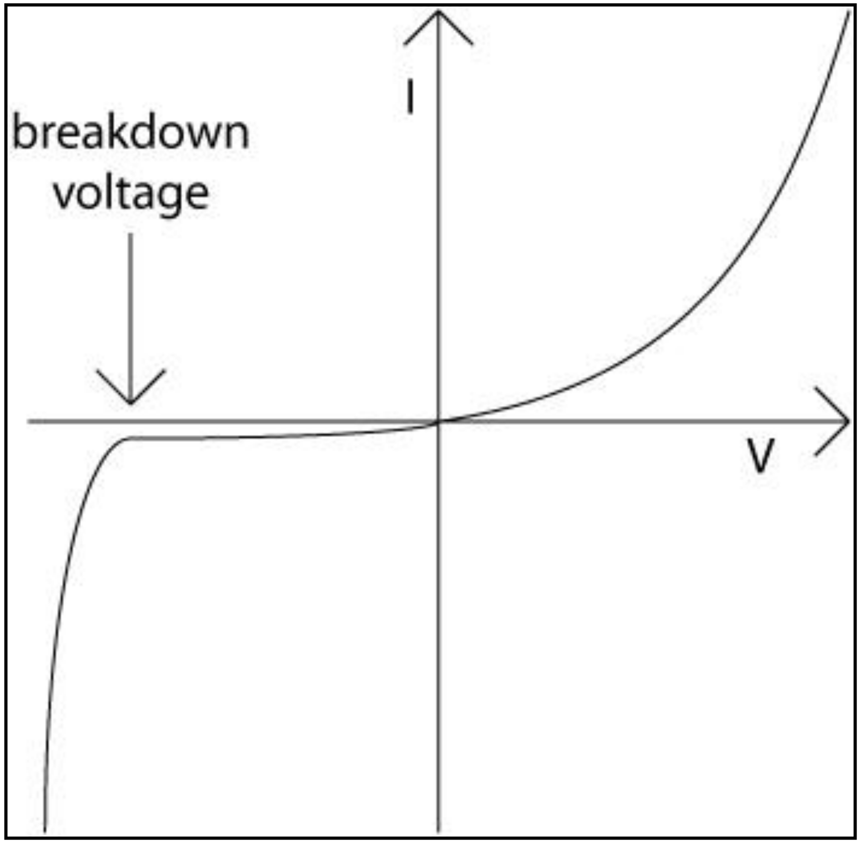


Figure 5: Actual graph of I-V curve for p-n junction

- From ohm’s law,

$$V = IR \qquad (1)$$

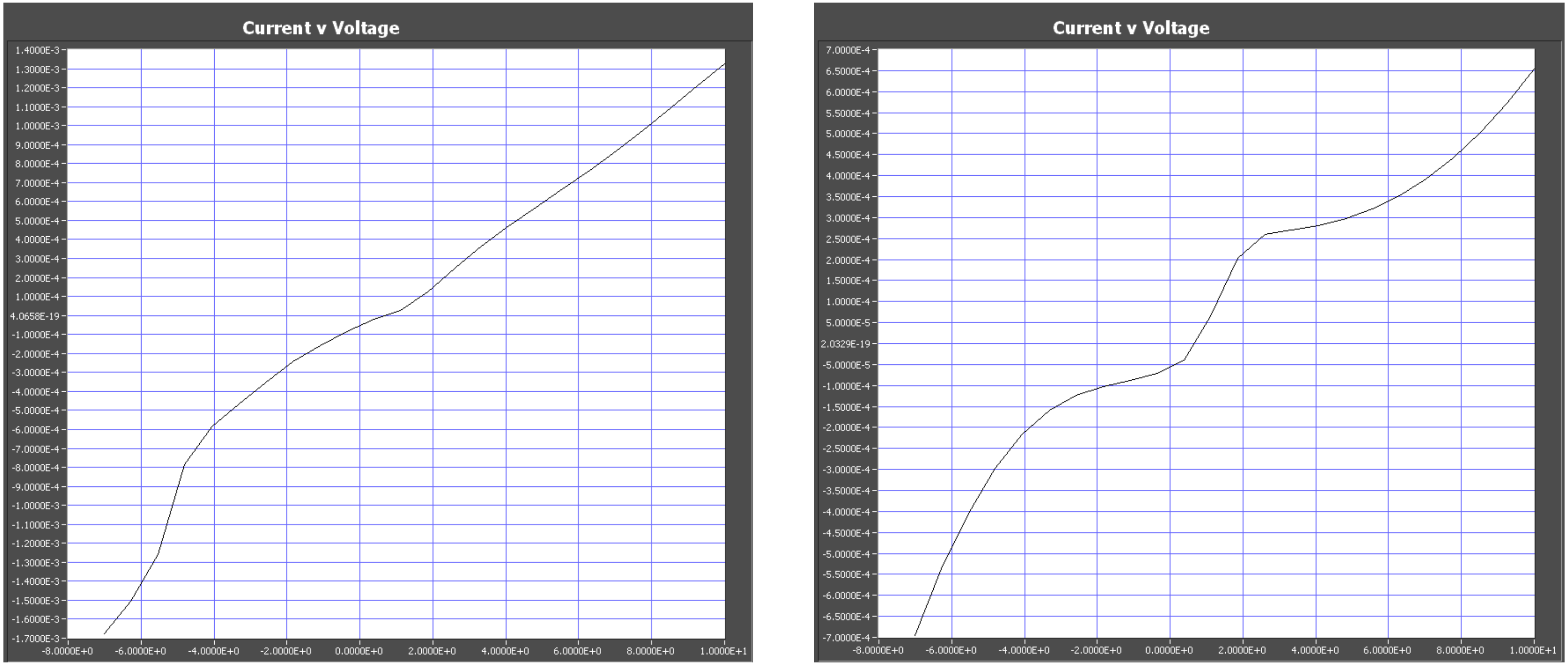
- From the graph of I-V curve, the gradient, m is equal to I/V. So from this equation, the value of R can be calculated.

$$m = \frac{1}{R} \qquad (2)$$

So,

$$R = \frac{1}{m} \qquad (3)$$

I-V curve for sample where the masks are NOT ALIGN



(a)

(b)

Figure 6: Example I-V curve taken from (a) sample 2 and (b) sample 5

I-V curve for sample where the masks are NOT ALIGN

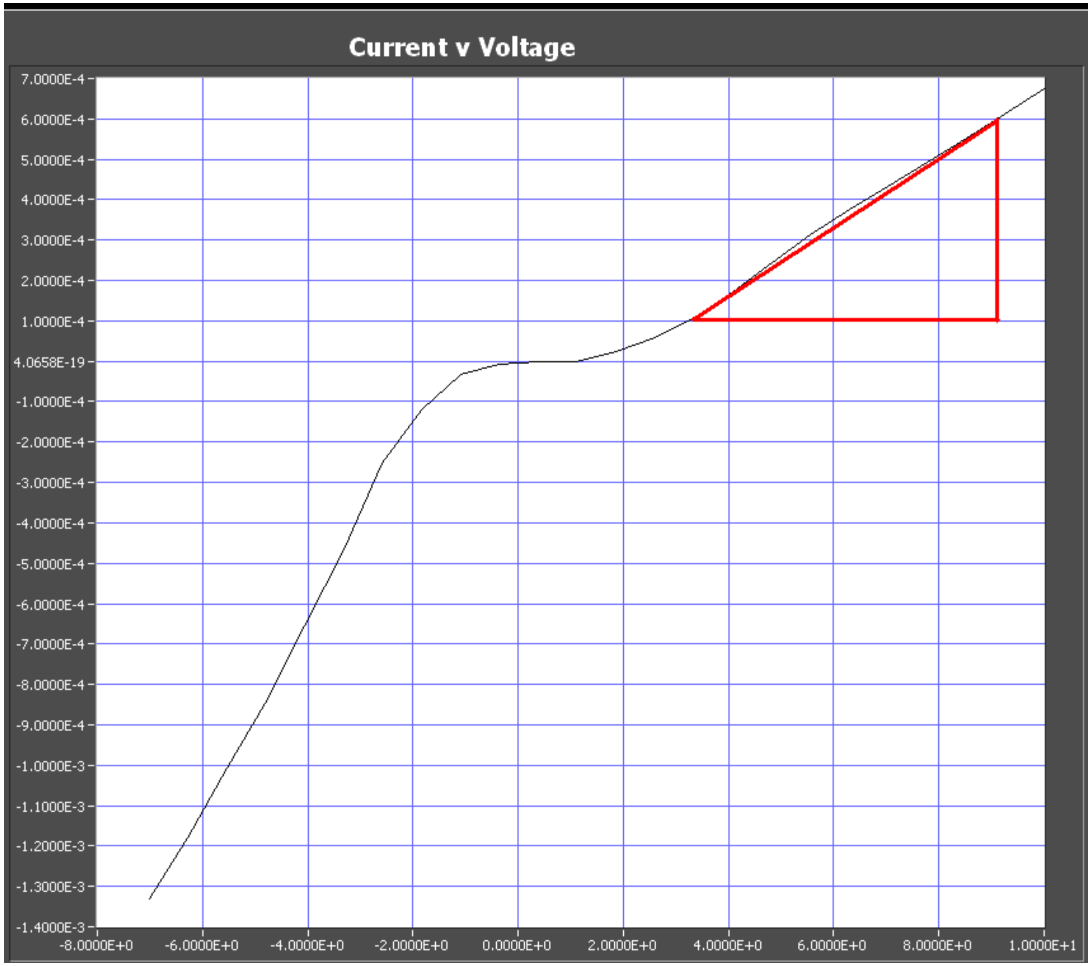


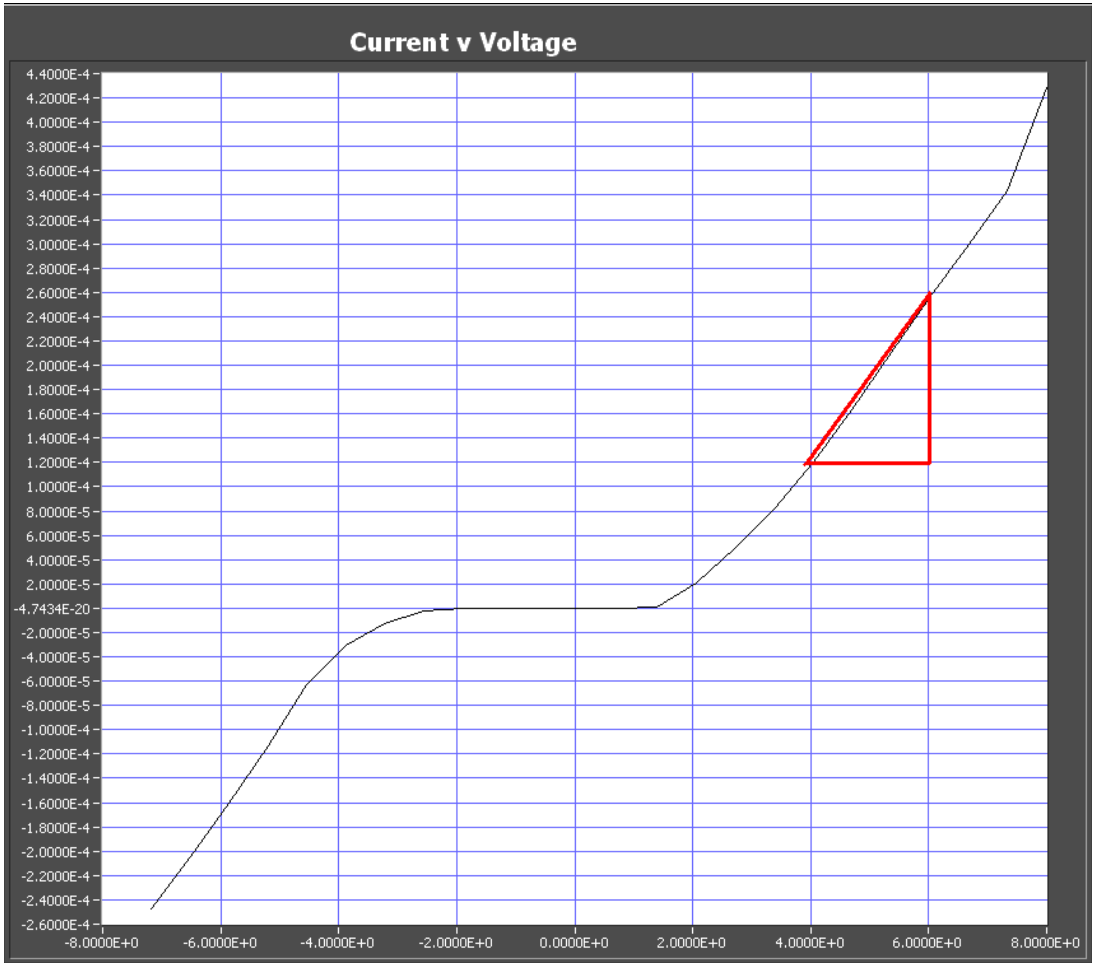
Figure 7: Example I-V curve taken from sample 2

‘ON’ voltage = -7.02 V

From the graph,

R = 12 K Ω

I-V curve for sample where the masks are NOT ALIGN



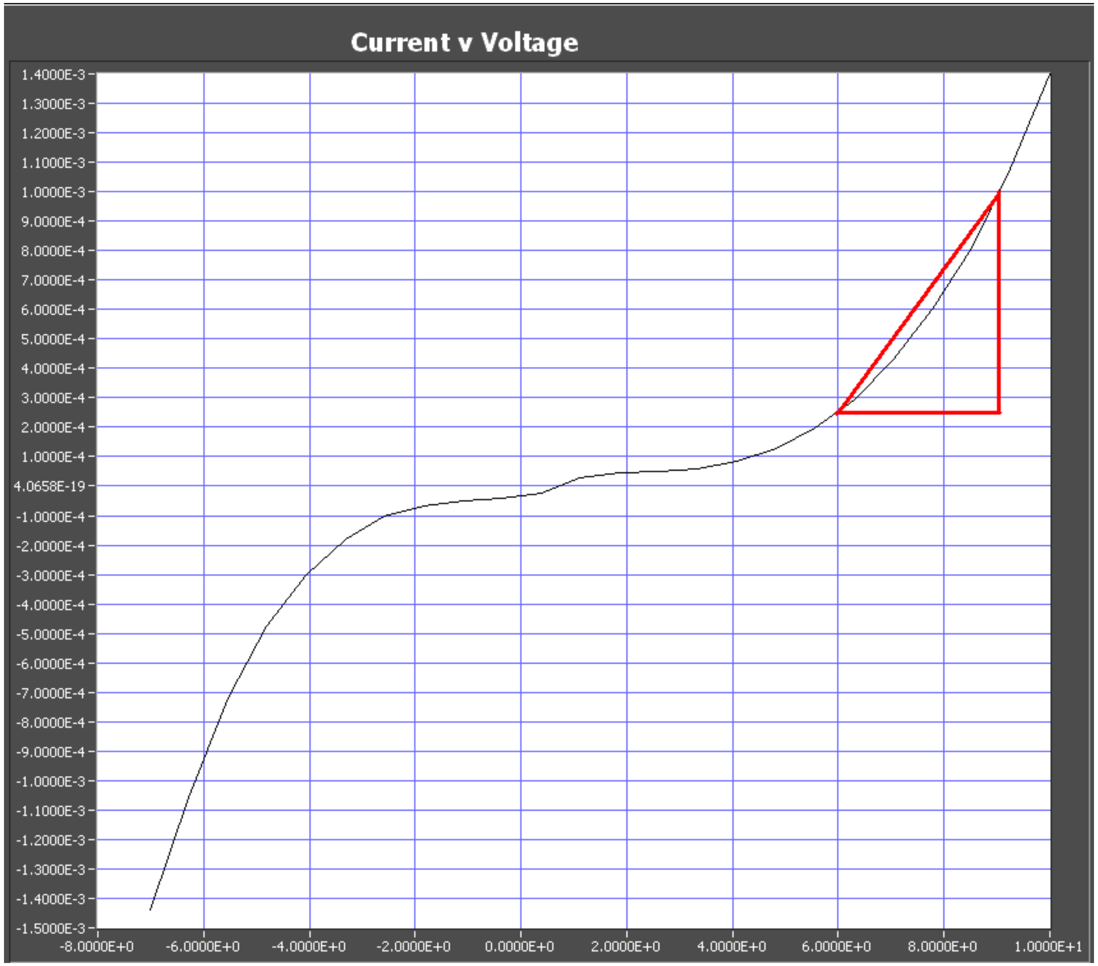
‘ON’ voltage = -7.18 V

From the graph,

R = 14.29 K Ω

Figure 8: Example I-V curve taken from sample 3

I-V curve for sample where the masks are NOT ALIGN



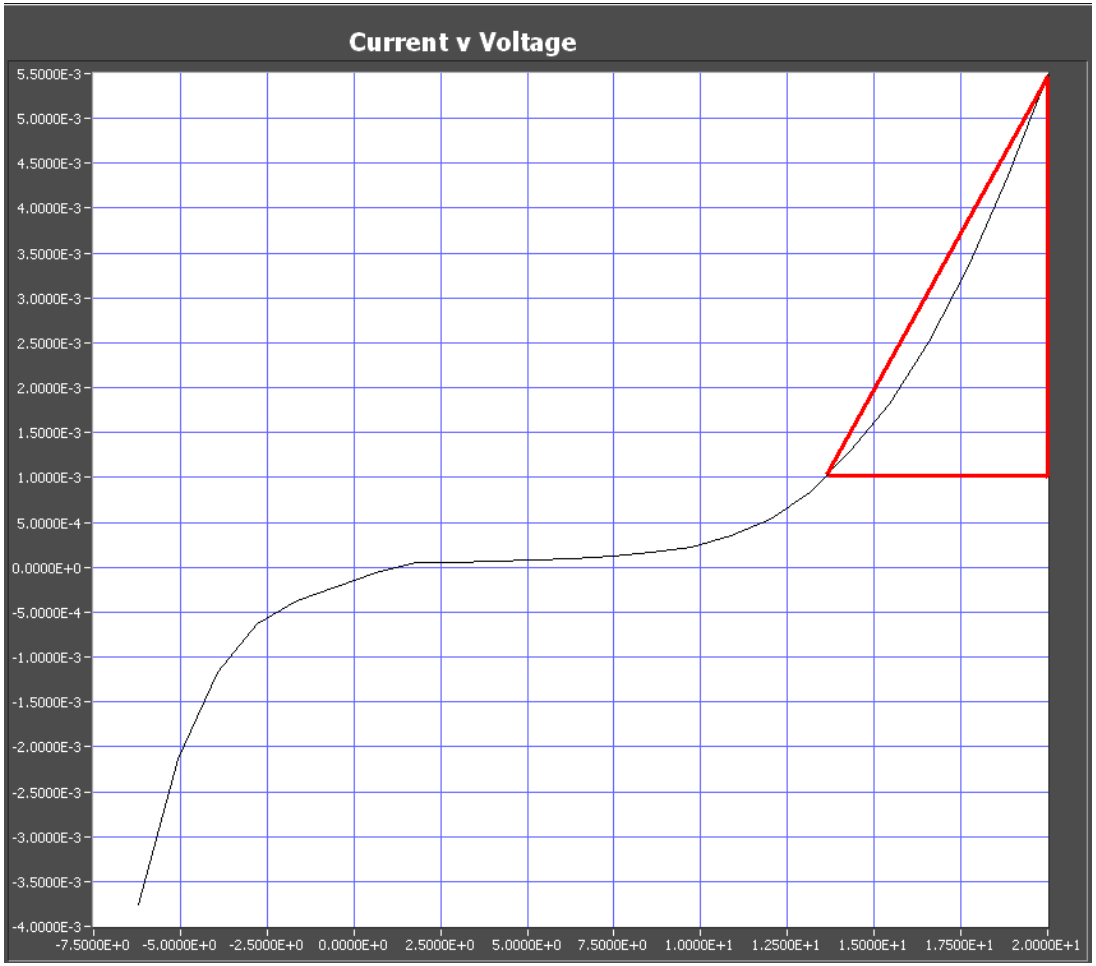
‘ON’ voltage = - 1.12V

From the graph,

R = 4 K Ω

Figure 9: Example I-V curve taken from sample 5

I-V curve for sample where the masks are ALIGN



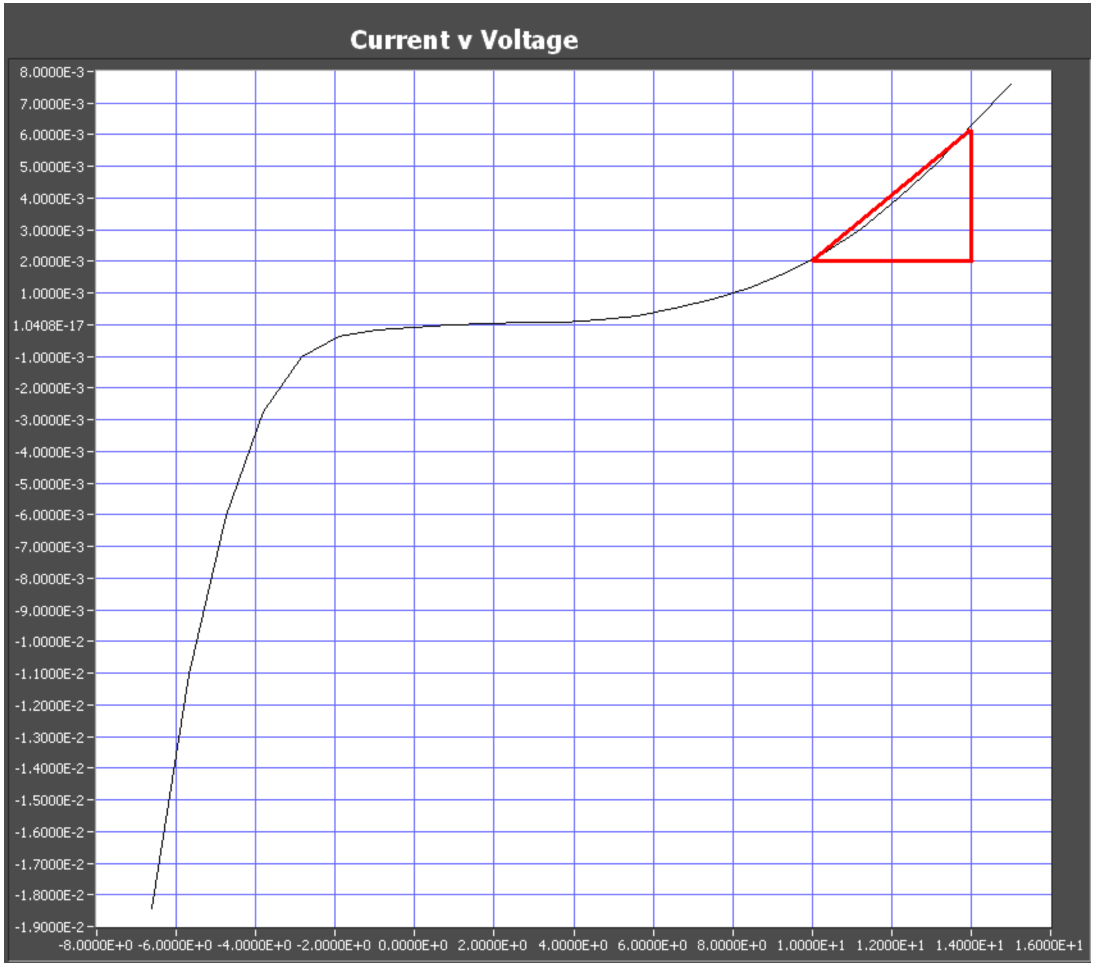
‘ON’ voltage = 6.32 V

From the graph,

R = 1.46 K Ω

Figure 10: Example I-V curve taken from sample 1

I-V curve for sample where the masks are ALIGN



‘ON’ voltage = 3.72 V

From the graph,

R = 1 K Ω

Figure 11: Example I-V curve taken from sample 4

Table 6: The value of ON voltage and Resistance of different sample

Sample	ON voltage (V)	Resistance (K Ω)
1(A)	6.32	1.46
2(NA)	-7.02	12.00
3(NA)	-7.18	14.29
4(A)	3.72	1.00
5(NA)	-1.12	4.00

*(A) = align
(NA)= not align

- From the I-V characterization, the percentage of acceptable device of each sample calculated.

Table 7: The percentage of acceptable device for different sample

Sample	Percentage of acceptable device (%)
1(A)	83.33
2(NA)	18.18
3(NA)	10.00
4(A)	92.67
5(NA)	25.00

*(A) = align
(NA)= not align

CONCLUSION

- Even though many devices are failed for the samples that fabricated using the unaligned masks, from figure 7-9, it also showed that some devices acceptable (graph of p-n junction diode obtained). But refer to table 7, it showed that all the samples have a very low percentage of acceptable device and prove that mask alignment is very important and surely will give negative effects to our devices.

- The most suitable mask of all the masks that have been created is design 4. From table 6, it showed that sample 4 (that used design 4) have the lowest value of resistance and ON voltage and referring table 7, it also showed that sample 4 have the highest percentage of acceptable device.

- From table 4 and figure 3, it showed that the dimension (length and width) of device on the mask design effect the doping process. Smaller dimension of device pattern on the mask design make the concentration of electrons that diffuse to the silicon substrate is lower. Table 5 and figure 4 prove that small dimension of device (sample 2 and 3) have a higher percentage of sheet resistance increased than bigger dimension of device (sample 4 and 5).

RECOMMENDATIONS

- This study should be done by a group of people so that the accuracy of the results is higher .
- More samples and more design should be used in order to gain more data so that more choices to determine the most suitable mask design.
- More accurate equipment should be used (instead of dropper), in order to determine the exact amount of the liquid dopant that should be applied on the wafer for doping process.

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THE END
THANK YOU…