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Recycle Folded Cascode OTA with Current Control Circuit

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Abstract: This paper presents an improved architecture of recycle folded cascade (RFC) OTA with current control circuit that achieves improved DC gain and settling time without sacrificing power and area. This is achieved by exploiting and using idle device in the signal path and separates the AC and DC path, which results in an enhanced transconductance, output resistance, gain, settling time and power dissipation. A recycle folded cascade amplifier architecture was implemented in 90 nm CMOS process with 1 V power supply. Simulation results shows that the proposed structure significantly increase the DC gain bandwidth compared to the recycle folded cascade OTA and consume very low power dissipation. Theoretical analysis and LTSpice simulations prove the performance of the new OTA.

Keywords: Operational transconductance amplifie; OTA; transconductance; settling time, DC gain.

1. Introduction

Operational Transconductance Amplifier (OTA) is one of the vital building blocks of analogue integrated circuits and it is widely used as compared to other topologies of operational amplifier because it provide a large voltage output swing and they are less susceptible to common mode noise. The most commonly used architectures is folded cascade amplifier for its high gain and large voltage swing. Moreover, the PMOS input of folded cascade has become the prime choice over its NMOS counterpart for its higher non-dominant poles, lower flicker noise, and input common mode level[1],[2],[3].4]. OTA must meet the following requirement for the best operation such as large bandwidth, high gain, high slew rate and low power. A several methods have been designed to enhance the performance of OTA without increasing power or area consumption. Recycling folded cascade structure which is proposed in [1] intends to use M12 and M10 as driving transistor by splitting it to conduct current mirror with fixed ratio. Another method was implementing AC and DC path separation in current mirror to enhance the gain of the OTA [2]. However, it shows degradation in phase margin due to the multiple path current mirrors. Multiple path scheme of current mirror [3] was also applied to the Three-Current-Mirror OTA to enhance the output impedance and slew rate but it is not suitable for high speed applications as the transfer function of the OTA had numerous low frequency pole-zero pairs. Switching circuit in [4] proposed to control the current of output stage and nonetheless [1-4] form the basis of the proposed modifications to the conventional folded cascade OTA. The paper is presented as follows; Section II explains the proposed architecture, whereas Section III and IV discuss the simulation results and conclusions.

2. Principle of Enhanced RFC OTA Topology

The operational transconductance amplifier (OTA) is an amplifier where all nodes are low impedance except the input and output nodes [5]. The conventional OTA in Fig.1 becomes popular choice because of its single pole characteristic and wide output voltage swings. Transistor M5 and M6 in Fig.1 draw the most current and it has the largest transconductance in many designs. However, their role is only limited to providing a folded node for the small signal current generated by the input driver (M3 and M4). The output resistance and transconductance of the conventional OTA is

$$R_O = g_{m12} r_{ds12} (r_{ds3} || r_{ds5}) || g_{m10} r_{ds10} r_{ds8} \quad (1)$$

$$Gm_o = g_{m4} \quad (2)$$

The very common method to enhance the gain is by increasing the output resistance at the output stage by cascading the transistor but in turn suppressing the voltage swing. Without reducing the voltage swing or increasing current and power consumption, M5 and M6 can be exploiting to shifting the gain to the desired level.

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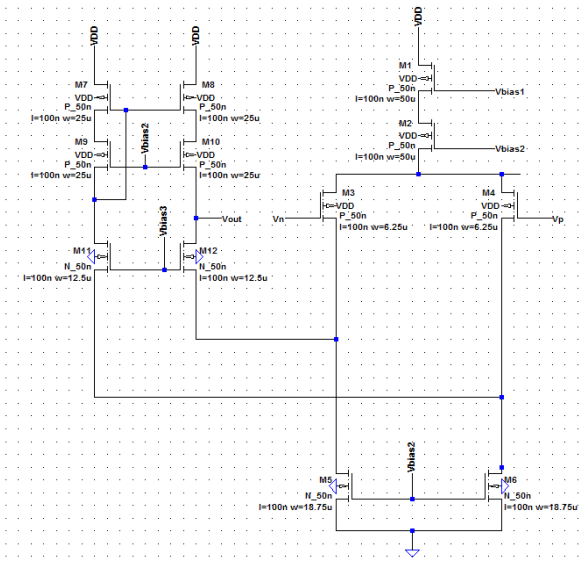


Figure 1.Conventional OTA

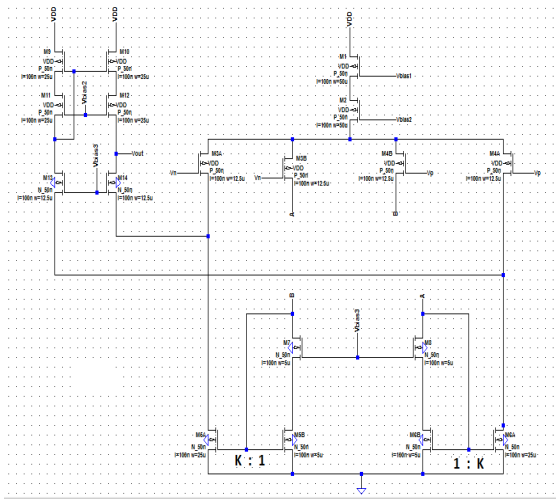


Figure 2.Recycling Folded Cascode OTA [1]

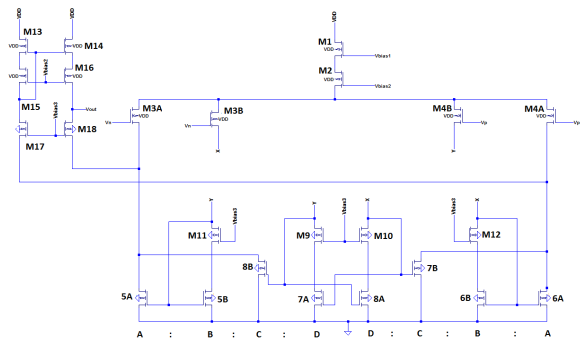


Figure 3.Recycling Folded Cascode with current control circuit

Fig.2 shows recycling folded cascade structure which is proposed in [1]. The input pair is split into half (M3A, M3B, M4A, M4B) while ratio of current mirror (M5A:M5B and M6B:M6A) is set to three to maintain the correct summation of DC currents without increasing biasing current and power consumption. In this work, AC and DC current is sharing the same path, so the transconductance in this circuit is limited by DC currents[2]. The gain enhancement is attributed to the increased r_{ds} of M3A and M5A as they conduct less current compared to their counterparts M3 and M5 in Fig.1.

The proposed structure as shown in Fig.3 is a modification to folded recycling structure in Fig.2 [1] and [2] by adding the current control circuitry (M7A, M7B, M8A, M8B, M9, and M10) to reduce the quiescent current at the M3A. Control circuit introduced in [4] form the basis of this work which during the quiescent condition transistor M7B and M8B act as voltage control current sources where a significant amount of the drain current M3A now flows into the current source M7B as well reducing the output current. Transistor M9, M10, M7A and M8A sense the input differential voltage and control two voltage controlled current sources, M7B and M8B. If the current through M3A increases by $g_{m3A} \times (V_{in}/2)$, the current through M8B decreases by $g_{m11} \times V_{in}/2 \times C/D$, where $V_{in} = V_p - V_n$. The total amount of current increase in M5A is equal to the amount of power change in M8B. Therefore the total current change in M5A is the sum of the changes in M3A and M8B. DC currents flow through transistor M5A, M5B, M7A, M6A, M6B and M8A while almost no AC current flows through M7A, M8, M9 and M10 because they have high impedance for AC signal. The expression for the new output resistance transconductance for the proposed architecture is represented in (3) and (4) respectively.

$$Gm_{new} = \frac{B+C}{B+C+D} \times g_{m,in} \times (A+B) + \frac{D}{B+C+D} \times g_{m,in} \times \frac{C}{D} \times (A+B) \quad (3)$$

$$R_{O,new} = g_{m18} r_{ds18} \left(R_{out3A,5A}\right) || g_{m16} r_{ds16} r_{ds14} \quad (4)$$

Where the transconductance $g_{m,in}$ is the total input transconductance $g_{m3A,3B} + g_{m4A,4B}$ which equals the input transconductance $g_{m\,3,4}$ in (2). The current at transistor M5A is reduced by the existence of control circuit M8B and as the result, the output resistance is increased as

$$R_{out3A,5A} = r_{o3A} || r_{o5A} = \frac{2}{(\lambda_{3A}+\lambda_{5A})} \times \frac{B+C+D}{A} \quad (5)$$

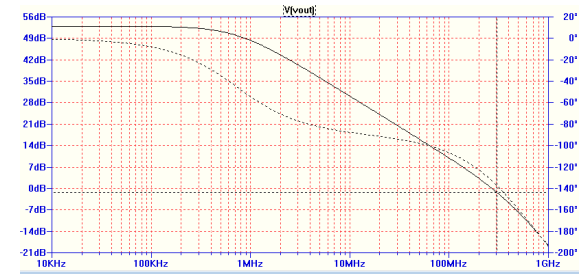
Examining (3) and (5), since both output transconductance and resistance is increased, the overall DC gain increase in the proposed architecture is significant increased as (6)

$$A_V = Gm_{new} \times R_{o,new} \quad (6)$$

3. Experimental Results and Discussion

In order to investigate the feasibility of the enhancement technique discussed above, the simulated open loop performance of the proposed architecture is compared to the performance of recycle folded cascade architecture[1]. Both circuit was designed with the same length 100 nm and widths are decided to have overdrive voltage about 200 mV. In order keep the DC current unchanged , the ratio of transistors are as follows; the value of A, B, C and D in the proposed architecture are 4,1,8 and 1, respectively .

The circuit has been simulated using LTSpice and BSIM MOS transistor models (level 54) with well 50nm CMOS process. Both folded recycle OTA and proposed OTA are designed to have same 100µA tail current and power supply 1 V. Fig.4 shows that the DC gain is improved by approximately 5dB, however the phase margin of the proposed architecture is slightly lower compared to RFC. This is due to the increased capacitance at the cascade nodes, increasing pole and zero. The dc gain of the new OTA is significantly increased from 52 to 59 dB. The unity gain frequency of the RFC is 260 MHz with 48^0 phase margin, while new OTA has 230 MHz with 40^0 phase margin. The effect of non dominant poles decrease the phase margin of the new OTA, but it still a sufficient phase margin is achieved. Step response of the new OTA is shown in Fig.4 to confirm the stable operation of the circuit. Simulation results show there is a slight overshoot due to 40^o of phase margin.



AC Analysis RFC [1]

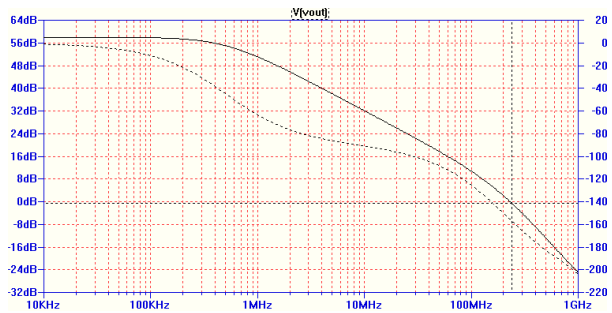


Figure 4. AC Analysis proposed OTA

Fig.5 shows the frequency responses of both RFC and proposed OTA with 5 pF load capacitor respectively.

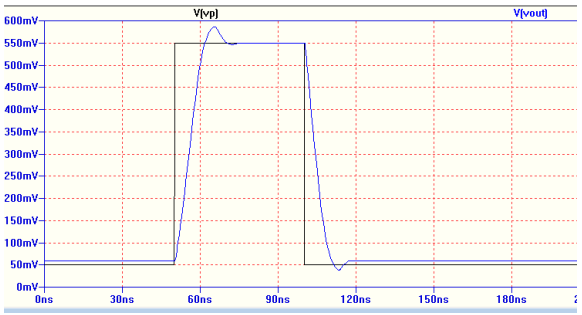


Figure 5 :Step response

The large signal transfer characteristic of the OTA for unloaded output is shown in Fig.6 and the voltage swing is relatively wide.

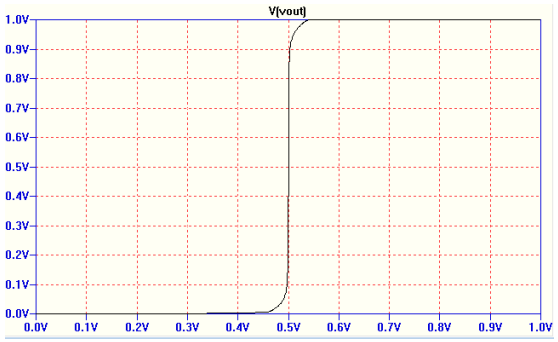


Figure 6. Voltage Swing

The simulation results is shown in Table 1 comparing the performance of recycle folded OTA with proposed architecture.

Table 1

Proposed OTA		**Conventional OTA (RFC) [1]**	
DC Gain	57.9565 dB	DC Gain	52.9649 dB
UGBW	231.7 MHz	UGBW	260.435 MHz
Phase Margin	40^0	Phase Margin	48^0
Transconductance ,G_m	2.52 µA/V	Transconductance ,G_m	1 µA/V
Capacitive Load	5pF	Capacitive Load	5pF
1 % Settling Time	9.6854 nS	1 % Settling Time	11.2848 nS
Bias Current	100uA	Bias Current	100uA
Power Dissipation	220µW	Power Dissipation	280 µW

4. Conclusion

An improved architecture of recycling folded cascade OTA is proposed to enhance the output resistance of the OTA without increasing power or area consumption by adding the current control circuit . Simulation shows that the proposed architecture has a 5 dB improvement compared to the RFC architecture and also there is an improvement in transconductance parameter. The proposed OTA consumed slightly less power dissipation about 220 µW compared to the RFC.

References

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