Design And Analysis of Building Evacuation System's Controller Using FPGA

Nurul Fatihah Jusoh, Sukreen Hana Herman and Suhana Sulaiman

***Abstract*— This work is focused on the hardware support for improving an emergency evacuation known as decision support system, "*op_sys*". The Controller Operating System Unit is a module in *"op_sys"* that is designed to improve occupants' information if there is an emergency situation such as fires is occured. This module is handled through Controller Alarm and Controller System Floor, by displaying the data output through FPGA board on three varieties of manually selected modes at FPGA board. Also, the Controller System Floor is tested for simulation waveform using Modelsim Altera EDA application software. The compilation for hardware verification functionality, simulation waveform functionality, and timing analysis show the results is consistent and met the specification requirement with the theoretical analysis. Furthermore, the estimated of four alarm sensors and controller system floor is required if the system is implemented for the future work.**

***Index Terms*— controller, evacuation, emergency, FPGA board.**

I. INTRODUCTION

High-rise building is a tall building or structures that are used as a residential, office or institutional building, and shopping complex building. In the United States, the National Fire Protection defined a high-rise as being higher than 75 feet (23 meters), or about 7 stories [1-2]. Building code of Hyderabad, India and Emporis Standards (Real State Information Industry in Germany), stated that a high-rise building is one with four floors or more, or being equal or higher than 15 meters in height [3], and as a multi-story structure between 35-100 meters tall, or a building of unknown height from 12-39 floors [4], respectively.

In Malaysia, the procedures regarding fire emergency is a legal requirements stated in Uniform Building By-Law 1984. The procedures has to be approved and recognized with the standard international building regulations (by-laws) fire's requirement system regulated from the Fire and Rescue Department of Malaysia, (FRDM).

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The fire's requirement system is classified for fire precaution in air-conditioning system, fire mode of operation, fire resistances and structural member, test of fire resistances, emergency exit signs, sprinkler valves and voice communication system. Another certification is Certificate of Completion and Compliance (CCC). This certificate is meant for the builders, Professionals Architects, Professionals Engineer, and Registered Draughtsman building of any type of building construction to obtain the approval that is authorized from the local authority and the "*Lembaga Arkitek Malaysia*". This approval is an endorsement to certify that the building or the accommodation were qualified or fit and safe for the occupants. This certification is under By-Law 25A [5] and as a credential for inhabits and living in the building before the building owners handed it over to the buyer.

National Fire Protection Association (NFPA) is a global non-profit organization establish in 1896 at United State, U.S and devoted to eliminating death, injury, property and economic loss due to fire, electrical, and related hazards [6]. Based on NFPA in 2007-2011, an estimated 15,400 reported (an estimated 3%) high-rise structure was on fire per year resulted in associated losses of 46 civilian deaths, 530 civilian injuries, and $219 million in direct property damage per year [1].

In Malaysia, as reported in between year 2012 and 2013, FDRM has noticed an increment pattern of fire incident with 371 cases. These results has shown that there is demand for high-rise building building evacuation strategies during an emergency situation such as fire safety planning [7] to be investigated. The question is prompted; how sufficient the present evacuation plan for high rise building, what is an emergency procedures should be employed or implemented to improve the evacuation efficiency? [8].

Some works have been researched in order to improve the effectiveness of evacuation plan for occupants and evacuees in minimizing the time to find and get an access to the safe place in an emergency situation. The issue arises due to the evacuation model system capabilities did not provide up-to-date information with the exact data information location (room and floor) when the fire occurred in the building. Hence, due to lack of knowledge or exact information (information of exact data location which room and floor), it may cause some occupants and evacuees encounter the situation of panic, chaotic, and also may root the evacuees to reach near the location of fire, traffics, trapped, and increase total injured and death among evacuees.

In this paper, an evacuation system architecture for multi-storey building to provide accurate information (i.e. room and level of floor) during an emergency situation is implemented. The system model is focusing on the Controller Operating System Unit. The main modules in *"op_sys"* is targeted to fulfill and improve the demand of the safety building evacuation system. Hence, by designing the Controller Alarm and Controller System Floor modules in *"op_sys"*, it can improve occupants' information if an emergency situation such as fires occurs. Moreover, the system is expected to minimize evacuation time, traffic, and panic among the evacuees or occupants to find and reach a safe path. In Section II, some works on the warning system is discussed. Section III discusses the framework of the controller operating system unit using FPGA. The design and methodology is described in Section IV. Section V and VI are the result and discussion and conclusion of this work repectively.

II. Previous work

Several works on the hardware support for evacuation plan developed by other researchers are mainly focused on the warning of the emergency evacuation for high-rise building on improving the evacuation plan.

Work by C. Y. Lin *et. al* [9] proposed a system called Active Emergency Disaster system (AEDS) that automatically control the device to correspond on natural disasters such as earthquake situation. The AEDS provides the information on family member position automatically as well as for relief operation unit to take action during the disasters. The system used a common Alerting Protocol, (CAP) for giving warning message and Tibbo EM1000TEV and passed to XML files to extract the information through internet. GA 1000 Wifi Module Kit Board is used to communicate and receive CAP warning messages. Also, the system only provides information such as sender, date, and response time if disaster occurs [9].

Q. Sun *et. al* works are related to emergency evacuation information system based on the internet of things [10]. However, the ideas were on the status of emergency evacuation management with the implementation strategy of information system. In their work, the emergency evacuation system was designed whereby the system is divided into basic platform and data module. Basic platform consists of sensor network, transmission network and application network composition that can be used for government places to public [10]. The data module consists of underlying database, specialized database and emergency database.

Research by R. A. Kosiński, A. Grabowski and J. Teekul, S. Sinthupinyo respectively [11, 12] mainly focused on the numerical simulation formula. The result of an experiment during drill evacuation from a building were taken using intelligent agents system. The work only concentrated for the simulation of the evacuation period time during analysis data from active counter and image recorded. The analysis data is the real event of the pedestrian flow process and reused the building block that have similar property in-term of block model, respectively. These dynamic activities were described using equation of motion where the numerical simulation was performed for different buildings, including multistorey buildings. Also, other type of mathematical models of pedestrian motion in hazardous situations is based on the application of 2-dimensional probabilistic automata, in which the spatial distribution of cells correspond to the internal geometry of rooms in a building and the transition rules define the shift of a pedestrian to neighboring cells. Hence, these models enable to observe collective dynamic phenomena in pedestrian motion.

Based on the discussed work, the FPGA was not utilize due to the fact that the work was set to comprehend the evacuation plan and warning for high-rise building and natural disaster. Thus, this work presents several reasons why the decision support system is implemented and employed using FPGA with wireless communication. This is because wireless communication and microelectronic allow the system to be built smaller [13, 14], the system itself is low cost in power consumptions [13-15], and the system is battery powered with smart sensing device [13-14, 16] with on board processing and communication capabilities [13]. Other few advantages are due to the fact the system can be made with multitude of sensor connected by wireless communication system or internet connection. Furthermore, the system can offer some prospects or monitoring system application [13,15] and safety management application [13,15] especially for housing [15-17], town [34], high-rise building, and the environment [15,18].

For that reason, several works using hardware support for evacuation plan has been developed by other researches such as A. Hayek *et. al* [20] and U. Quadri *et. al* [19]. Work by A. Hayek *et. al*, is a prototyping platform employing FPGA for safety related communication system utilizing a wireless sensor network [20]. The system implemented Ioo2 architecture into a single FPGA (XILINX Spartan 3 family) based on IEC61508 for wireless sensor application with 2 fully synchronized 8bits microprocessor integrated which control by an on-chip diagnosis unit. The author [20] also used two Triaxial acceleration sensor beside FPGA in order to achieve redundancy at sensor level. The sensor BMA180 from Bosch was used to achieve high performance digital triaxial acceleration sensor. Moreover, graphical user interface, GUI is used in order to provide the user with the available sensor data. The communication system set up utilized the OEM Wireless LAN module (UART) for serial LAN adapter 311 (OWSPA311G) from connectBlue (presented as serial port UART to the host) using HDL language to configure the behaviors of FPGAs with wireless LAN (IEEE 802.11 a/b/g/n) thru TCP/IP connection. In this work, A. Hayek *et. al* argued and claimed that FPGAs can at least be used as a basic platform for several communication application in safety related field [20].

U. Quadri *et. al* work is related to the implementation of FPGA-based digital logic emulator (for safety) [19]. The system is capable for implementing Boolean functions which form a platform for the design of higher combinational and sequential logic circuit. The system techniques employ 3-wire Resistance Temperature Detector (RTD), Pt100 as a platinum temperature sensor whose metallic resistances changes with respect to temperature and ATmega8L-Atmel AVR in 8-bits microcontroller for ADC devices board as function for the conversion of analog to digital converter [19]. The 8-bits data

from microcontroller is then connected to the transmitter of the node. The communication system technique utilized the CRC block as function to encrypt data and transmit data to the receiver. The transmitter will begin with the data transmission only after there is reception of signal from the receiver [19]. This emulator system consists of digital logic block and their operations were performed using appropriate 4 bit number named equation. Each equation was represented with a fixed logical operation and the output was represented as a result of the block [19]. The work has been tested with compilation, RTL viewer, and simulation waveform verification using 13.1.ISE Simulator. The FPGA-based reprogrammable prototyping board and the result showed that the system is capable and compatible in the implementation of circuit and hardware verification. Also, the system proved to be power efficient by making use of power getting mechanism and task oriented control signal [19]. A. Hayek *et. al* [21] also implemented and employed an FPGA-based wireless smart sensor network to integrate the acceleration sensor for increasing the safety aspect in cognitive system used for industrial communication. Wireless sensor network (WSN) is compatible with FPGA device. It has the ability for monitoring and steering industrial system and has emerged as an important new implementation in a new wireless embedded technology in safety related system [21]. Furthermore, several hardware platforms can be targeted for the integration of the acceleration sensor due to the flexibility and configurability along with high performance, power efficiency. By having FPGA-based wireless smart sensor network, it can be another platform to realize such intelligent sensor network that can also integrate embedded processor and on chip memory into a single die and easily configured to interface with a wide variety of popular communication protocol i.e. SPI, UART, and I2C.

To summarize, FPGAs is feasible to be used for the implementation of simple interface circuit or complex state machine to satisfy a different system requirement. Besides, it can improve the system integration [22], reliability [22], performance for low cost [22] and reduce power consumptions [22-24]. It also contains a programmable logic components as known as 'logic block' and wired together in a special hierarchy of configurable interconnect.

Hence, the motivation of this study is to implement an evacuation system architecture for multi-storey building known as decision support system through FPGA EP2C35F672C6 Altera Family device with feasibility proficient and capable in providing accurate information (*i.e.* room and level of floor) by using wireless communication system to occupants and evacuees during an emergency situation. However, the system model for this work was focused on the Controller Operating System Unit. This modules in *"op_sys"* is targeted to fulfill and improve the demand of the safety building evacuation system. Hence, by designing the Controller Alarm and Controller System Floor modules in *"op_sys"*, it can improve occupants' information if an emergency situation such as fires occurs. In addition, the system is expected to minimize evacuation time, traffic, and panic among the evacuees or occupants to find and reach a safe path.

III. FRAMEWORK OF THE CONTROLLER OPERATING SYSTEM UNIT USING FPGA

The controller operating system unit consists of three different controllers: controller selected modes, controller system floor and controller alarm as shown in Figure 1. The controller selected modes is manually controlled and interface with Altera DE2 to synchronize with the alarm device. There are two modes for controller selected modes which are assigned for *"selector button"* and *"message_7segment"*. LED & LED7SEG unit is the setup for the interconnection to display the output data from the controller selected modes. Its role is for the hardware functionality of the *"selector button"* and *"message_7segment"*. There are 2 types of mode: Mode Type 1 and Mode Type 2. Mode Type 1 represents the blinking and sounds for the speaker on the Altera DE2 Family Board whereas Mode Type 2 is designed to display *"FirE-OCCUrS"* on the LED7SEG. The controller system floor is for the assignment of the floor level and controller alarm is assigned for the alarm signal in two different floor levels.

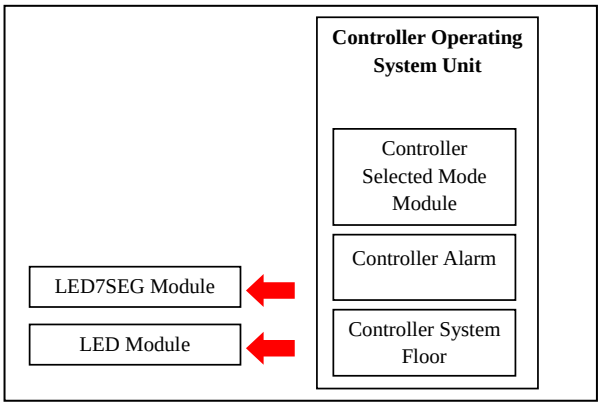


Figure 1: Block Diagram of Decision Support System using FPGA

Figure 2 illustrates the building evacuation system based on decision support system, "*op_sys*". As shown in Figure 2, the specification is targeted for educational occupancies with building specification construction building of central air conditioning for two or more "*storey*" and within a gross floor area 500sq.m till 1000sq.m. The wireless smoke detector alarm was recommended to be installed in every room or office in the future work. This is because if the fires occured, the smoke detector will trigger and controller alarm and controller system floor will send the signal to the LED & LED7SEG and send the signal through the communication unit.

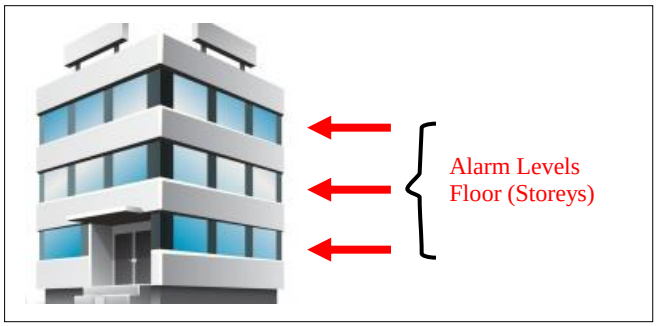


Figure 2: Illustration of building evacuation system to indicate the alarm level floors for Decision Support System.

IV. DESIGN METHODOLOGY

The Controller Selected Mode Module, is designed for three type's categories modes "*Selector_button*" sub-module in transmitting output data based on the manually selected by the user at FPGA board. The Controller Alarm Module is responsible in analyzing, and recognizing receiving input signal based from the transmitting information data of alarm signal either from alarm 1, alarm 2, alarm 3, or alarm 4 were detected on fires and displays data output through FPGA board. Two different sub-modules were designed namely, selector input for first floor, "*selector_input_f1*" sub-module and selector input for second floor, "*selector_input_f2*" sub-module respectively. These sub-modules were referred to be placed in two different floor levels as suggested in this work. Another sub-module is "*controller_floor*" that is responsible to recognize the level of floor in the building either for alarm 1 and alarm 2 or from alarm 3 and alarm 4 for floor 1 or floor 2, respectively.

A. Controller Selected Mode Module

Figure 3 depicts the flow chart for the controller operating system unit for "*Selector_button*" sub-module. The "*Selector_button*" will arrange and transfer the signal according to specific input data in three modes known as selected controller modes sub-modules i.e. "*mode_1*", "*DATA_TX_SUB*", and "*music2*" for Mode 1, Mode 2, and Mode 3, respectively. If "*RST*" input data is at logic '*1`b1'*, all the temporary registers "*state*", "*mode_1*", "*mode_2*", "*mode_3*", and "*display*" will be cleared into '*1`b0'* bit logic. The receiver input data of 4-bits widths input data port, "*button1*" is connected to switch port FPGA device with the fixed value parameter that will responds to four different variable declarations to produce an output data. There are four fixed variable declaration parameter is '*0*', '*5*', '*12*' and '*15*' that will produce an output data for "display", "*mode_1*", "*mode_2*", and "*mode_3*", respectively.

The three variable data from the output port will be transmitted to the other sub-modules for the next processing modes i.e. "*mode1*", "*DATA_TX_SUB*", "*music2*" sub-modules and another one data output to be transmitted to the sub-modules, "*message_7segment*" that is responsibility to display character output through 7-segment port at FPGA device.

B. Controller Alarm And Controller System Floor

Figure 4 and 5 show the flow chart of "*selector_input_f1*" sub-module for first floor controller alarm and Flow "*selector_input_f2*" sub-module for second floor controller alarm respectively. Both operations will analyze the data input signal to the running operation depending on the received data at input port "*sw*". The input port "*sw*" will receive input bit data from the manually selected mode from user at the switch port FPGA device.

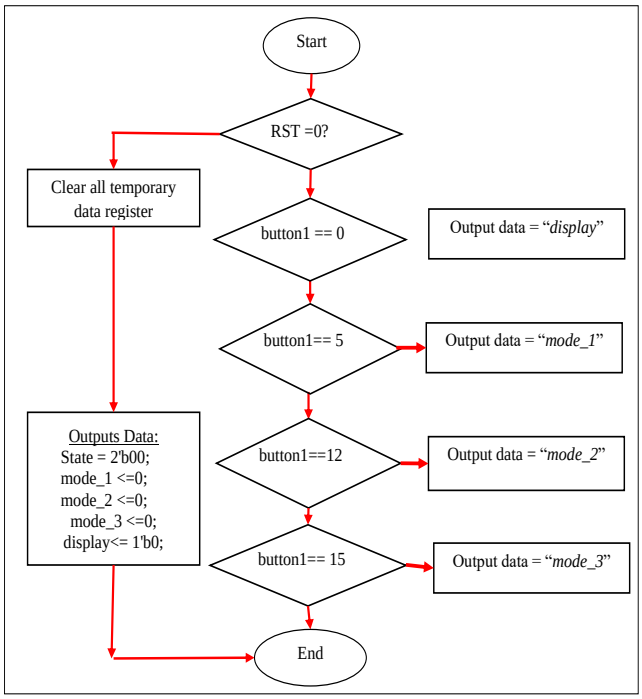


Figure 3: Flow chart for the controller operating system unit for "*Selector_button*" sub-module.

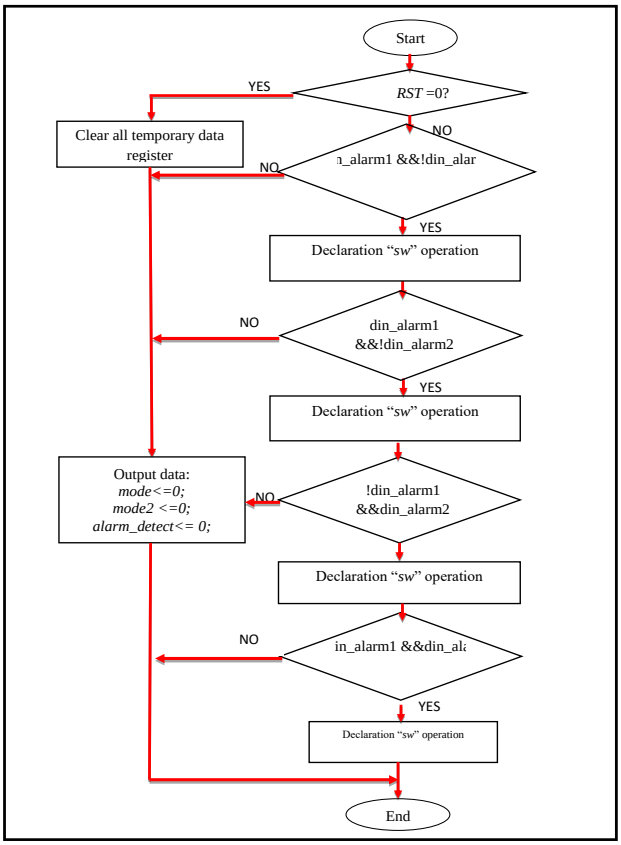


Figure 4: Flow Chart of "*selector_input_f1*" sub-module for first floor controller alarm

The Controller System Floor on the other hand, has two different sub-modules declared as "*selector_alarm*" and "*controller _floor*" sub-modules. The "*selector_alarm*" is designed to receive output data from "*selector_input_f1*" and "*selector_input_f2*" respectively. The output will produce 4-bits data output : "*alarm_LED*", and 1-bit data for each, "*detect_A1*", "*detect_A2*", "*detect_A3*", and "*detect_A4*" at a different assign pin planner location for LED ports at FPGA device. This is to illustrate how the evacuees and occupants to identify the exact location of the fire alarm sensor device with its room or office which is on fire.

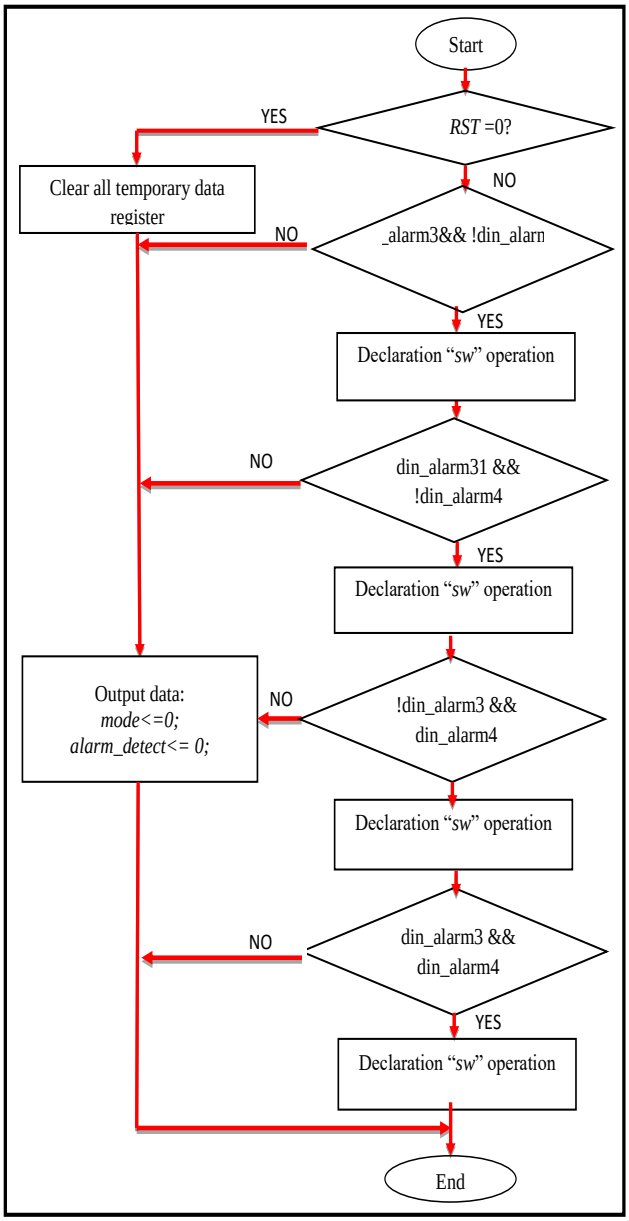
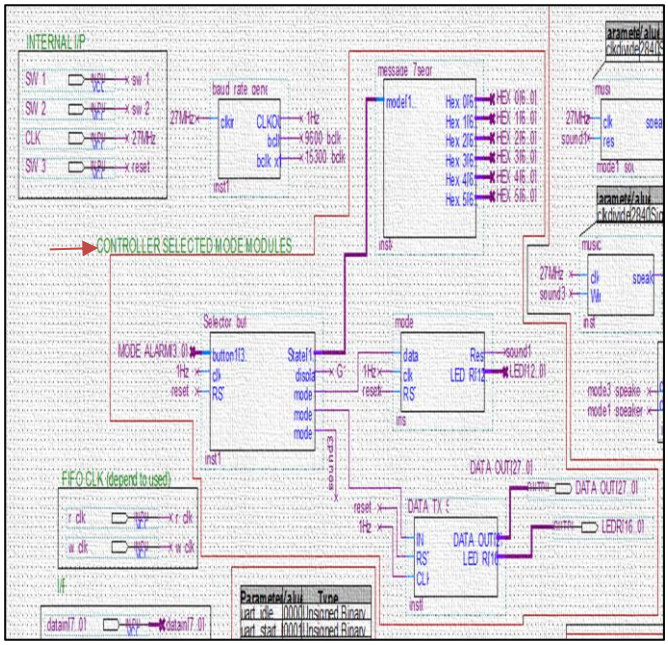


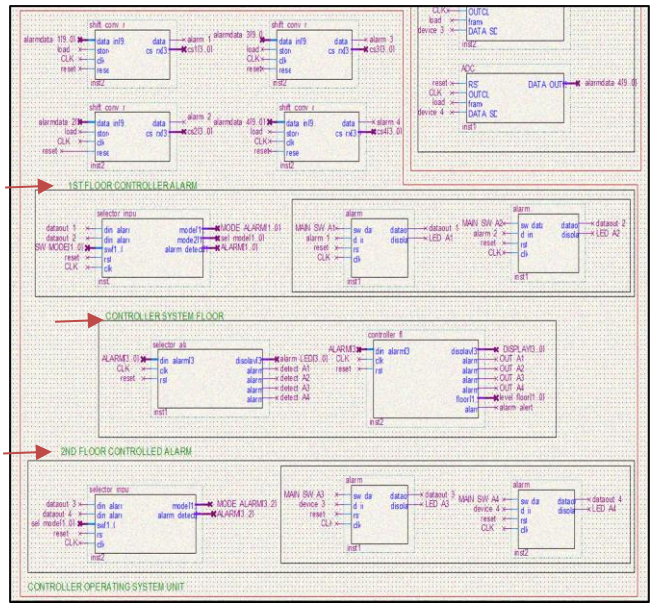
Figure5 : Flow Chart of "*selector_input_f2*" Sub-Module for Second Floor Controller Alarm

V. RESULT AND DISUSSION

Figures 6 (a) and (b) depicts the Controller Operating System Unit which comprises of symbol logic for Controller Selected Mode Module and Controller Alarm And Controller System Floor respectively (indicated by red arrow).



(a) Controller Selected Mode Module



(b) Controller Alarm And Controller System Floor

Figure 6: Controller Operating System Unit

The output for the controller selector Mode modules were exhibited with the hardware board to check the functionality of the design and manually controlled.
Figure 7 exhibits the result of Altera Board for "*Selector_button*" and "*Message_7segment*" sub-modules, respectively.

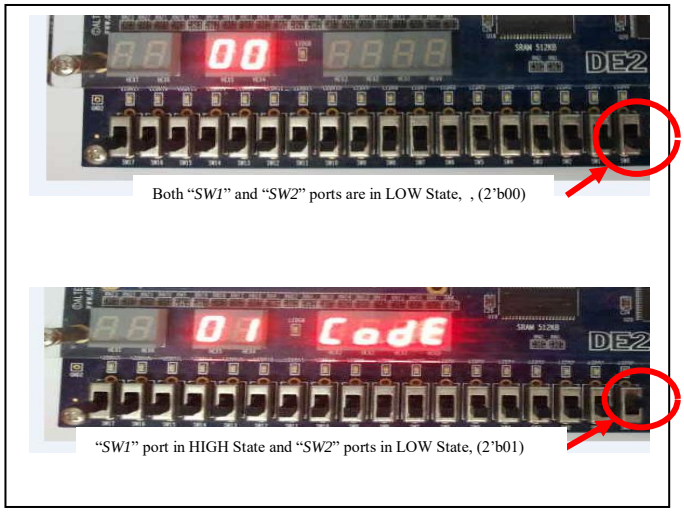


Figure 7: "*Selector_button*" and "*Message_7segment*" sub-modules, respectively.

To illustrate the indication of the fire is occurred and warning; two types of mode were designed namely Mode Type 1 and Mode Type 2. The purpose of these modes is to present the functionality of the alarm. The "*mode1*" module provides warning situation in term of applying a blinking mode pattern by assigning 13 red LED ports and sound speaker for sound 1 on Altera DE2 Family Board. The signal "*data_1*" and "*CLK*" are assigned to the interconnections output signal from "*Selector_input*" sub-module and at *"27MHz",n* conservative clock, respectively.

Figure 8 shows the result for data output at 1 Hz clock cycle to display slower pattern of blinking mode at 13 "LEDR" outputs ports modes in order to act upon the warning situations.

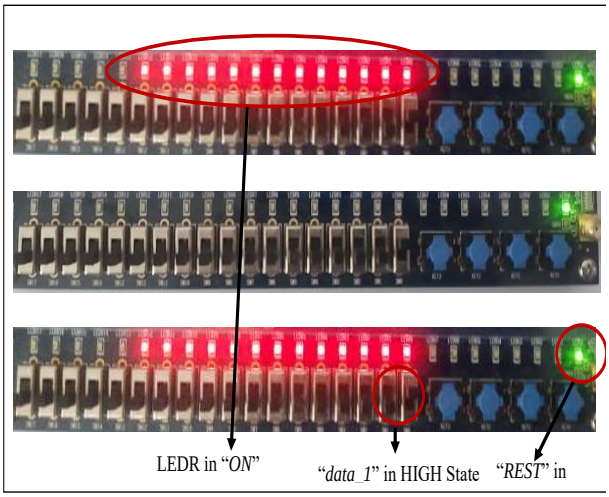


Figure 8: The blinking mode at 13 "LEDR" outputs ports

The illustration of the data character to display "*FirE-OCCUrS*" on LED7SEG is completed based on the limited graphic pattern encoded into the DE2 Family ALTERA. This is to show a simple word of expression and to alert the user. The word *FirE-OCCUrS* was shifted from right to the left and looping synchronously with the 17-bits data of *LEDR* at 1Hz, *n* clock cycle. This specification and architecture of the Mode Type 2 was created in "*DATA_TX_SUB*" sub-module.

Figure 9 exhibits the inputs ports "*IN*" and "*RST*" have been assigned into switching port of pin locations at *SW0* and *SW1*, respectively with the character data of display on LED7SEG "*FirE-OCCUrS*". The character data of display on LED7SEG "*FirE-OCCUrS*" is chosen based on the limited graphic pattern of characters on 7 segments to encoded into the DE2 Family ALTERA. The graphic is shifting from right to the left mode and looping synchronously with the 17-bits data of LEDR shifting with the same pattern at 1Hz, *n* conservative clock cycle. The sub-module "*divider1*" is designed as a converter to convert 27 MHz to 1 Hz, *n* clock cycle. The output clock from *"divider1"* sub-module is connected directly to the sub-module "*DATA_TX_SUB*" at "*CLK*" input port in order to produce an output signal progressively in RTL Reviewer Result. The word "*FirE-OCCUrS"* is used to express some attentions warning to the user.

A. Waveform Simulation For Controller System Floor

The Controller alarm was assigned with two inputs namely selector input first floor, *"selector_input_f1"* and selector input second floor, *"selector_input_f2"* in order to assign an alarm that was allocated in two different floor level. On the other hand, the controller system floor was appointed for the input as controller level floor, *"controller_floor"* for the assigned floor level. These sub-modules decision support system was tested and simulated to detect the assigned alarm.

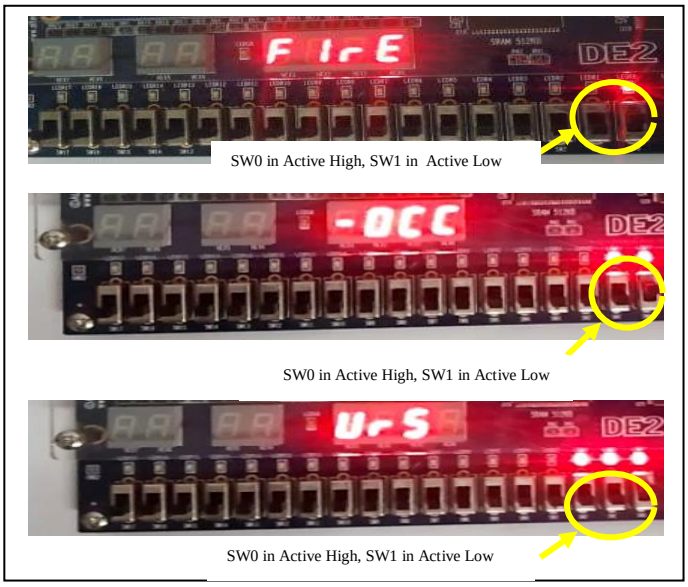


Figure 9 : Data character to display "*FirE-OCCUrS*" on LED7SEG

As shown in Figure 10, *"selector_input_f1_testbench"*RTL waveform for sub-modules *"selector_input_f1"*is presented. The *"selector_input_f1_testbench"* was simulated for timing interval between '0 ps - 1300 ps' where the input reset, *"rst"* is forced to "0". the "din_alarm1" and "din_alarm2" are assigned to '1' and '0', respectively with the interval time of "100ps-500ps". The input *"sw[1..0]"* was assigned with continuous 1-bit from 2`b00 till 2`b11 and repeated for every '100ps' interval. As a result, the output waveform produces an output bit for"mode[1..0]", *"mode2[1..0]",* and *"alarm_detect[1..0]"* based upon the receiving data of *"din_alarm1", "din_alarm2", "sw[1..0]",*and *"rst",* respectively. This simulation test-bench was implying that if the smoke was detected, *"alarm_detect"*

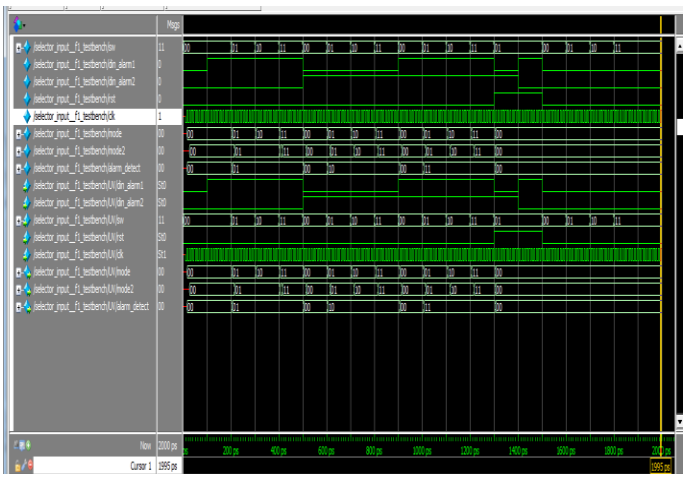


Figure10: Output waveform for *"selector_input_f1_testbench"*

Figure 11 exhibits *"selector_input_f2_testbench"* RTL waveform for sub-modules *"selector_input_f2".* At time interval of '0ps- 1300ps', the input reset *"rst"* is assigned to active-low while *"din_alarm3",* and *"din_alarm4"* are assigned to '1' and '0' for "100ps- 500ps" and '0' and '1' for '501ps-900ps' respectively. Input *"sw[1..0]"* was assigned for continuous 1bit from 2'b00 till 2'b11 and repeated for '100ps' time interval. Thus, the output waveform will produce an output bit for *"mode[1..0]"* and *"alarm_detect[1..0]"* upon receiving the data of *"din_alarm3", "din_alarm4", "sw[1..0]",*and *"rst",* respectively. This simulation is implying that if the smoke is detected, *"alarm_detect"* will declare an output when receiving the data from either *"din_alarm3"* or *"din_alarm4"* based on the triggered data from *"alarm3"* and *"alarm4"* sub-module, respectively. In this simulation, the receiving data from alarm 3 and alarm 4 is employed for the alarm in second floor of a building. While *"sw[1..0]"* is act as user selected mode data bits outputs [3..2] for sub-modules *"selector_button".* However, the selected mode in this testbench is set for the input value *"rst"* in active-low condition to clear the temporary data register.

The interfacing between the alarm and floor level is made by the *"controller_floor".* The*"controller_floor _testbench"*is prepared to test the*"controller_floor"*and*"selector alarm"* modules to prove the simulation are able to identify and detect the alarm and level of the building if hazard occurred.

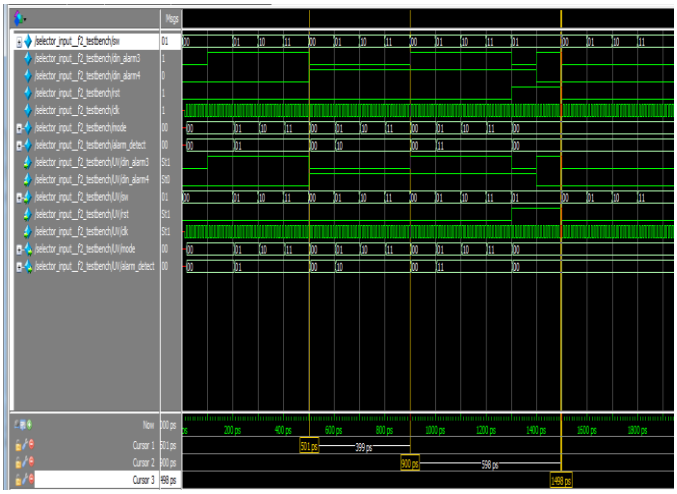


Figure 11: Output waveform for *"selector_input_f2_testbench"*

Figure 12 represents the RTL waveform of the test-bench controller system floor *"controller_floor_testbench"* for sub-modules *"controller_floor".* The input reset, *"rst"* is assigned to active-low at time '0ps- 1800ps', *"din_alarm[3..0]"* is declared to '4`b000' till '4`b1111'with 1-bit data for every time interval of "100ps". Hence, the output is produced based on the receiving input data *"din_alarm[3..0]"* by indicating the location of the detected alarm and its floor level of building assigned as *"display[3..0]", "alarm1", "alarm2", "alarm3", "alarm4", "floor[1..0]"* and *"alarm_alert".* The testbench is simulated in such that the data for *"din_alarm[3..0]"* is obtained by receiving inputs from *"selector_input_f1"* and *"selector_input_f2"* sub-module, respectively. However, the output also rely on the input value *"rst",* is in active-low to clear the temporary data register.

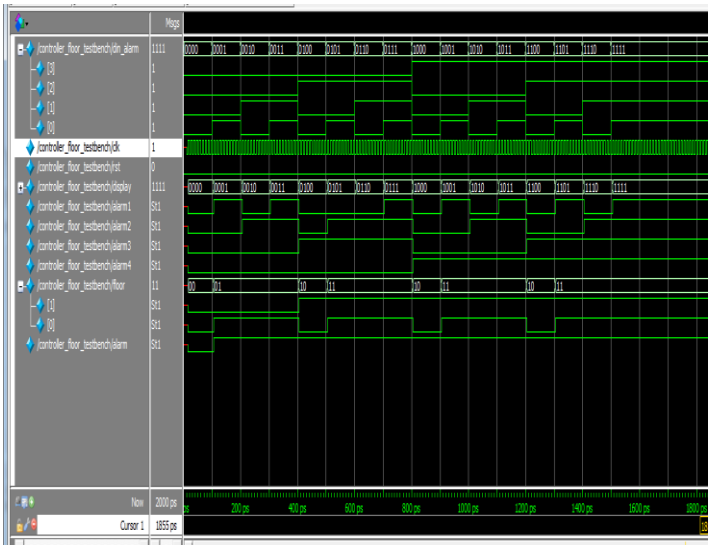


Figure 12: Output waveform for *"controller_floor _testbench"*

VI. CONCLUSION

The hardware functionality result and discussion for the controller selected modes layout (i.e. for mode 1, mode 2 and mode 3) were verified using the real hardware and displayed an output thru FPGA board (in several pattern movement design on LED display and also at LED7SEG with pattern right of shifting movement in displaying an output characters, *"FirE-OCCUrS"* that were chosen based on the limited graphic pattern of characters on 7 segments to encode to the DE2 Family ALTERA) and speaker in order to check the functionality of the designed architecture. The verification process for waveform simulation through Modelsim Altera Application tool involving "*controller_floor*" has shown that results meet the requirements of data signal flow as expected in theoretical control signal and data control.

VII. ACKNOWLEDGMENT

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