INVESTIGATION OF STRESS EFFECT TECHNOLOGY ON ELECTRICAL CHARACTERISTICS OF 90nm CMOS DEVICES

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4. Enhanced Research Title and Objectives

For the implementation of this research, no significant changes in the report from previous proposal since the research is mainly focus on simulation using SILVACO TCAD TOOL.

5. Report

5.1 Proposed Executive Summary

The implementation of this research is to find a solution for CMOS devices problems related to hot carrier effect due to advanced technology node where the devices are scaled in nano-region. Stress effect or known as strained silicon technology is capable to increase performance of CMOS devices in terms of the mobility of electrons and holes. This can significantly increased the performance of integrated circuits whereby CMOS devices are widely used. Four fabrication methods are identified for the purpose of this research which consist of shallow trench isolation, silicide, silicon nitride capping layer and embedded silicon germanium effect. All this fabrication techniques will be implemented in simulation using SILVACO TCAD tool. The CMOS devices under study will be 90nm CMOS devices. The results will be in the formed of device structure from fabrication process and characterization of the stressed CMOS devices.