Statistical Optimization Influence on High Permittivity Gate Spacer in 16nm DG-FinFET Device

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ABSTRACT

In this paper, the effect of high permittivity gate spacer on short channel effects (SCEs) for the 16 nm double-gate finFET is investigated, with the output responses optimized using L9 orthogonal array (OA) Taguchi method. The determination is done through Signal-to-noise ratio to the effectiveness of the process parameters towards four output responses such as threshold voltage (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) and Subthreshold Swing (SS). The virtual fabrication of the 16 nm double-gate fin FET was performed using ANTHENA module while the electrical characteristics of the device were simulated using ATLAS module. These two modules were combined with Taguchi method to aid in designing and optimizing the process parameters. The electrical characterization was performed and significant improvement could be seen on the TiO_2 and HfO_2 material in terms of the I_{ON}/I_{OFF} ratio obtained at 4.03×10^6 and 3.61×10^6 respectively for 0.179±12.7% V of V_{TH}. It can be observed that when approaching a higher value of dielectric constant (high-K), the I_{ON} increases while the SS and I_{OFF} decreases. As conclusion, the output responses from high-K materials have been proven to meet the minimum requirement by International Technology Roadmap Semiconductor (ITRS) 2013 for high performance Multi-Gate technology for the year 2015.

Keywords: *Double-gate FinFET; NMOS Device; Orthogonal Array; Taguchi Method; Statistical Method*

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Introduction

Several of classification of electronic devices consumed today that includes mobile phone, computer, smart systems in home equipment for which become increasingly thin, lightweight, and compact in order to make electronics more flexible and portable. That said, smaller devices demand has forced the electronic industry to revolutionize the CMOS technology embedded in the devices altogether as well. On top of that, Moore's Law scaling prediction suppression can be done through the proposed new semiconductor devices and applications [1, 2]. Various types of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) have been developed since then, while size of integrated devices reduces day by day with higher demand in multiple operations and therefore, causing size of MOSFETs which is the main component in memory and processors to be scaled down [3]–[9]. The reduction to nanometer regime has triggered the short channel effects to arise which degrades the system performance and reliability [10]. The devices performance may have been degraded via scaling process for the transistor miniaturization. The short channel effects (SCEs) have affected the device and the performance of the circuit in electron drift characteristics limitation within the channel, besides the reconstruction of the threshold voltage.

Therefore, a fin-shaped field effect transistor (FinFET) has been established in mitigating the SCEs in the occurrences of the more conventional planar MOSFET that have triggered the SCEs in the shrinking process. Constant challenges towards electrical definition to the parameter variations have also been studied [11]. Other than that, the performances of the transistor can be materialized through the implementation of FinFET. That said, the transconductance, carrier mobility and other possible parameters of the devices can be manipulated whereby the performance of the device can be hugely affected with the reduction to the channel length. Other introductions to the improvement of short channel performance includes the drain-induced barrier lowering (DIBL), subthreshold swing (SS) as well as threshold voltage (V_{TH}) roll-off that could yield enhancement to that of the desired results. The FinFET design of 16nm technology is designed along with the performance of the transistor that is improved in relation to the Moore's Law alongside the considerations on reducing the depletion depth of the silicon and also the gate oxide thickness to the proportion of the gate length. Therefore, the gate oxide thickness and the gate-controlled junction or depletion depth in the silicon have to be reduced in proportion to L (Gate Length).

In complimenting the enhancement of design processes in the Polysilicon/Silicon Dioxide ($PolySi/SiO_2$)-based DG-FinFET, several types of materials have been chosen with different constants, for which may significantly improve the output responses in threshold voltage level (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}), and sub-threshold swing (SS), with

four parameters chosen. Appropriate statistical analysis techniques have been implemented to apply the input process parameter optimization from data collected, as proven by others through the implementation of statistical method to improve the robustness of nanoelectronics engineering [12]–[18]. The optimization has been succeeded in process parameters via the application of Taguchi method by Salehuddin et al. and Afifah et al. for which the authors have underlined the optimization of both V_{TH} and I_{OFF} for a 45 nm besides lowering the I_{OFF} whilst nominalized the V_{TH} for a 22 nm design in addition to the execution of high-k/metal gate for the design [19]–[23]. In this case, the process optimization is utilized towards three different spacer materials.

Other than that, in obtaining the desired threshold V_{TH}, I_{ON}, I_{OFF}, and SS, several device characteristics is studied and optimized by implementing L_9 orthogonal array (OA) Taguchi statistical method since the variations of the process parameters may result in variations to the output responses [4]. The simulation based fabrication is done rather than the actual fabrication since it is proven to be more cost effective since it allows repetition to the experiment while the actual fabrication would have cost a lot more had the experiment to be done several times with variations in parameters. Besides, the disadvantage of the actual fabrication that is less feasible in gathering the immeasurable information however can take its place with virtual fabrication. The implementation of Taguchi method in this study is none other than the fact that the technique is extremely time effective as well as the robustness it is providing. Besides, Taguchi method also eases the actual fabrication process since its complexity increases as the device approaches the nanometer regime [18].

Methods and Materials

Device fabrication

The construction of 16nm DG-FinFET as shown in Table 1 in this study has been succeeded with the utilization of the ATHENA and ATLAS modules from Silvaco International for the virtual process simulation as both tools serve differently in obtaining the respective physical characterisations and its electrical characterisations. Additionally, five geometrical parameters that is identified in its ability to trigger variations towards the output responses whereby the variations may also be caused by the fluctuations to the process parameter over the variations to the local parameters that are 30% from the overall [19].

The physical structure mesh simulation is developed for a P-type silicon with the employment of substrate orientation at <100> for which is followed by the formation of the oxide layer on the silicon bulk that is purposed as mask during the implantation of P-well. Subsequent to the gate terminal that is

secluded from both source and drain, for which opposes the conductive channel by a dielectric layer, Boron is infused into the silicon substrate for $1x10^{17}$ atom/cm^3 before the gate oxide is established for 870 ºC with 3% of hydrochloric acid (HCl) in dry oxygen condition at 1 atmospheric pressure. Subsequently, the variation in threshold voltage can also be achieved with Boron implanted for $1.95x10^{13}$ atom/cm^3 with 5 KeV of energy in the channel region. Conclusively minor alterations on the gate concentration shall produce a significant difference to the variations of the said output responses. This phenomenon allows four most significant process parameters to be chosen based on the output responses produced with the same levels of parameter alterations. Subsequent to the deposition of polycrystalline silicon on the semiconductor wafer as the formation is succeeded to the multi-layered structure, the conformal polysilicon process follows.

Table 1: Minimum values of spacing and edge and end distances

Parameters	Value (nm)
Gate Length, L_G	16
SiO_2 Thickness, T_{OX}	3.25
Main substrate (silicon) length, L_C	35
Polysilicon Length, L_{DM}	17.3
Silicon Thickness, T_{FIN}	18.7

The utilisation of indium as a dopant for $1.17x10^{13}$ atom/cm^3 along with 1 KeV of energy has allowed the reduction in SCEs specifically for n-type doped Source/Drain (S/D) areas alongside the p-type substrate. The construction of sidewall spacer with the development of Si_3N_4 layer to the surface of both silicon and polysilicon. Implant of arsenic dose is compensated at $22x10^{18}$ atom/cm^3 with 3 KeV of implant energy formation to the S/D implantation, for which allowing the reduction inside capacitance. Metallization process taken its place through aluminium deposition followed by the patterning based on the formation of contact window in the S/D region before the structure is mirrored and defined. The final structure of the device is fabricated via simulated as shown in Figure 1. The optimization process follows the virtual fabrication process through an orthogonal array with three different levels based on process parameters chosen and that is identified to have shown significant changes towards the output responses.

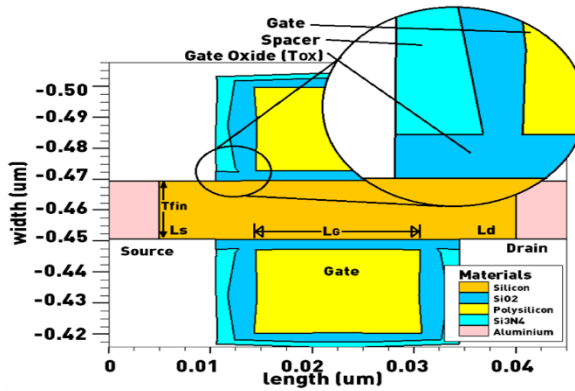

Figure 1: A simulated structure of the PolySi/SiO_2-based DG-FinFET.

Optimization using L9 Orthogonal Array for Taguchi method

The L9 orthogonal array (OA) selection has been due to the fact that it is suitable in the optimization environment that requires four relevant process parameters added to three different levels alongside two noise factors. The implementation of L9 and its experimental layout is as shown in Table 2 and Table 3, for each represents four process parameters and its levels, and the noise factor respectively. These range of value are within the standard ranges of semiconductor doping utilized in real fabrication process [24, 25]. V_{TH} doping dose, V_{TH} doping tilt, polysilicon doping dose and polysilicon doping tilt are all included in the process parameters with three different levels; where each is symbolled as A, B, C and D respectively. However, the V_{TH} doping dose differs depending on the material used since each material holds different permittivity values with Si_3N_4 with k = 9.5, HfO_2 with k = 25 and TiO_2 with k = 85 that produces different output responses.

The inclusion for the noise factor is required in the statistical designed by the Taguchi approach. That said, both gate oxide temperature, Y and polysilicon oxidation temperature, Z as both may minorly bringing some changes to the results. This is due to that the local parameter variations affects the changes in output responses by a third of the overall variations, given that the local parameter is varied. Performance improvement of the integrated circuits meanwhile have spurred the parameter fluctuation control for which consequently affecting the scaling process. That said the circumstances in the scaling process is also affected from increment in parameter variation. Meanwhile, the selection of L9 OA has been largely due to the total degree of freedoms whereby the differences in the output responses can be studied via the determination of the three-levelled OA from the lowest to the most. Throughout 9 experiments for three different arrays, combination of four

simulation experiments were held since the four experiments consisted in a single combination factor, were projected from two levels that is unified to two noise factors in Y_1Z_1, Y_1Z_2, Y_2Z_1, and Y_2Z_2.

Table 2: Experimental layout using l9 orthogonal array

Factor	Process Parameter Control Factor			
Experiment No.	A V_{TH} Doping Dose	B V_{TH} Doping Tilt	C Polysilicon Doping Dose	D Polysilicon Doping Tilt
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

Table 3: Experimental layout using l9 orthogonal array

Process Parameters		Unit	Level 1	Level 2	Level 3
VTH Doping Dose	Si_3Ni_4	atom/cm^3	3.85 x10^{13}	3.87 x10^{13}	3.89 x10^{13}
	HfO_2		3.75 x10^{13}	3.77 x10^{13}	3.79 x10^{13}
	TiO_2		3.75 x10^{13}	3.77 x10^{13}	3.79 x10^{13}
VTH Doping Tilt		deg.	5	6	7
Polysilicon Doping Dose		atom/cm^3	2.10 x10^{14}	2.12 x10^{14}	2.14 x10^{14}
Polysilicon Doping Tilt		deg.	-22	-21	-20

Table 4: Noise Factor of PolySi/SiO_2-based FinFET

Noise Factor	Units	Level 1	Level 2
Gate oxidation temperature, Y	ºC	870	875
Polysilicon oxidation temperature, Z	ºC	870	875

Each output responses desires different optimization characteristics, with V_{TH} classed as nominal-the-best (NTB), for which the V_{TH} is aimed at 0.179 V or within 12.7% of the value selected. I_{ON} meanwhile is targeted to be 1700 μA/μm or preferably higher than that and therefore best apply to larger-the-best (LTB) in order to achieve as high as possible given that the other output responses are achieving the targeted values. With I_{OFF} and SS requiring

values that are as minimum as possible, with I_{OFF} required to achieve lower than 100 pA/μm; the smaller-the-best (STB) characteristics is implemented to these aforementioned output responses. The values of SNR (ŋ) for the NTB, LTB and STB can be achieved with the dedicated equations in Equation (1), Equation (4) and Equation (5), respectively [26-28]:

$$\eta_{\mathrm{NTB}} = 10\log_{10}[\mu^2/\sigma^2] \tag{1}$$

where,

$$\mu = (Y_i + \cdots \ldots . + Y_n)/\mathrm{n} \tag{2}$$

and

$$\sigma^2 = \sum_{i=1}^{n} (Y_i - \mu)^2 /(\mathrm{n} - 1) \tag{3}$$

$$\eta_{\mathrm{STB}} = 10\log_{10}[\frac{1}{n}\sum (Y_1^2 + Y_2^2 + \cdots + Y_n^2)] \tag{4}$$

$$\eta_{\mathrm{LTB}} = 10\log_{10}[\frac{1}{n}\sum ((1/Y_1^2) + (1/Y_2^2) + \cdots + (1/Y_n^2))] \tag{5}$$

The experimental values for the output responses characteristics, as well as the number of tests and the value of the experimental responses are all represented by the respective η and Y_n. Consequently, the characteristics of experimental design's orthogonal allows every effect on the process parameter of the SNR to be break out at different levels. Through the implementation of the equation (1)-(5), the acquisition of mean, variance and SNR values for the PolySi/SiO_2 FinFET for spacer materials of Si_3N_4, HfO_2, and TiO_2 are gathered as in Tables 5, 6 and 7, respectively.

Table 5: Mean, variance and S/N Ratio for V_{TH}, I_{ON}, I_{OFF} and SS for Si_3N_4 spacer on PolySi/SiO_2-based FinFET

Exp. No.	V_{TH}				I_{ON}	I_{OFF}	SS
	Mean	Variance	SNR (Mean) (dB)	SNR (NTB) (dB)	SNR (LTB) (dB)	SNR (STB) (dB)	SNR(STB) (dB)
1	0.176	9.81E-06	-15.10	34.98	64.75	-57.52	-39.51
2	0.178	8.69E-06	-15.00	35.60	65.71	-60.40	-39.56
3	0.177	8.72E-06	-15.02	35.57	66.05	-62.47	-39.61
4	0.182	8.96E-06	-14.78	35.70	66.01	-61.36	-39.61
5	0.180	1.06E-05	-14.89	34.85	64.77	-56.69	-39.51
6	0.182	8.71E-06	-14.80	35.80	65.67	-59.47	-39.56
7	0.187	8.80E-06	-14.56	36.00	65.64	-58.45	-39.55
8	0.187	9.33E-06	-14.58	35.72	65.97	-60.43	-39.60

Table 6: Mean, variance and S/N Ratio for V_{TH}, I_{ON}, I_{OFF} and SS for HfO_2 spacer on PolySi/SiO_2-based FinFET

Exp. No.	V_{TH}				I_{ON}	I_{OFF}	SS
	Mean	Variance	SNR (Mean) (dB)	SNR (NTB) (dB)	SNR (LTB) (dB)	SNR (STB) (dB)	SNR(STB) (dB)
1	0.179	6.75E-06	-14.96	36.75	64.20	-51.64	-39.43
2	0.177	5.22E-06	-15.05	37.77	65.34	-55.16	-39.44
3	0.174	4.63E-06	-15.18	38.17	65.72	-57.40	-39.45
4	0.179	4.69E-06	-14.92	38.36	65.67	-60.92	-39.45
5	0.183	6.71E-06	-14.75	36.98	64.23	-51.70	-39.43
6	0.181	5.17E-06	-14.84	38.03	65.29	-54.21	-39.44
7	0.186	5.07E-06	-14.59	38.36	65.27	-53.19	-39.45
8	0.184	4.70E-06	-14.71	38.56	65.63	-55.33	-39.45

Table 7: Mean, variance and S/N Ratio for V_{TH}, I_{ON}, I_{OFF} and SS for TiO_2 spacer on PolySi/SiO_2-based FinFET

Exp. No.	V_{TH}				I_{ON}	I_{OFF}	SS
	Mean	Variance	SNR (Mean) (dB)	SNR (NTB) (dB)	SNR (LTB) (dB)	SNR (STB) (dB)	SNR(STB) (dB)
1	0.178	9.74E-06	-15.01	35.10	64.36	-51.91	-39.39
2	0.177	6.03E-06	-15.03	37.17	65.55	-55.40	-39.40
3	0.175	4.77E-06	-15.12	38.10	65.93	-57.62	-39.41
4	0.181	5.22E-06	-14.87	37.96	65.89	-56.50	-39.41
5	0.182	9.74E-06	-14.80	35.31	64.39	-51.12	-39.39
6	0.182	6.17E-06	-14.82	37.28	65.51	-54.45	-39.40
7	0.187	6.20E-06	-14.57	37.50	65.49	-53.44	-39.40
8	0.185	5.41E-06	-14.65	38.01	65.85	-55.56	-39.42

Results and Analysis

ANOVA for optimization

The analysis of variance (ANOVA) is capitalized by divisions of variance for which allows the output response variations can be achieved based on the process parameter set. The relative power factor is denoted by the factor effect percentage of SNR, which is affecting the reduction towards variation whereby the larger percentage contribution indicates larger significance towards the performance. Based on Table 8, for which is the factor effect towards the responses of V_{TH}, I_{ON}, I_{OFF} and SS for the device with Si_3N_4 spacer, polysilicon doping tilt for factor D showcases significance with 100% and 99% contribution for I_{ON} and SS and is dominant towards V_{TH} and I_{ON} with 71% and 86% respectively. V_{TH} doping dose contributes 19% as well towards V_{TH} which is highest among other output responses. However, both V_{TH} doping tilt and polysilicon shows highest percentage contribution at only 8% and 2% towards V_{TH}, for which is insignificant towards variations of the responses. That said, output responses I_{ON}, I_{OFF} and SS will highly reactive towards variations on the tilt to the polysilicon doping.

The reaction for the output responses for the device with HfO_2 spacer in Table 9 showcases similar reactions towards the parameter variations. V_{TH}, I_{ON}, and SS shows higher percentage factor against polysilicon doping tilt with significant 87%, 78% and 99% respectively, with only 35% dominant towards I_{ON}. However, the V_{TH} doping tilt, V_{TH} doping tilt and polysilicon doping dose

for factor A, B and C showcases 22% contribution factor towards I_{ON} with 12% and 14% percentage factor recorded towards V_{TH} and I_{OFF} for factor A.

Table 8: Factor effect of S/N ratio for V_{TH}, I_{ON}, I_{OFF} and SS for Si_3N_4 spacer on PolySi/SiO_2-based DG-FinFET

Symbol		A	B	C	D
Process Parameters		V_{TH} Doping Dose	V_{TH} Doping Tilt	Polysilicon Doping Dose	Polysilicon Doping Tilt
V_{TH}	Symbol	A3	B3	C1	D2
	% Factor	19	8	2	71
	Value	3.89×10^{13}	7	2.10×10^{13}	-20
I_{ON}	Symbol	A2	B2	C2	D2
	% Factor	0	0	0	100
	Value	3.87×10^{13}	6	2.12×10^{13}	-20
I_{OFF}	Symbol	A3	B2	C2	D1
	% Factor	14	0	0	86
	Value	3.89×10^{13}	6	2.12×10^{13}	-22
SS	Symbol	A2	B2	C2	D1
	% Factor	1	0	0	99
	Value	3.87×10^{13}	6	2.12×10^{13}	-22

Table 9: Factor effect of S/N ratio for V_{TH}, I_{ON}, I_{OFF} and SS for HfO_2 spacer on PolySi/SiO_2-based DG-FinFET

Symbol		A	B	C	D
Process Parameters		V_{TH} Doping Dose	V_{TH} Doping Tilt	Polysilicon Doping Dose	Polysilicon Doping Tilt
V_{TH}	Symbol	A1	B2	C2	D3
	% Factor	12	0	0	87
	Value	3.75×10^{13}	6	2.12×10^{13}	-20
I_{ON}	Symbol	A1	B1	C3	D3
	% Factor	22	22	22	35
	Value	3.75×10^{13}	5	2.14×10^{13}	-20
I_{OFF}	Symbol	A3	B2	C2	D1
	% Factor	14	4	5	78
	Value	3.79×10^{13}	6	2.12×10^{13}	-22
SS	Symbol	A2	B2	C2	D1
	% Factor	1	0	0	99
	Value	3.77×10^{13}	6	2.12×10^{13}	-22

Although Table 10 shows similar trends towards factor D for all process parameters at 96%, 100%, 89% and 87%, factor B and C show very minimum contribution to the responses with only SS might be varied with only 4% and 3% respectively. Factor A meanwhile shows minimum contribution towards V_{TH}, I_{OFF} and SS with respective 2%, 11% and 6% and zero contribution towards variations of I_{OFF}.

Table 10: Factor effect of S/N ratio for V_{TH}, I_{ON}, I_{OFF} and SS for TiO_2 spacer on PolySi/SiO_2-based DG-FinFET

Symbol		A	B	C	D
Process Parameters		V_{TH} Doping Dose	V_{TH} Doping Tilt	Polysilicon Doping Dose	Polysilicon Doping Tilt
V_{TH}	Symbol	A2	B2	C2	D3
	% Factor	2	1	1	96
	Value	3.77 x10^{13}	6	2.12 x10^{13}	-20
I_{ON}	Symbol	A2	B2	C2	D2
	% Factor	0	0	0	100
	Value	3.77 x10^{13}	6	2.12 x10^{13}	-20
I_{OFF}	Symbol	A3	B2	C2	D1
	% Factor	11	0	0	89
	Value	3.79 x10^{13}	6	2.12 x10^{13}	-22
SS	Symbol	A1	B2	C2	D1
	% Factor	6	4	3	87
	Value	3.75 x10^{13}	6	2.12 x10^{13}	-22

Confirmation tests for output responses

Every response in V_{TH}, I_{ON}, I_{OFF} and SS has generated the output response desired that are optimized, with each classed by NTB, LTB and STB. That add comparisons have been made to each of the optimum response combination before best combination settings are made through selections of overall optimized response. The best combination settings are chosen by prioritization towards threshold voltage for which is nominal. Secondly, leakage current (I_{OFF}) is prioritized ahead of I_{ON} and SS as higher I_{OFF} will likely suffer the values of I_{ON}/I_{OFF} ratio despite high I_{ON} achieved. The prioritization to the combinations has been chosen based on the hierarchical order from V_{TH}, I_{OFF}, I_{ON} and SS desired respectively. Subsequently, confirmation tests are run via best setting combination as in Tables 11, 12 and 13, each representing the FinFET device with S_3N_4, HfO_2 and TiO_2 in that order, for spacer materials.

Table 11: Best setting combination for Si_3N_4 spacer on PolySi/SiO_2-based DG-FinFET

Symbol	Process Parameters	Best Combination		
		Symbol	% Factor	Value
A	VTH Doping Dose	A3	19	3.89 x10^{13} atom cm^{-3}
B	VTH Doping Tilt	B3	8	7º
C	Polysilicon Doping Dose	C1	2	2.10 x10^{13} atom cm^{-3}
D	Polysilicon Doping Tilt	D2	100	-21º

Table 12: Best setting combination for HfO_2 spacer on PolySi/SiO_2-based DG-FinFET

Symbol	Process Parameters	Best Combination		
		Symbol	% Factor	Value
A	VTH Doping Dose	A1	22	3.75 x10^{13}atom cm^{-3}
B	VTH Doping Tilt	B1	22	5º
C	Polysilicon Doping Dose	C3	22	2.14 x10^{13} atom cm^{-3}
D	Polysilicon Doping Tilt	D1	99	-22º

Table 13: Best setting combination for TiO_2 spacer on PolySi/SiO_2-based DG-FinFET

Symbol	Process Parameters	Best Combination		
		Symbol	% Factor	Value
A	VTH Doping Dose	A3	11	3.79 x10^{13} atom cm^{-3}
B	VTH Doping Tilt	B3	0	7º
C	Polysilicon Doping Dose	C2	3	2.12 x10^{13} atom cm^{-3}
D	Polysilicon Doping Tilt	D1	89	-22º

The results in Table 14 consists of initial simulated experiment, for which represents the responses achieved before it is optimized via Taguchi approach. Meanwhile, optimized simulations are achieved via simulation run based on the best setting combinations achieved from the aforementioned Tables 11, 12 and 13, with noise factor Y and Z in considerations whereby the noise factor along with the combination requires four runs for each spacer material design. The estimated value from the optimized simulations are also obtained through the SNR ranges achieved for each of the four parameters.

Table 14: Comparisons between optimized value with combination of $A_3B_3C_1D_2$ and the ITRS prediction for Si_3N_4 spacer

Device Characteristics	Pre-optimized Simulation	Optimized Simulation (Taguchi)		ITRS 2013 prediction (target o/p) [29]
		Estimated	Observed	
Level	$A_1B_1C_1D_1$	$A_3B_3C_1D_2$		
V_{TH} (V)	0.1871	0.167	0.1801	0.179
% Diff from target o/p	4.33	6.70	0.61	-
SNR-NTB (dB)	36.00	35.5	34.85	-
I_{ON} (μA/μm)	1916.87	1880.0	1740.97	>1700
% Diff from target o/p	11.31	9.57	2.35	-
SNR-LTB (dB)	65.64	65.5	64.77	-
I_{OFF} (nA/μm)	0.812	0.908	0.649	<100
% Diff from target o/p	99.19	99.09	99.35	-
SNR-STB (dB)	-58.45	-59.20	-56.69	-
I_{ON} /I_{OFF} ratio	2.36×10^6	2.07×10^6	2.68×10^6	1.7×10^4
SNR-LTB (dB)	-	-	-	-
SS (mV/dec)	93.18	95.00	94.47	N/A
% Diff from target o/p	-	-	-	N/A
SNR-STB (dB)	-39.65	-39.6	-39.51	N/A

Based on the results obtained, comprising the pre-optimized simulations, optimized solutions with the implementation of Taguchi statistical method, Tables 14, 15 and 16, V_{TH} is shown to have achieved within ±12.7% range from the targeted 0.179 V based on the roadmap provided by the ITRS 2013 based on the optimized results observed for Si_3N_4, HfO_2 and TiO_2. This is to precisely evaluate the performance in terms of the corresponding I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, and SS of the aforementioned device. An improvement is showcased towards the I_{ON}/I_{OFF} ratio on each of the optimized simulated experiments. This is due to the prioritization made towards lowering the I_{OFF} for which have significantly encouraged the rise in the I_{ON}/I_{OFF} ratio despite reduction in I_{ON} after the optimization succeeded. The significance of having a very high value of the I_{ON}/I_{OFF} ratio because it is suitable for high-speed logic and low power application [30,31]. The I_{ON}/I_{OFF} ratio is at 2.68×10^6 after it is optimized compared to 2.36×10^6 for Si_3N_4 spacer design, with another improvement on I_{ON}/I_{OFF} ratio for HfO_2 spacer design as well with 3.61×10^6 from the previous 3.29×10^6. TiO_2 spacer design meanwhile showcased a major leap to 4.03×10^6 from 3.2829×10^6. Besides, the V_{TH}

approaches closer to 0.179 V for both Si_3N_4 and HfO_2 with 0.61% and 1.16% respectively. Despite the slight increment towards the difference to 0.19% rather than 0.18% before optimized, the V_{TH} for TiO_2 spacer proves to achieved within ±12.7% range of 0.179 V [29].

Table 15: Comparisons between optimized value with combination of $A_1B_1C_3D_1$ and the ITRS prediction for HfO_2 spacer

Device Characteristics	Pre-optimized Simulation	Optimized Simulation (Taguchi)		ITRS 2013 prediction (target value) [29]
		Estimated	Observed	
Level	$A_1B_1C_1D_1$	$A_3B_3C_1D_2$		
V_{TH} (V)	0.184	0.129	0.181	0.179
% Diff from target o/p	2.61	27.93	1.16	-
SNR (dB)	38.56	37.81	38.03	-
I_{ON} (μA/μm)	1913.08	1490.0	1840.60	>1700
% Diff from target o/p	12.53	12.35	8.27	-
SNR (dB)	65.63	63.50	65.29	-
I_{OFF} (nA/μm)	0.582	0.523	0.510	<100
% Diff from target o/p	99.42	99.48	99.49	-
SNR (dB)	-55.33	-54.40	-54.21	-
I_{ON} /I_{OFF} ratio	3.29×10^6	2.85×10^6	3.61×10^6	1.7×10^4
SNR (dB)	-	-	-	-
SS (mV/dec)	93.89	93.80	93.78	N/A
% Diff from target o/p	-	-	-	N/A
SNR (dB)	-39.45	-39.44	-39.44	N/A

Table 16: Comparisons between optimized value with combination of $A_3B_3C_2D_1$ and the ITRS prediction for TiO_2 spacer

Device Characteristics	Pre-optimized Simulation	Optimized Simulation (Taguchi)		ITRS 2013 prediction (target value) [29]
		Estimated	Observed	
Level	$A_1B_1C_1D_1$	$A_3B_3C_1D_2$		
V_{TH} (V)	0.185	0.143	0.187	0.179
% Diff from target o/p	0.61	3.60	0.78	-
SNR (dB)	38.01	36.90	35.88	-
I_{ON} (μA/μm)	1961.19	1830.00	1882.35	>1700
% Diff from target o/p	15.36	7.65	10.73	-
SNR (dB)	65.85	65.30	64.33	-
I_{OFF} (nA/μm)	0.510	0.502	0.597	<100
% Diff from target o/p	99.49	99.50	99.40	-
SNR (dB)	-55.56	-54.1	-50.10	-
I_{ON} /I_{OFF} ratio	3.28×10^6	3.64×10^6	4.03×10^6	1.7×10^4
SNR (dB)	-	-	-	-
SS (mV/dec)	93.59	93.30	93.34	N/A
% Diff from target o/p	-	-	-	N/A
SNR (dB)	-39.42	-39.40	-39.39	N/A

Conclusion

In conclusion, the DG-FinFET from simulations has established good electrical properties such as high drive current and low leakage current based on the electrical characteristic analyzed. With sufficing V_{TH} that is within the predicted ±12.7% of 0.179 V, the TiO_2 and HfO_2 meanwhile have resulted in improvement of the device due to increment towards the I_{ON}/I_{OFF} ratio at respective 4.03×10^6 and 3.61×10^6 due to the permittivity of the material alongside the optimization that allows the values of I_{OFF} to be minimized despite lower I_{ON} acquired. It can be concluding that polysilicon doping tilt (factor D) is the most significant factor towards the output responses. That said, TiO_2-materialed spacer with combination of $A_3B_3C_2D_1$ shows the best I_{ON}/I_{OFF} ratio in conjunction to the device's power consumption efficiency. Besides that, the device characteristics have met the requirement of high performance (HP) multi-gate (MG) technology predicted by ITRS 2013 for the year 2015 requirements.

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