UNIVERSITI TEKNOLOGI MARA

NBTI EFFECTS ON THE PERFORMANCE OF SET AND DET D FLIP-FLOP TOPOLOGIES BY USING MOSRA AND PREDICTIVE TECHNOLOGY MODELS

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MSc

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AUTHOR'S DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the results of my own work, unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any degree or qualification.

I, hereby, acknowledge that I have been supplied with the Academic Rules and Regulations for Post Graduate, Universiti Teknologi MARA, regulating the conduct of my study and research.

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ABSTRACT

Negative Bias Temperature Instability (NBTI) is an aging mechanism that has become a key reliability issue in MOSFETs technology as well as FinFETs technology. The main reliability issues regarding the NBTI mechanism are that NBTI not only degrades the transistor electrical properties but also degrades the device performance as well as shortens the device operation lifetime over time. Therefore, the main objective of this study is to investigate the effect of the NBTI mechanism on the performance of the flip-flop circuits based on Single-Edge Triggered Flip-Flop (SETFF) and Double-Edge Triggered Flip-Flop (DETFF). In this work, the flip-flop circuits are simulated with different stress conditions and process variations by using HSPICE with MOSFET Reliability Analysis (MOSRA) and Predictive Technology Model (PTM) from 32nm to 16nm. The results suggested that the flip-flop circuits based on FinFET technology and MOSRA-based interface trap model (at V_{DD}=0.85V and T=125°C) can increase the delay time by 0.026% to 4.27% while the power consumption decreases by 21.67% to 26.34%. Under the same stress conditions, the findings have shown that the performance of DETFFs has higher degradation compare to SETFFs which results in 4.27% increase in delay time and 26.34% reduction in power consumption.

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