POWER EFFICIENT CMOS OTA



RESEARCH MANAGEMENT INSTITUTE (RMI) UNIVERSITI TEKNOLOGI MARA 40450 SHAH ALAM, SELANGOR MALAYSIA

BY:

NORDIANA BTE MUKAHAR SITI AISHAH CHE KAR

DECEMBER 2012

3. Acknowledgements

I would like to thanks to Research Management Institute for providing me financial support through Excellent Fund to make this research possible. Last but not least, special thanks I dedicate to my beloved family especially to my parent and also my colleagues in UiTM Terengganu.

5. Report

5.1 Proposed Executive Summary

Research in analogue circuit design is focused on low power battery operated equipment to be used in portable equipment of electronic application. A reduced supply voltage is necessary to decrease power consumption to ensure reasonable battery lifetime in portable electronics. Realizing high performance analogue circuit with limitation of power is a challenge. A device's figure of merit is illustrated by the gain-bandwidth product which states that at higher frequencies, the gain decreases. Higher bias current is needed in order to have a good gain at high frequency. This shows that in general a fast circuit consumes high power and it inherent property prompts for specific techniques that can reduce power while maintaining performance. Operational Transconductance Amplifier (OTA) is a fundamental building block of analogue circuit and systems. In OTA, the ratio of transconductance to current consumption reflects the power efficiency of the amplifier. This motivate the study presented in this work, searching for a power efficient OTA architecture with good supply voltage scalability and large flexibility for power/speed trade offs, while maintaining the correct analogue functionality. Most of the researchers focused on developing new method of designing op amp without sacrificing the power consumption and area. Transconductance has great influence in determining the power, stability and gain of the circuit system. Conventional method to enhance the transconductance of the circuit is by adding the gain boosting circuit or cascaded the output stage. This method will greatly increase the transconductance so as to improve the gain but it will also affect the stability of the analogue circuit system. The main focus in this research is on implementing new transconductance based technique to the main circuit without adding new block to the main amplifier. At the end of the research the performance of the improved OTA architecture with transconductance based technique will be analyzed and compared with the available circuit design.

5.2 Enhanced Executive Summary

Research in analogue circuit design is focused on low power battery operated equipment to be used in portable equipment of electronic application. A reduced supply voltage is necessary to decrease power consumption to ensure reasonable battery lifetime in portable electronics. Realizing high performance analogue circuit with limitation of power is a challenge. A device's figure of merit is illustrated by the gain-bandwidth product which states that at higher frequencies, the gain decreases. Higher bias current is needed in order to have a good gain at high frequency. This shows that in general a fast circuit consumes high power and it inherent property prompts for specific techniques that can reduce power while maintaining performance. Operational Transconductance Amplifier (OTA) is a fundamental building block of analogue circuit and systems. In OTA, the ratio of transconductance to current consumption reflects the power efficiency of the amplifier and transconductance has great influence in determining the power, stability and gain of the circuit system. Improved architecture of recycle folded cascade OTA with current control circuit using transconductance based methodology has been proposed in this work. This is achieved by exploiting and using idle device in the signal path and separates the AC and DC path, which results in an enhanced transconductance, output resistance, gain, settling time and power dissipation. Recycle folded cascade amplifier architecture was implemented in 90 nm CMOS process with 1 V power supply. Simulation results shows that the proposed structure significantly increase the DC gain bandwidth compared to the recycle folded cascade OTA and consume very low power dissipation. Theoretical analysis and LTSpice simulations prove the performance of the new OTA.

2

Contents

. Letter of Report Submission	iii
. Letter of Offer (Research Grant)	iv
Acknowledgements	V
. Enhanced Research Title and Objectives	vi
. Report	1
.1 Proposed Executive Summary	1
.2 Enhanced Executive Summary	2
.3 Introduction	3
5.3.1 Problem Statement	3
5.3.2 Objectives	4
5.3.3 Scope of Study	4
.4 Brief Literature Review	4
.5 Methodology	5
.6 Results and Discussion	9
.7 Conclusion and Recommendation	11
.8 References/Bibliography	12
Research Outcomes	14
Appendix	15