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Performance of High-k Dielectric Material for Short Channel Length MOSFET Simulated using Silvaco TCAD Tools

Fatin Antasha Anizam, Lyly Nyl Ismail, Norsabrina Sihab and Nur Sa'adah Mohd Sauki

***Abstract*—Short channel effect (SCE) occur in the MOSFET devices when the oxide layer became thinner, and the gate length become shorter. The purposed of this study is to find a new dielectric and gate material to replace the conventional oxide which is silicon dioxide (SiO_2) and polysilicon as gate material. The objective of this study is to investigate the performance of MOSFET using different types of high-k dielectric material and germanium (Ge) as gate material. The MOSFET structure was fabricated and simulated using Silvaco TCAD tool. The overall performance of the MOSFET is evaluated based on the current-voltage (I-V) characteristics. Result show that MOSFET fabricated with HfO_2 and Ge as dielectric and gate material has high drive current reduce leakage current by a factor of 0.55 from the conventional MOSFET. Therefore, combination of HfO_2 and Ge in MOSFET structure has the best performance compared to SiO_2 and polysilicon because it produces smaller leakage current and smaller V_{th} when shrinking the device sizes, hence reducing SCEs.**

***Index Terms*—Dielectric material, High-k, short channel effect, threshold voltage.**

I. INTRODUCTION

THE process to diminish the size of MOSFET devices have been control the technology for about three decades and it seems that this trend will continue for many more years [1]. The demands to scale down the channel length comes from DRAM industry as they want to reduce the cost [2].

This manuscript is submitted on 22th June 2021 and accepted on 25th August 2021. Fatin Antasha Anizam is with the School of Electrical Engineering, College of Engineering, University Teknologi MARA Cawangan Pulau Pinang, MALAYSIA (e-mail: antashafatin@gmail.edu.my).

Lyly Nyl Ismail is with the School of Electrical Engineering, College of Engineering, University Teknologi MARA Cawangan Pulau Pinang, MALAYSIA (e-mail: lylynyl814@uitm.edu.my).

Norsabrina Sihab is with the School of Electrical Engineering, College of Engineering, University Teknologi MARA Cawangan Pulau Pinang, MALAYSIA (e-mail: norsabrina@uitm.edu.my).

Nur Sa'adah Mohd Sauki is with the School of Electrical Engineering, College of Engineering, University Teknologi MARA Cawangan Pulau Pinang, MALAYSIA (e-mail: norsabrina@uitm.edu.my).

Since 1960, silicon dioxide (SiO_2) have been used as dielectric materials in microelectronics industry [1]. The gate oxide has been continuously scaled down from days to days as rapidly growth of technology in transistor and integrated circuits technology. Today, the gate oxide has been successfully shrinking up to 1.5 nm thick [2].

Shrinking the size of MOSFET will make the source and drain move closer to the gate. When the gate voltage, V_G are larger than source-drain voltage, V_{DS}, channel or path is created for electron and holes to move from source to drain [3]. Nevertheless, keep increasing V_G, it causes drain and source to move more closer to gate and causes short channel effect (SCEs) to occur. SCEs will interfere the current flow and potential distributions of MOSFET hence worsen the performances. Some of the limitations to narrowing the size of devices is gate insulator scaling, shallow junction technology, SCEs and off-state leakage current in MOSFET devices. Varied dielectric thickness and channel length can reduce the device's size but leading to tunnelling leakage current between source and drain [4]. In addition, there are several disadvantages of using SiO_2 as dielectric material. SiO_2 have limited maximum capacitance and tunnelling current leakage increases if the thickness of SiO_2 decreased [5]. Consequently, to designs smaller or ultra-thin MOSFET, many things should be considered such as dielectric material.

High-k material is suggested to replace SiO_2in this study to overcome the SCEs issue. The purpose of using high-k material is because it has low interface state density and good thermal stability [6]. I-V characteristics of MOSFET such as threshold voltage, $V_{th,}$ drive current, I_{ON} and leakage current, I_{OFF} are the parameter that affected when changing the dielectric material because its value depends on the value of the dielectric constant and the thickness of the dielectric layer. With high value of dielectric constant, the thickness of the dielectric or oxide layer can be modified so that the I-V characteristic can be enhanced [7, 8]. Table 1 below summarized some high-k material that compatible with silicon (Si) substrate which has high dielectric constant, k and high energy band gap, E_g. Hafnium oxide (HfO_2) were selected to use a new dielectric material because it has the high dielectric constants ~ 22, high energy gap, E_g in the range of 4.5 ~ 6.0 eV, high I_{ON} and low I_{OFF}.

Other researcher suggested by changing the material use to fabricate gate from polysilicon to metal can also enhance mobility and reduce leakage current in MOSFET device, hence increased the device performance. This is because metal has lower value of E_g. Germanium (Ge) are proposed in this study to replace polysilicon because Ge has energy bandgap for around 0.6 eV while polysilicon is 1.1 eV [9].

TABLE I
PROPERTIES OF HIGH-K DIELECTRIC MATERIAL

MATERIAL	DIELECTRIC CONSTANT, K	Energyband gap, Eg (eV)	Offset Eg (eV)
SiO_2	3.9	8.9 ~ 9.0	3.0 ~ 3.5
Si_3N_4	7.9	5.0 ~ 5.3	2.0 ~ 2.4
Al_2O_3	9.5	5.6 ~ 9.0	2.78 ~ 3.5
HfO_2	22	4.5 ~ 6.0	1.5

Therefore, the objective of this study is to overcome the SCEs in MOSFET fabricate with SiO_2 and polysilicon as dielectric and gate material. This study was to investigate the performance of MOSFET fabricate with high-k dielectric (HfO_2) and Ge as new dielectric and gate material, respectively. The performance of the new structure MOSFET (HO_2 and Ge) is evaluated based on the I-V characteristics. The result of a new structure MOSFET was compared with conventional MOSFET that use SiO_2 and polysilicon. The fabrication of MOSFET structure was simulated using Silvaco TCAD tool where Athena was used to produce the MOSFET structure and ATLAS to investigate the device performance which is the I-V characteristics.

II. METHODOLOGY

A. MOSFET Device Structure

There are two type of MOSFET structure are simulated using Silvaco TCAD tool as shown on Fig.1. First MOSFET structure using SiO_2 and polysilicon as dielectric and gate material, respectively and second structure of MOSFET using high-k and Ge as dielectric and gate material, respectively. Thickness of oxide layer, t_{ox} and channel length, L_g was varied to investigate the I-V characteristic which focus on threshold voltage, $V_{th,}$ drive current, I_{ON} and leakage current, I_{OFF}. The performance of MOSFET was compared to investigate which one have the best performances. Athena were used to create a two-dimensional (2D) MOSFET structure. The parameter properties used to create the MOSFET structure are tabulate in Table 2.

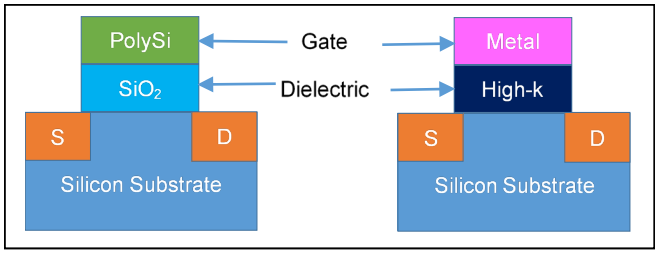

Fig. 1. MOSFET structure (a) SiO2 as dielectric material (b) High-k as dielectric material.

TABLE II
PARAMETER FOR NMOS STRUCTURE

PARAMETER	MOSFET WITH POLYSI AS GATE	MOSFET with Ge as Gate
Acceptor doping	1×10^{20}	2.02×10^{12}
Donor doping	1×10^{20}	2.02×10^{12}
Substrate / channel doping	1×10^{17}	4×10^{15}
1) Dielectric gate	SiO_2, Al_2O_3, Si_3N_4, HfO_2	HfO_2
2) Substrate	Si	Si
3) Source	Al	Al
4) Gate	PolySi	PolySi & Ge
5) Drain	Al	Al

B. ATLAS Simulator

ATLAS has been used to analyse the electrical behaviour in MOSFET structure. It consists of a few files, which are text file, log file and structure file. All the command was written in text file. Structure file store all 2D data related with value of solution and defines all the structure that was simulated. Tony plot is the visualization tool that comprehensives to view and analyse simulator output [11]. In this study, it was used to generate the result and graph of I-V characteristics such as drain current vs gate voltage (I_D-V_G), drain current vs drain voltage, (I_D-V_D), threshold voltage, $V_{th,}$ drive current, I_{ON} and leakage current, I_{OFF}. Table 3 summarized the list of coding used in ATLAS to extract the I_D-V_G and I_D-V_D.

TABLE III
PROPERTIES OF HIGH-K DIELECTRIC MATERIAL

Symbol	Coding	Explaination
1	solve init solve vdrain=0.05 solve vdrain=0.1 solve vdrain=0.2 solve vdrain=0.5 log oufile=sio2.log solve vgate=0 vstep=0.05 vfinal=1 name=gate tonyplot sio2.log sio2.net	Set drain biases and I_D-V_G graph was plotted on Tonyplot
2	solve init solve vgate=3.3 outf=solve_hfo21um load infile=solve_hfo21um log outf= hfo21um.log solve name=drain vdrain=0 vfinal=3.3 vstep=0.3	Set gate biases and I_D-V_D graph was plotted on Tonyplot

III. RESULTS AND DISCUSSION

The performance of MOSFET structure on V_{th}, leakage current and I_D-V_G and I_D-V_D characteristics can be investigated by vary thickness of oxide, t_{ox} layer and vary channel length, L_g.

A. Fabrication of MOSFET structure

Figure 2 show the two types of MOSFET structure that was simulated using ATHENA. Figure 2(a) show the 1st MOSFET structure with SiO_2 and polysilicon as dielectric and gate

material while Fig. 2(b) show the 2nd MOSFET structure with HfO_2 and Ge as dielectric and gate material. For both structure the oxide thickness, t_{ox} and channel length was set to be fixed values which is t_{ox} is10 nm and L_g is 1.0 um because these two values are the maximum value for SiO_2 as dielectric. Above these values, MOSFET with SiO_2 start showing the degradation in device performance due to SCEs effect.

Once the MOSFET structure are constructed, the extract data for I-V characteristics which is I_D-V_D and I_D-V_G can be obtained. From the I_D-V_D and I_D-V_G, data for V_{th}, I_{ON} and I_{OFF} can be obtained. Data for I_{ON} and I_{OFF} was used to identify which structure has the best MOSFET performance, best MOSFET structure performance was obtained when I_{OFF} = 0 and has higher value of I_{ON}. Equation (1) show the relationship between dielectric constant, k and oxide thickness, t_{ox} [12]. Smaller k with smaller t_{ox} produce larger capacitance hence higher in device leakage current, I_{OFF} . It is undesirable to have high I_{OFF} because high-power consumption and decreases the efficiency of the system. High I_{ON} was needed to control process of charge and discharge the circuit and it can be used for fast switching device[2].

$$\frac{C_{ox}}{A} = \frac{k \times \varepsilon_o}{t_{ox}} \quad (1)$$

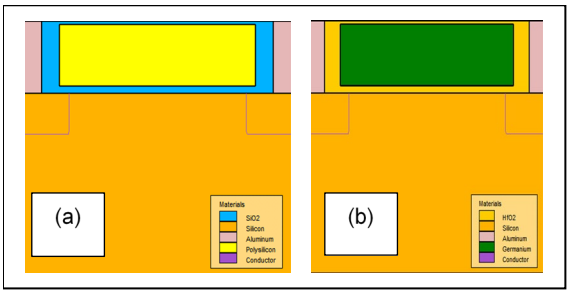

Fig. 2. MOSFET structure with (a) SiO_2 and polySi as dielectricand gate material (b)) HfO_2 and Ge as dielectric and gate material.

Figure 3 shows I_D-V_G graph for MOSFET with different dielectric material. It shows that HfO_2 has larger value of I_{ON} ~ 60.5 x10^{-6} A/um and low I_{OFF} ~ 92.4 x10^{-12} A/um when compared to SiO_2 with I_{ON} of 21.5 x 10^{-6} A/um and I_{OFF} of 0.126 x10^{-9} A/um. This result proved that using HfO_2 as dielectric material can increased the MOSFET performance because it has higher value of I_{ON} and low value of I_{OFF} due to high value of k even though it has low mobility.

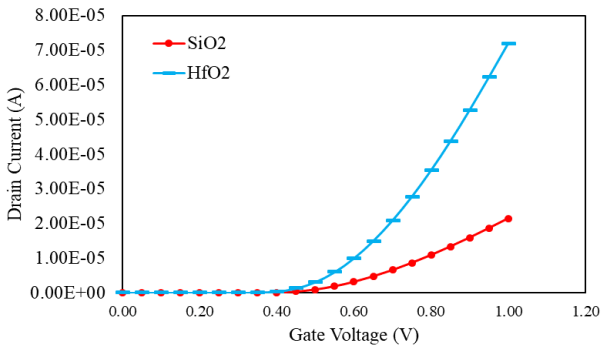

Fig. 3. I_D-V_D graph for MOSFET structure with SiO_2 and HfO_2 as dielectric material.

B. *Fabrication of MOSFET using different gate material*

The purpose of simulating MOSFET with different gate material is to enhance the lower mobility that occur in the MOSFET structure with SiO_2 and HfO_2. Patiya et.al stated that material with lower energy band gap are capable to boost the mobility of a device. Higher mobility device has less leakage current and smaller subthreshold voltage, *subvt* [9].

Figure 4 show the comparison of I_D-V_G graph MOSFET with HfO_2 as dielectric and polysilicon and Ge as gate material. MOSFET with Ge has I_{OFF} of 6.94 x 10^{-11} A/um and I_{ON} is 1.63 x 10^{-6} A/um. While MOSFET with polysilicon has I_{OFF} of 1.2 x 10^{-10} A/um and I_{ON} is 7.19 x 10^{-5} A/um. From the result show that MOSFET with Ge has reduced leakage current by a factor of 0.58. This result proved that using Ge as gate material enhance the MOSFET performance because Ge serves as a carrier and can pack in more electrons than polysilicon [9, 13]. It also concludes that HfO_2 and Ge are having good MOSFET performance.

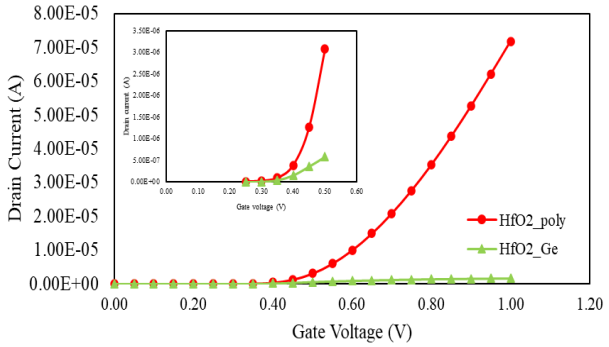

Fig. 4. Comparison of I_D-V_G graph for MOSFET structure with HfO_2 as dielectric and PolySi and Ge as gate material.

C. *Effect of Oxide Thickness*

Oxide thickness, t_{ox} also play important role in determine the MOSFET performance. Equation (1) and (2) show the relationship between t_{ox} and V_{th}. The device with thinner oxide layer has higher I_{ON} and it has lower gate control for the process of turning "on and off" of the device [16]. It also shows better interface layer between dielectric and gate material and hence improve the performance of the transistor [14].

Leakage current, I_{OFF} can be obtained from the I_D-$V_G$graph which is at low drain voltage, V_D. Leakage current was triggered by the charging tunneling of the traps in the interface between oxides and the semiconductor [15]. I_{OFF} become higher due to weak inversion state leakage that is a function of V_{th}.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_G - V_T)^2 \quad (2)$$

Figure 5 and fig. 6 illustrates the thickness of oxide layer that was vary from 5 to 15 nm for both MOSFET structure. Figure 7 show the I_D-V_G graph of MOSFET when t_{ox} at 5nm.

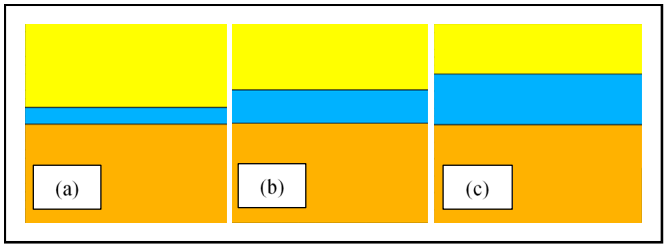

Fig. 5. 1st MOSFET structure with variation of oxide thickness (a) 5 nm (b) 10 nm (c) 15 nm

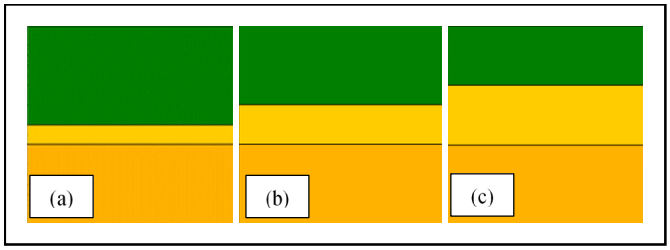

Fig. 6. 2nd MOSFET structure with variation of oxide thickness (a) 5 nm (b) 10 nm (c) 15 nm

I_{OFF} can be reduced by reducing *subvt* as reducing t_{ox} will decrease C_{ox} hence *subvt* is lower. *Subvt* was defined by using Eq. (3). If V_G is under V_{th}, the transistor flows into the subvt region with a very tiny current[3]. Fast switching device was obtained on a device with lower *subvt* [10]. High-k material has acceptable I_{ON} that reduce *subvt*. *Subvt* determines how much gate voltage swing that is needed to change the current one-decade, based on the result obtained in Table 3, the value is around 70 ~ 100 mV/decade[3]. Thus, $HfO_2$was fast switching device that has smallest *subvt* value as compared to SiO_2.

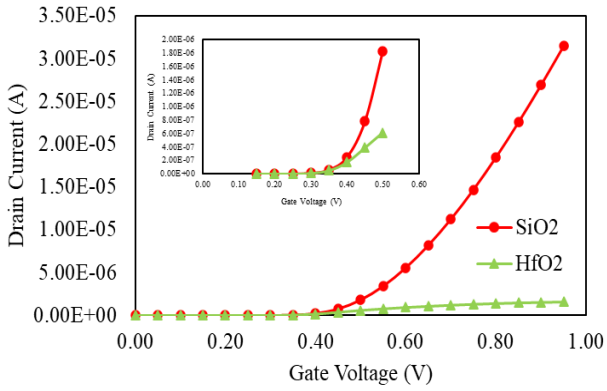

Fig. 7. I_D-V_D graph for oxide thickness at 5 nm

Table 4 show the comparison of I-V data when t_{ox} is varies. Thicker oxide layer affect increasing in V_{GS} and increase I_{OFF}. Besides, it also proves that the V_{th} value will increase as t_{ox} increase.

TABLE IV
COMPARISON OF MOSFET PERFROMANCE WHEN OXIDE THICKNESS VARIES

	SiO_2			HFO_2		
t_{ox} (nm)	5	10	15	5	10	15
V_{th} (V)	0.361	0.365	0.377	0.114	0.119	0.124
Subvt (mV/dec)	0.076	0.081	0.086	0.074	0.075	0.076
I_{ON} ($x10^{-6}$ A/cm)	36.1	21.5	15.1	1.66	1.63	1.61
I_{OFF} ($x10^{-12}$ A/cm)	122	126	128	68.8	69.4	70.1
I_{ON}/I_{OFF} ($x10^6$)	0.295	0.171	0.118	0.024	0.023	0.023

D. *Effect of Channel Length*

Channel length is directly proportional with V_{th} . When V_{th} drop too much, I_{OFF} become too large and L_g will turned to unacceptable value. Theoretical, by decreasing Lg, the saturation drain current will increase.

In this study, L_g was varied from 0.5 um, 0.8 um and 1.0 um to obtain the optimized L_g with good performance MOSFET. Figure 8 and fig. 9 shows the comparison I_D-V_G for MOSFET with SiO_2 and HfO_2 when L_g is varies. Reducing L_g, increased the saturation drain current, I_{DS} and reducing the V_{th} value. As V_{th} was reduced, distance for drain to source and drain to channel also reduced. L_g with 0.8um show the best optimized data for MOSFET fabricate with SiO_2 and HfO_2. Figure 10 show the comparison graph of I_D-V_G for MOSFET with SiO_2 and HfO_2 at L_g of 0.8 um.

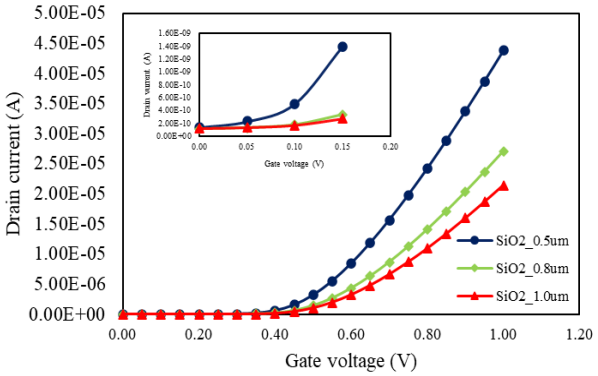

Fig. 8. MOSFET structure with SiO_2 when channel length is varies.

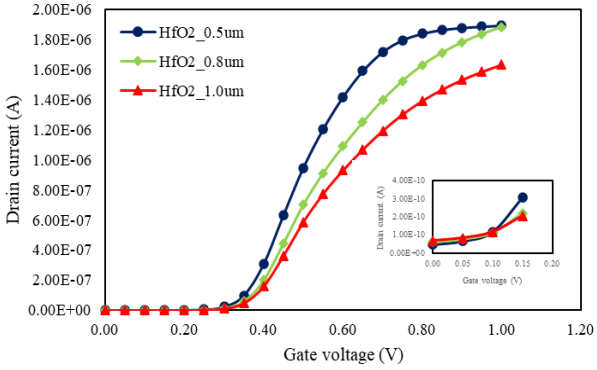

Fig. 9. MOSFET structure with HfO_2 when channel length is varies

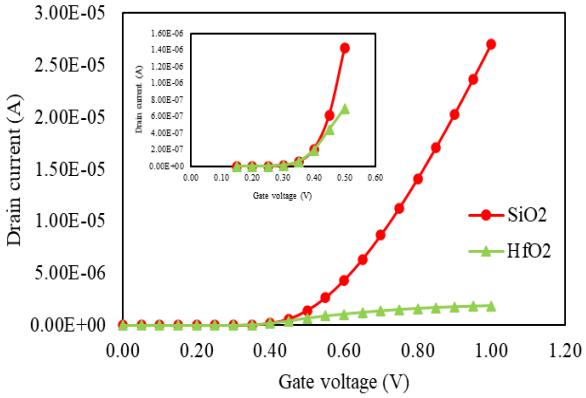

Fig. 10. Comparison of I_D-V_D graph for SiO_2 and HfO_2 at L_g is 0.8um

Figure 11 and fig.12 illustrates I_D-V_G graph when L_g was varied for MOSFET structure using SiO_2 and HfO_2 respectively. From this graph, it clearly shows linear and saturation region. As L_g decreased, distance between drain and source and drain to channel are also reduce. Modulation of the L_g ensures that the saturation region marginally decreases as the drain to source voltage rises. Both I_D-V_D graph for MOSFET with SiO_2 and HfO_2, it clearly shows that both device with shorter channel suffers more from channel modulation effect [18]. MOSFET with HfO_2 and Ge has lower channel length modulation effect as compare to MOSFET with SiO_2 and polysilicon.

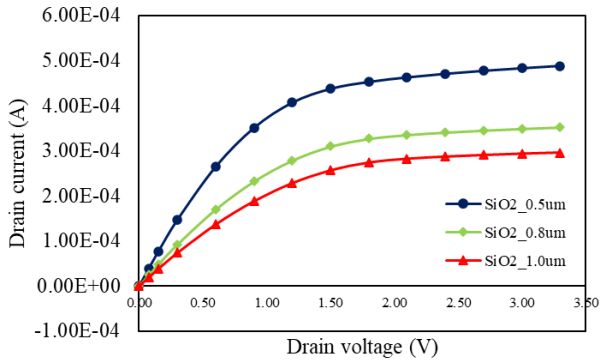

Fig. 11. I_D-V_D for MOSFET structure with SiO_2 when channel length is varies

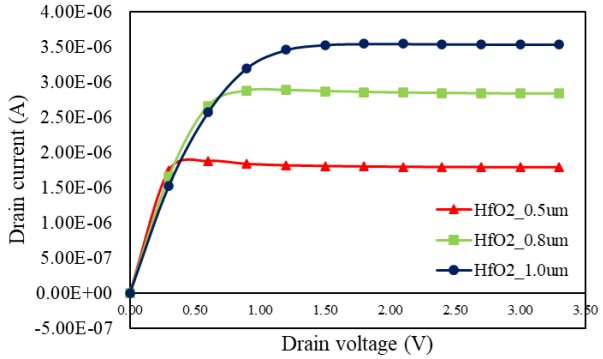

Fig. 12. I_D-V_D MOSFET structure with HfO_2 when channel length is varies.

Gate material engineering increase surface potential in the channel at the contact of two metals which makes the field to reallocate at the drain end [18]. According to Fig. 12, the drain bias voltage, V_D has no significant effect on the inversion layer hence no channel length modulation effect is observed in the device structure [18]. Reducing the L_g width affect V_{th} and I_{OFF} because both was modulated by the width.

The variation of L_g was fabricate and the data has been recorded in Table 5. Table 5 illustrate the comparison reading for SiO_2 and HfO_2 where shorter gate length has highest I_{OFF} for SiO2 structure while for shorter gate length of HfO_2 structure has smallest I_{OFF}. Besides, it also shows that the present of high-k material and lower energy bandgap of metal has changed device performance. High-k device has lower I_{OFF}, smaller V_{th} and smaller *subvt*. Thus, SCEs was control by using HfO_2 as dielectric gate and Ge as gate. The relationship between L_g and V_{th} shows that, shorter L_g affect smallest value of V_{th}. The charge in depletion region was support by drain and source. Meanwhile, charge support in gate region decrease and it reduce V_{th} value. V_{th} decrease with reduction in L_g hence reduce *subvt*. On the other hand, the relationship between L_g, I_{OFF} for SiO_2 structure indicates that the shorter the channel length, it has higher I_{OFF}. The short MOSFET channel required lower energy supply to reduce electrical domains internally and power consumption [13]. A smallest I_{OFF} should be maintained to minimize the static power of a circuit. Shrinking the channel length on HfO_2 MOSFET has smaller I_{OFF} compare to SiO_2.

TABLE V
COMPARISON OF MOSFET PERFROMANCE WHEN CHANNEL LENGTH VARIES

	SiO_2			HFO_2		
Lg (nm)	0.5	0.8	1.0	0.5	0.8	1.0
V_{th} (V)	0.3207	0.3548	0.3654	0.1029	0.1133	0.1191
Subvt (mV/dec)	0.0905	0.0823	0.0809	0.0753	0.0747	0.0750
I_{ON} ($x10^{-6}$ A/cm)	43.8	27	21.5	1.89	1.88	1.63
I_{OFF} ($x10^{-12}$ A/cm)	144	115	126	48.6	61.6	69.4
I_{ON}/I_{OFF} ($x10^{6}$)	0.311	0.235	0.171	0.0389	0.0305	0.0235

IV. CONCLUSION

MOSFET structure was successfully design in Silvaco TCAD tool using different type of high-k dielectric material. Fast switching device need higher value of I_{ON} and it can be obtained from HfO_2 structure that has dielectric constant k=22 bigger than SiO_2 with k=3.9. Hence, HfO_2 was choose as new dielectric material that qualified to reduce SCEs. The variation of polysilicon and Ge able to control SCEs due to a decrement in leakage current by a factor of 0.55. On the other hand, thinner oxide layer and shorter gate length lead to SCEs. Reducing the size of structure can still enhance MOSFET performance in V_{th}, I_{OFF} and I-V characteristics. This is because SCEs was reduced in HfO_2 structure and the result show it has smaller V_{th} and I_{OFF} in comparisons with conventional structure. Therefore, material

with high-k material such as HfO_2 is suitable to combine with lower energy bandgap metal, Ge to produce smaller size of MOSFET with high efficiency performance. This proved that material with highest dielectric constant than HfO_2 and metal with lower energy bandgap are suggested for future study as it can reduce SCEs.

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