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FINAL REPORT OF DIPLOMA PROJECT

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DARKNESS CONTROLLED LIGHT
SWITCH

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1.1 ABSTRACT.

Our project is 'darkness control light switch'. Dark Controller Light Switch is a circuit that used to ON and OFF the switch automatically depend on the light. Generally, this circuit is used in the street light at the building light also in the light at the garden where it can ON and OFF automatically. These project circuits use a basic electronic device such as integrated circuit, light dependent resistance, relay, transistor, diodes and resistance. This circuit needs to connect lamp where AC supply to the lightning load is thus connected via the contact of the relay.

The main future of this project is to switch ON and OFF the street light automatically without human control. So, we can save the time and electricity for this application. As a result, Darkness Control Light Switch is useful for the future e application such as to control street light, building light or the other equipment.

1.2 ACKNOWLEDGEMENT.

In the name of ALLAH S.W.T, the gracious of merciful, syukur alhamdulillah thanks to ALLAH because we can finish our project successfully. Thanks because give us energy and strength also the opportunity to complete this project. We would like to thank to our project supervisor Puan Tuan Shahirah for this consistent advice, sharing in valuable knowledge and guidance as well as provision of their valuable time, encouragement and patient with our problem.

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2.0 THEORETICAL BACKGROUND

2.1 INTERGRATED CIRCUITS

2.1.1 ICI CD 4060 (14-stage binary ripple counter with oscillator)

Features

- All active component on chip
- RC for crystal oscillator configuration
- Output capability : standard (except for RTC and CTC)
- ICC category :MSI

General Description

The 74HC/HCT4060 are high speed Si-gate CMOS devices and are pin compatible with “4000B” series. They are specified in compliance with JEDEC standard no.7A.

The 74HC/ HCT4060 are 14-stage ripple-carry counter/dividers and oscillator with three Oscillator terminals (RS, RTC and CTC), ten buffered output (Q3 to Q9 and Q11 to Q13) And an overriding asynchronous master reset (MR).