A Generation Of Transmitter Signal For 16-PSK STBC MIMO On FPGA Based Polarizone Testbed

Mohd Naim Bin Ab Kassim 2011374999
Faculty of Electrical Engineering
Universiti Teknologi MARA
40450 Shah Alam, Selangor Darul Ehsan.

Associate Prof. Dr. Nur Idora Abdul Razak
Faculty of Electrical Engineering
Universiti Teknologi MARA
40450 Shah Alam, Selangor Darul Ehsan.

***Abstract*—This research focusing on implementation of actual experiments of FPGA board for analysis of multiple input multiple outputs (MIMO) on Space Time Block Code (STBC) scheme. Current research show that STBC is efficient to decrease the distortion effect in transmission system by provide diversity. STBC is known as a technique to transmit redundancy signal through multiple antenna and received various signal data with consistency of data transfer. In this research, Alamouti scheme will be implemented on a FPGA Testbed by Polarizone. Modulation scheme of 16 PSK with two number of transmitting antenna is implemented.**

Keywords—FPGA, STBC, Polarizone Testbed, Alamouti scheme, 16 PSK

I. INTRODUCTION

STBC is a MIMO transmit approach which exploits transmit diversity and high consistency. It is a simple scheme, which very effective ways to get transmit diversity when others forms of diversity might be limited or unreal. Codes are generate at multiple receive antennas, provide receive and transmit diversity. This scheme can also be decoded at receiver through simple linear method of received signals at different receive antennas [1].

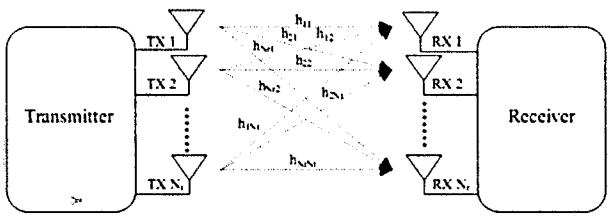

Fig. 1. Multiple Antennas use for Space Time Block Coding.

In order to transmit multiple redundancy of signal through multiple antennas, STBC method is used. The transmitted signal will facing scattering, refraction, reflection and few spoiled scenario condition with the hope that one or more received redundancy of data will be having less distortion than others. This will results a higher chances for data to be decoded properly [2].

The year is 1998, [1] Alamouti designed the simplest scheme of STBC. It is called as the coding matrix:-

$$S = \begin{bmatrix} s1 & s2 \\ -s2^* & s1^* \end{bmatrix} \quad (1)$$

* is a complex conjugate.

TABLE I. ENCODING PROCESS OF ALAMOUTI SCHEME.

	Time Slot 1	Time Slot 2
Antenna 1	$s1 = I_1 + Q_1$	$-s2^* = -I_2 + Q_2$
Antenna 2	$s2 = I_2 + Q_2$	$s1^* = I_1 - Q_1$

As can be seen in Table 1, two time slots is required to transmit two symbols. This result a great orthogonality between symbols. This scheme provide full diversity gain and full transmission data rate.

Type of board used for this implementation is WIMAX BASE BAND Board (DUAL MAX-PRO V464X) realised with VIRTEX-4 FX FPGA by Polarizone. The language is coded manually using Verilog Hardware Description Language (VHDL) programs and implemented them using the software Xilinx ISE 14.2 [3], [4].

Digital baseband data can be achieve by varying the phase of radio frequency carrier. This modulation technique is known as MPSK. In this modulation signalling scheme, it may send one of M possible signals *s1(t),s2(t)...sm(t),* during each signalling interval of duration Ts. For almost all applications, the number of possible signals $M=2n$, where n is an integer. The symbol duration $Ts=nTb$, where Tb is the bit duration. In pass-band data transmission these signals are generated by changing the phase of a sinusoidal carrier in M discrete steps thus we have MPSK modulation schemes. There are only two basis signals, which indicate the constellation of MPSK is two dimensional. From Figure 2 below, MPSK is a constant envelop signal when no pulse shaping is used. This diagram provides a graphical representation of the complex envelop of each possible symbol state. The x-axis represents in-phase component of the complex envelop and the y-axis represents the quadrature components of the complex envelop [5].

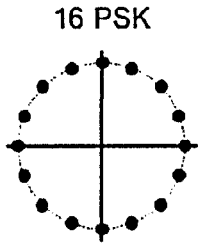

Fig. 2. Constellation diagram of 16 PSK.

The objective of this research is to design the Encoder Register Transfer Level (RTL) STBC using an Alamouti scheme system of transmitter with two antennas for 16 PSK modulation technique on Polarizone FPGA Testbed.

II. PROBLEM STATEMENT

All the review paper from previous researcher, which relate to FPGA hardware research had been constructed to performance simulation based on different coding algorithm, modulation and channel estimation, but most of them have not been tested and evaluate on real MIMO testbed with radio frequency transmission. Their researches for Alamouti's STBC here are mostly only on MATLAB simulation and coding it to VHDL using synthesis tools before simulate it using FPGA hardware. In order to optimized to perform DSP oriented mathematical, recent FPGA are equipped with DSP block. The function of this DSP block is to translate Register Transfer Level (RTL) design and this design is compared to MATLAB input in order to verify its correctness.

Motivated by all researchers studies, especially by Tarokh in [6], Hamid Jafarkhani in [7], D. B. S. P.Sindhu, K.Hari Kishore in [8], and M. T. I. Mostafa Wasiuddin Numanl in [9] it can be say that there is a research gap where this research is focus to explore on MIMO STBC and its implementation on MIMO testbed.

III. RESEARCH METHODOLOGY

There are three methodology that will be used in this research in order to implement Alamouti's scheme with two system of transmitter antennas for 16 PSK modulation technique on Polarizone FPGA Testbed ;-

A. Flow Chart

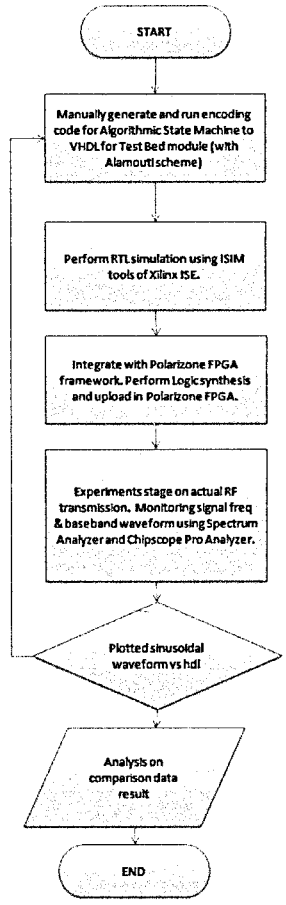

Fig. 3. Flow chart process.

Figure 3 showing a general process of flow chart for this research. The first process is started by manually generate and run the encoding code for algorithmic state machine to VHDL for testbed module with alamouti scheme. Next process is to perform RTL simulation using ISIM tool and integrate it with polarizone FPGA framework before perform logic synthesis and upload it in Polarizone FPGA board. For experiment stage of actual radio frequency transmission, monitoring on signal frequency and baseband waveform is being done here using Spectrum and Chipscope Pro Analyzer. Lastly, once the output waveform is obtain, the comparison will be done between hdl simulation (binary form) versus actual radio frequency waveform acquired from Chipscope Pro Analyzer.

B. Coding tools using Xilinx ISE 14.2

Xilinx ISE system is used to create a program for simulation purpose before implement digitally on FPGA board [10]. In this case, this program is use mainly for verification process by using the program ISIM tools as to perform the RTL simulation in order to integrate the system with polarizone FPGA framework, and run the Chipscope Pro Analyzer as to view waveform behavioural of VHDL code.

C. Encoder RTL Design for STBC

High level architecture is illustrated in figure 6. Its represent the STBC encoding system which receive buffer of eight bit input. For 16 PSK symbol, each byte of data are split into two unit of four bit vector and each four bit is converted to 16 PSK symbol following binary value and PSK constellation point. Constellation point binary illustration will depend on the DAC that is used in the MIMO setup. *s1* and *s2* of I and Q value is set for 16 PSK constellation points. This set of values for two time slots is further encoded by Alamouti encoder.

The output from encoder is scheduled for two time slots and values is send to DAC. The DAC will determine the appropriate value in PSK module; i.e. bit width, value constellation point and etc.

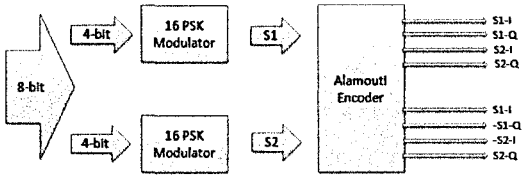

Fig. 6. 16 PSK Alamouti Block Level Architecture.

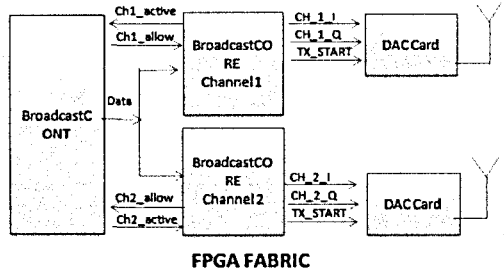

Fig. 7. 16 PSK Alamouti Encoder System Level Architecture.

Referring to figure 7, FPGA system which connected to four units of maxim card or antenna modules is provided in testbed system for baseband processing. As for this research, the system design is limited to two units of antenna modules. FPGA board is connected to RF modules which consists of Digital-to-Analog Converter (DAC) and antennas. Register Transfer Level (RTL) design is implemented inside FPGA fabric for Alamouti encoding.

There are three main components inside the FPGA fabrics;

i) BroadcastCONT.

ii) BroadcastCORE for Channel 1.

iii) BroadcastCORE for Channel 2.

RESET and synchronization between all modules is another important aspects in this design. Alamouti concept for encoding is where all modules can be controlled by reset signal and all are synchronized to the same clock signal. It required two time slots for RF transmission and the timing for two channel must be the same. BroascastCONT only functions as data provider for all channels in the form of eight bit counter it is locally generated inside the FPGA itself. BroadcastCORE for Channel 1 and BroadcastCORE for Channel 2 is a baseband processor for each antenna module. It encode data which come from BroadcastCONT and schedule it for transmission in two time slots accordingly. 16 PSK symbol mapping or bit pattern is perform from four bit binary data to each of its corresponding sinusoidal waveform of I and Q value for each channel. The amplitude (for PSK modulation, the amplitude is design to stay at 100% maximum of utilization from DAC card) and phase of sample points in sinusoidal wave is sent to DAC module for carrier modulation. Different sampling points is sent with different bit pattern.

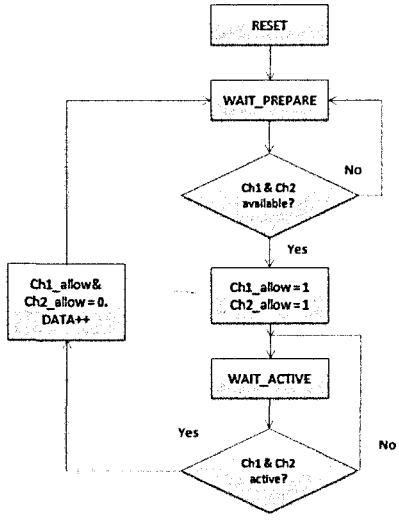

Fig. 8. Algorithmic State Machine for BroadcastCONT.

Figure 8 showing the behaviour of BroadcastCONT described in Algorithmic State Machine (ASM) notation. At WAIT_PREPARE state, system will waits for the readiness flag of Channel 1 and Channel 2. If both channels are active, it will keep looping to the same state. Once the BroadcastCORE for channel 1 and channel 2 flag is ready, state transition will started from WAIT_PREPARE state to WAIT_ACTIVE state and BroadcastCONT will allow signal to activate BroadcastCORE. At WAIT_ACTIVE state, it waits until both channels are active for state transition to WAIT_PREPARE state, otherwise it loops at the same state.

Figure 9 showing the behaviour of BroadcastCORE for channel 1 in the form of ASM notation. It will transits to PREPARE state once RESET and INITIALIZE for synchronization ; waiting for allow signal from BroadcastCONT. BroadcastCORE for Channel 1 are waiting for Ch1_allow signal to arrive. Once arrive, state transition will change from PREPARE state to ACTIVE state.

At ACTIVE state, BroadcastCORE must operate according to Alamouti encoding scheme. During time slot 1, BroadcastCORE for Channel 1 modulates the carrier signal by sending 32 sample points to DAC card, both for I and Q channel through data generation process (refer figure 10). The DAC card modulates this carrier signal according to the value of the sample point received. The same behaviour of channel 1 is apply to channel 2.

The process at time slot 1 is for 32 clock cycles. At time slot 1, BroadcastCORE for Channel 1 and BroadcastCORE for Channel 2 will send (I_1+Q_1) and (I_2+Q_2) respectively. At time slot 2, BroadcastCORE for Channel 1 and BroadcastCORE for Channel 2 will send $(-I_2 + Q_2)$ and (I_1-Q_1) respectively. Result of this transmission is shown at result section.

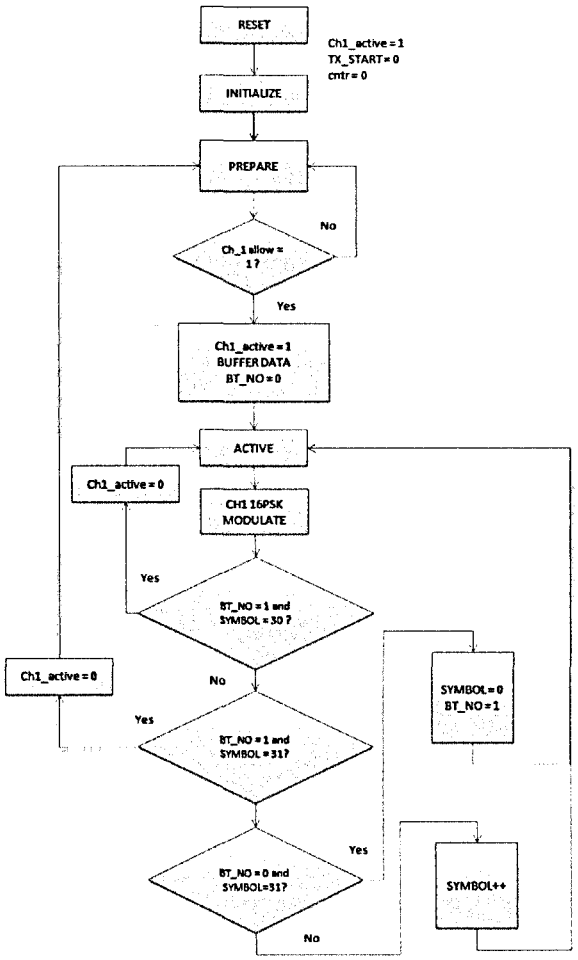

Fig. 9. Algorithmic State Machine for BroadcastCORE channel 1 (modulate waveform).

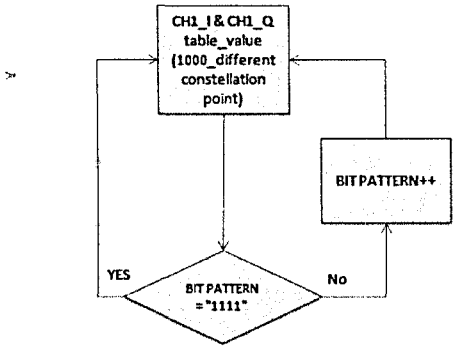

Fig. 10. Channel 1, 16 PSK input data generator module.

IV. RESULTS

A. Output waveform from the Transmission Encoder acquired randomly from Chipscope Pro Analyzer;-

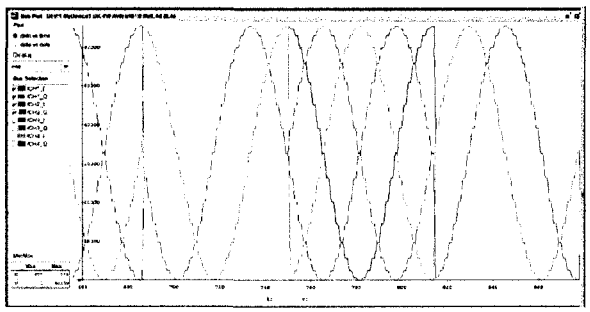

Fig. 11. I and Q for Channel 1 and 2.

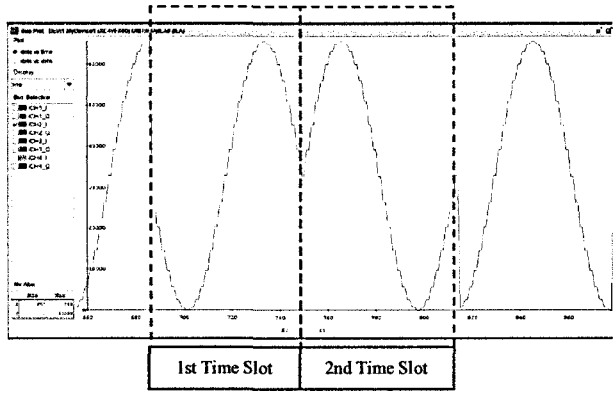

Fig. 12. I for channel 2 waveform start at 180° constellation point.

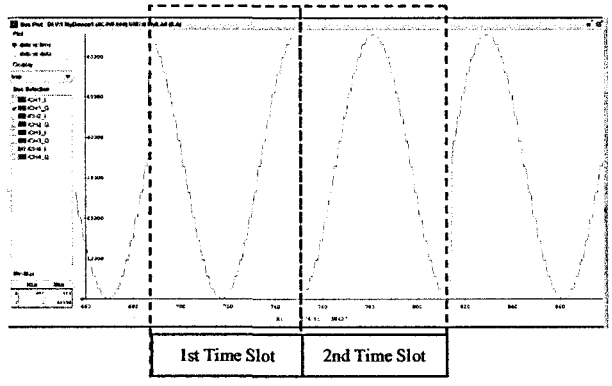

Fig. 13. Q for channel 1 waveform start at 90° constellation point.

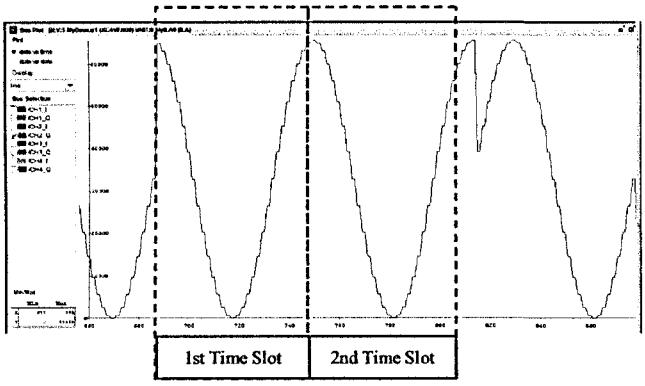

Fig. 14. Q for Channel 2 waveform start at 90° constellation point.

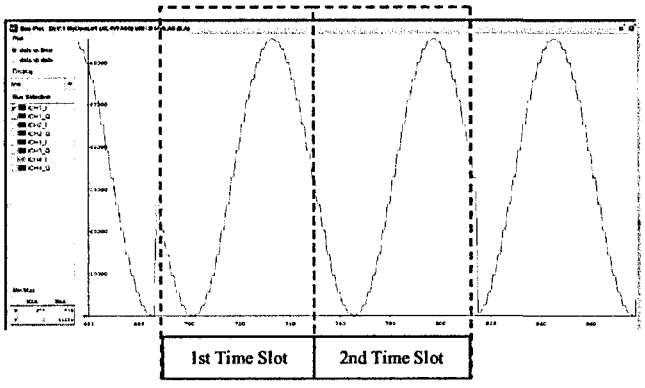

Fig. 15. I for Channel 1 waveform started at 203° constellation point.

Figure 11, 12, 13, 14 and 15 is randomly acquired from Chipscope Pro Analyzer. The data input generation (from 0000 until 1111 of binary value) is set to produce 16 pattern of waveform from 16 constellation point (from 0° until 338°) . It had shown the baseband waveform as expected. During certain time slot between I and Q, result will showing the same or reflected pattern of waveform output accordingly following the algorithmic of Alamouti encoding scheme which discussed in research methodology section on Encoder RTL Design for STBC.

B. Comparison result between HDL simulation in binary form and actual waveform acquired from Chipscope Pro Analyzer.

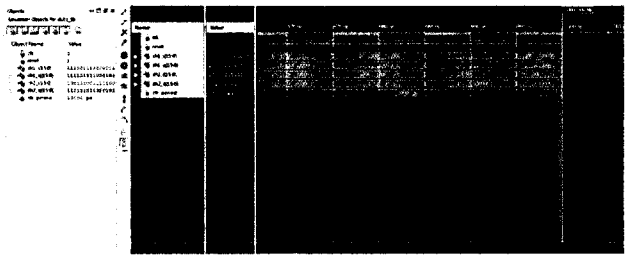

Fig. 16. HDL Simulation in binary form for data input generation 0000 and 0001.

The alamouti transmitter is designed to operate at the same clock speed as the data rate of the FPGA, so one clock cycle is assumed to be one symbol period. Therefore, two clock cycles are needed to encode two symbols and the resulted output waveforms are shown in Figure 16.

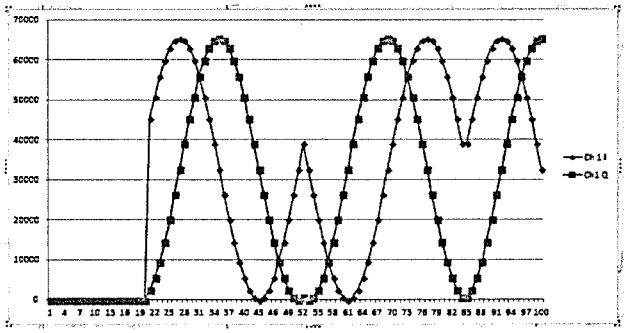

Fig. 17. HDL simulation result Channel 1 for I and Q, manually plotted in waveform pattern for data input generation 0000 and 0001.

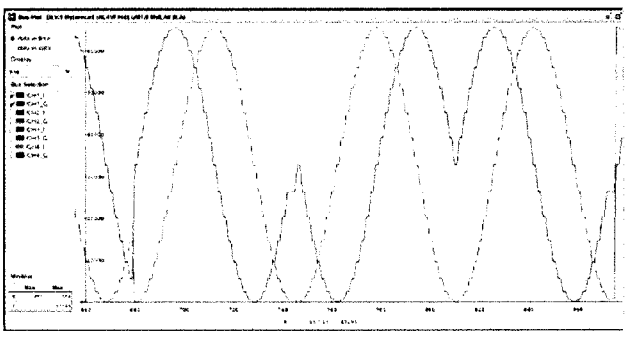

Fig. 18. Actual waveform result Channel 1 for I and Q, acquired from Chipscope Pro Analyzer for data input generation 0000 and 0001.

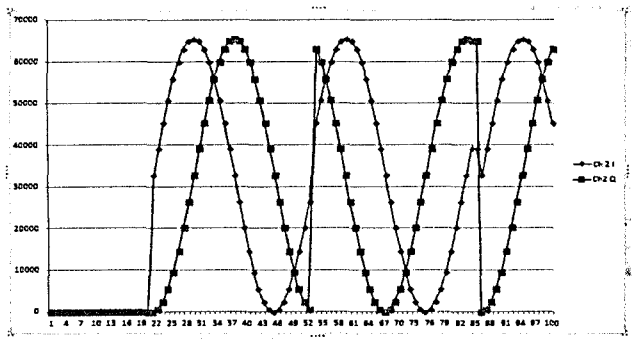

Fig. 19. HDL simulation result Channel 2 for I and Q, manually plotted in waveform pattern for data input generation 0000 and 0001.

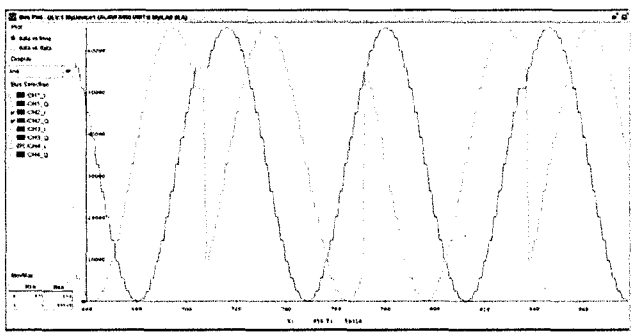

Fig. 20. Actual waveform result Channel 2 for I and Q, acquired from Chipscope Pro Analyzer for data input generation 0000 and 0001.

For verification purpose, Channel 1 and 2 for I and Q of input generation 0000 and 0001 had been selected by showing the comparison between hdl simulation and actual radio frequency waveform results. Figure 17 and 19 showing a results of manually plotted waveform acquired from binary form of hdl simulation, while figure 18 and 20 showing actual radio frequency waveform acquired from Chipscope Pro Analyzer. The comparison showing the same pattern waveform as expected.

C. Output results of constellation diagram.

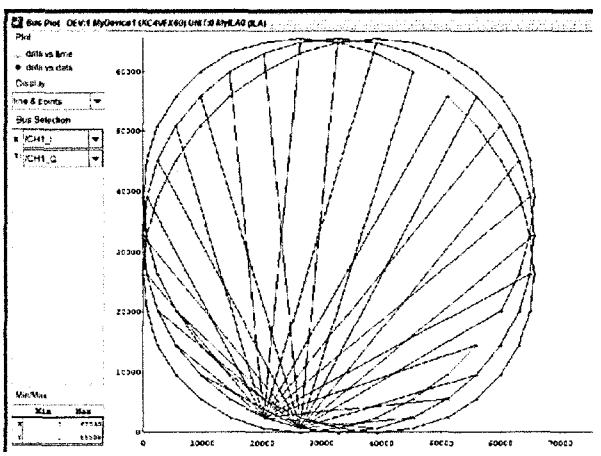

Fig. 19. Example of constellation diagram 16 PSK digitally plotted by Chipscope Pro Analyzer.

Figure 19 showing an example of constellation diagram acquired from Chipscope Pro Analyzer. This data is digitally generate randomly for 32 sample points with two time slot on each sample and the pattern form will change from sample to sample depending on the signal its receive from data input generation.

V. FUTURE WORK

The completion of this research is able to achieve on encode of incoming data from the data generator module and produce baseband waveform accordingly. This research can be further expand until decoder RTL design for STBC. As for decoder, some sub-modules such as "symbol estimator" and "correlator" can be consider in the design, but this requires a lot of integration work with Polarizone platform. Many things regarding the communication with ADC module is required to be explored.

In this research, the Chipscope Pro Analyzer only able to show a result of constellation diagram in a digital form (figure 19). For better plotting diagram, it is recommended to use oscilloscope and capture it in analog form from the output I and Q of testbed.

VI. CONCLUSION

This research presenting a generation of transmitter signal for 16-PSK STBC MIMO on FPGA based Polarizone Testbed. It involve FPGA board with actual MIMO's radio frequency transmission experiments. The Alamouti encoder and decoder is designed and verified by previous paper researcher such as Tarokh in [6], Hamid Jafarkhani in [7], D. B. S. P.Sindhu, K.Hari Kishore in [8] and M. T. I. Mostafa Wasiuddin Numanl in [9]. Their design concept is implemented and extend to this research in actual FPGA board for MIMO's radio frequency transmission on Polarizone Testbed.

Key contributions that had been made to this project are design for encode on incoming data generator module and produce baseband waveform accordingly on MIMO system through;-

- Exploring on 16 PSK Alamouti Block level and Encoder System Level Architecture.
- Writing the behaviour of algorithmic State Machine VHDL code as to implement these designs on Alamouti scheme system with two of transmitter antennas for 16 PSK modulation technique.

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