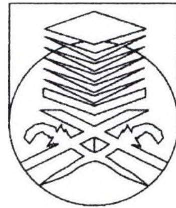
HIGH LEVEL SYNTHESIS FOR PARALLEL SCAN



INSTITUT PENGURUSAN PENYELIDIKAN
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM, SELANGOR
MALAYSIA

BY :

RIHANA YUSUF
NORSABRINA SIHAB
ZURITA ZULKIFLI

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ABSTRACT

As digital systems become more complex, they become much harder and expensive to test. One solution to this problem is to add logic to the Integrated Circuit (IC) so that it can be testable. This concept is an important aspect to be considered in early stage of IC design process. This is different from traditional test philosophy, where the testing is carried out after the IC design has been completed. In this paper, the scan-based architecture which is widely used in modern design for testing purpose will be employed in testing the IC circuit. However, the applicability of scan testing is being severely challenged recently by four problems which are area overhead, test application time, power consumption, and test-related yield loss. This project addresses the issue of reducing test application time using a parallel scan method in which the test vector has parallel loading and unloading sequence mechanism that can shorten the test application time. A 2-bit Full Adder circuit is utilized as a Circuit Under Test (CUT) while the VHSIC Hardware Description Language (VHDL) is used as a tool to design the whole system and will be run on MAX+plus II platform.