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Design of Gate Driver and Comparative Performance Evaluation of GaN vs. Silicon MOSFETs in Buck Converters

Mir Ahmad Fikry Faudzi, Wan Fazlida Abdullah*, Siti Amalina Enche Ab Rahim, Maxime Morenas, Lim Zi Xin, and Salleh Ahmad

***Abstract*— Gallium Nitride (GaN) devices enable high-frequency and high-efficiency operation in modern DC-DC converters, but their fast switching speeds and strict gate voltage limits require dedicated gate driver architectures. This paper presents the design of a specialized GaN gate driver for buck converter applications, featuring an integrated level shifter, bootstrap circuit, dead-time control, and high-speed output stage. Beyond the driver design, this study specifically evaluates the impact of replacing traditional Silicon (Si) power MOSFETs with GaN High Electron Mobility Transistors (HEMTs). Simulation and experimental results verify stable high-side operation and precise gate-to-source voltage control. Comparative analysis demonstrates that the GaN-based system, supported by the proposed driver, significantly outperforms the Silicon baseline in terms of efficiency and switching speed. The results validate the design's suitability for high-performance, high-density power conversion where traditional Silicon reaches its physical limits.**

***Index Terms*—buck converter, dc-dc converter, GaN driver, fast switching, wide bandgap.**

I. INTRODUCTION

DC-DC converter is defined as to translate from different voltage levels to supply to the other voltage levels either from low voltage to high voltage domain (boost converter), high voltage to low voltage domain(buck converter), and both (buck-boost converter) using silicon (Si) power MOSFETs, operating in switching mode to achieve high efficiency. However, silicon devices face its limit [1] with performance degradation at high switching frequencies [2] due to relatively large parasitic capacitances, which increase switching losses [1], [2] and limit switching speed. To address these limitations, wide bandgap devices such as Gallium Nitride (GaN) have gained attention, offering a wider bandgap energy (approximately 3.4 eV compared to 1.1 eV for silicon), lower parasitic capacitances [3], faster switching capability [4], and reduced switching losses [4], [5], making them well suited for high-frequency [5], high-efficiency power conversion. Because GaN power transistors have different gate characteristics, tighter gate voltage limits, and very fast dv/dt [6]and di/dt transitions, a dedicated gate driver is essential [4] to provide precise voltage and current control for reliable turn-on and turn-off [7] and fast charging and discharging [8] while minimizing noise, ringing, false triggering, and more challenge [3]. Therefore, this paper focuses on to replace silicon MOSFET with the GaN MOSFET and the design of a GaN gate driver capable of effectively controlling GaN power transistors in high-performance DC-DC converter.

A. Swithing Loss and Converter Effieciency

By replacing silicon power MOSFET with the GaN power MOSFET could help in reducing the switching loss at high frequency [9]. Equation (1) refer to the switching loss on the high side. In [10], stated that when the body-diode is activated, the low-side MOSFET activates at the gate voltage. The load current then keeps flowing through the body-diode in the same direction as when the MOSFET is turned off at the gate voltage. The drain voltage stays low as a result. Consequently, there is less switching loss on the low side. Psw is the switching power loss, Vin is the main supply to the power MOSFET, Io is the output current, tr and rf is the rise and fall time, and fsw is the switching frequency.

$$Psw = \frac{1}{2} \times Vin \times Io \times (t_r + t_f) \times fsw \quad (1)$$

Switching loss also could affect the efficiency which when the switching loss is high then the efficiency starts to drop. This also because silicon power MOSFET has high [9] input capacitance, Ciss and output capacitance, Coss. Equation (2) shows that efficiency can be calculated in two ways which is the standard one using output power over the input power while the second one is the loss based form. These shows that as the switching loss increases, efficiency starts to drop.

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$$\eta = \frac{Pout}{Pin} = \frac{Pout}{Pout + Ploss} \quad (2)$$

II. METHODOLOGY

A. General Block Diagram

Fig. 1. shows the block diagram of the GaN's driver that will be designed to drive the GaN power MOSFET (External). These blocks consist of multiple functioning blocks that are used properly for voltage control of the power transistor.

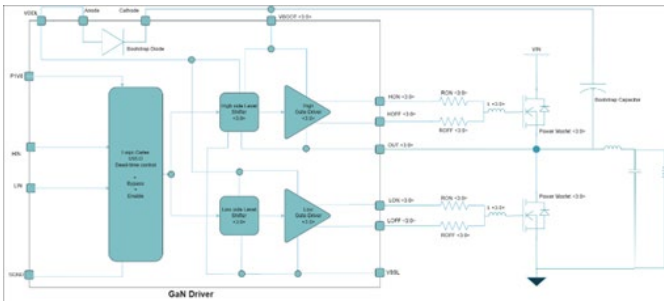

Fig. 1. GaN driver block diagram.

Fig. 2. shows that in GaN driver has two sides which are high side and low side. High side one of the challenges to design compared to the low side due to the referenced floating instead of grounded which means that the reference for the high side is moving [11], [12]. Since the reference also is moving then the high side supply also must be moving so that the gate-source voltage (VGS) is not exceed than the 6V (max) but in this paper will be designed for VGS =5V which fully turn on at the same does not affect the short lifespan of the GaN power MOSFET. This aligns with the engineering practice of not driving at the absolute maximum gate voltage in [13].

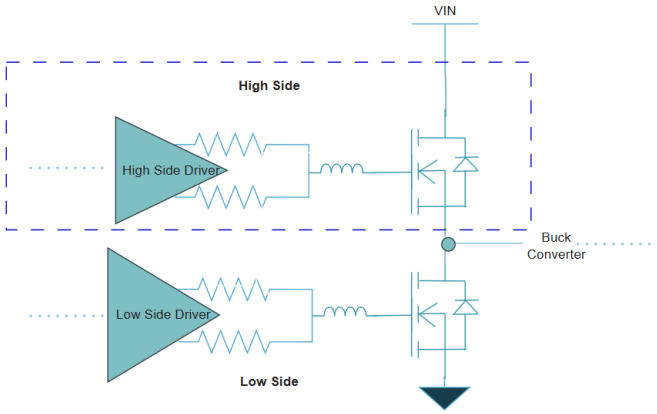

Fig. 2. High side and low side [14].

1) Level Shifter

A level shifter in a GaN driver is a circuit block that safely translates control signals from the low-voltage logic domain (like a controller or PWM chip) to the higher voltage domain which allow different block with varying voltage requirements to communicate safely and effectively especially when working with high side [15]. Fig. 3 shows the quite simple architecture of the level shifter that has its core on level shifter operation called cross coupled which interfaces between low and high voltage levels.

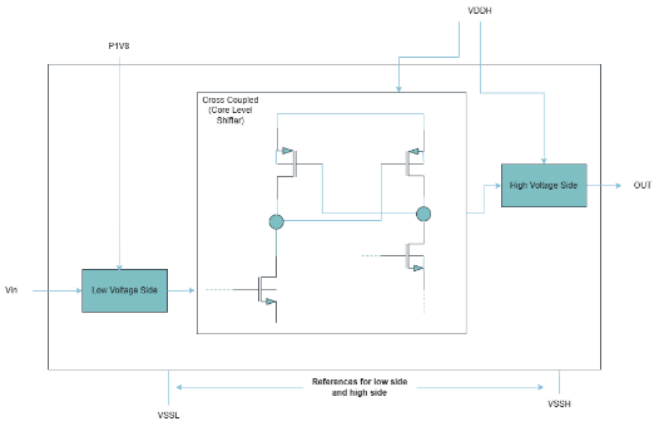

Fig. 3. Block diagram of level shifter.

2) Bootstrap circuit

Bootstrap circuits commonly have bootstrap capacitors and bootstrap diode which the purpose is to create the floating supply for the high side driver. These to ensure that to keep VGS at the correct small value (=5V) relative to the moving source, without exceeding GaN's very tight gate limits. The bootstrap will charge up to VDDL when the high side is off while the low side is on. After that, when the high side supply is turning on, the supply does not respect VDDL anymore instead of VIN (from the primary supply) + VBOOT. From this mechanic the real supply of the high side driver is the difference between the high side supply and the floating reference node (VBOOT-OUT) = VDDL. Fig. 4. shows the simple bootstrap circuit that connected and supplied the high side driver such as high side level shifter and output driver

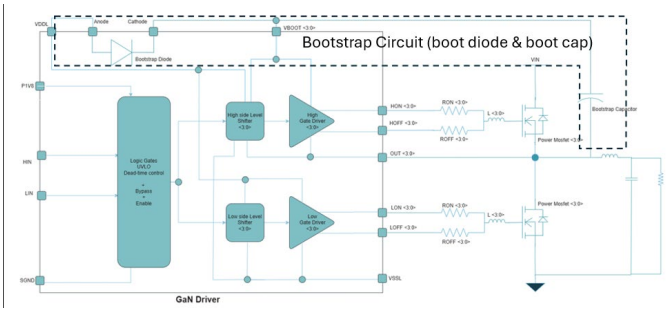

Fig. 4. Bootstrap circuit.

3) Dead-Time Control Block

Dead- Time Control block also one of the important block that needed to ensure that both side do not turn on at the same because it can cause excessive surge of current called shoot-through which a condition where both the high-side and low-side transistors conduct simultaneously, potentially causing excessive current and damaging the devices. Fig. 5. shows the dead time adjustable block diagram that has 6-bit with total of 64 binary number. The block contained multiple delay cell with each cell has 2ns delay and capable to delay the rising edge for both inputs to avoid cross conduction on both high side and low side.

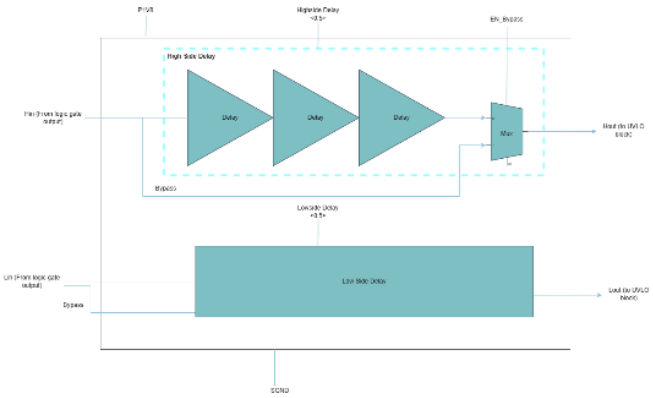

Fig. 5. Deadtime block diagram.

4) Output Driver

The gate driver is the stage that comes just before the GaN power transistor and is responsible for delivering the appropriate signals and provide strong signal drive capability and proper voltage control to the gate of the power MOSFET to ensure proper switching operation [16]. Fig. 6. shows the output driver block diagram which contained buffers using tapering factor method which gradually increase transistor size step by step.

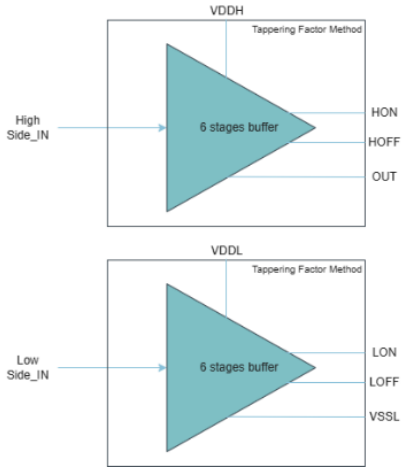

Fig. 6. Output driver block diagram.

5) Other Blocks

By referring to Fig. 1. there are other block like bypass, logic gates, and UVLO. Bypass block diagram is the bypass circuit that has been added to UVLO, dead time control, and logic gate to bypass the block in case it does not work without interrupting normal operation. UVLO is the safety block [17] that will disable the device [18] when the supply falls below its threshold [17] so that, it can avoid the circuit from operating incorrectly or unstable. Other than that, logic gates block, is the first block as the input for both sides entered, also used to protect from shoot-through which both sides turn on at the same time instead of complimentary. It will turn off the device as both input are high and normal operation for complimentary signal.

B. Power MOSFET

This performance simulation utilizes the EPC2111 GaN power MOSFET as the primary device under test, comparing its operational characteristics against three ultra-low-power silicon MOSFETs which are the CSD16301Q2, CSD18540Q5B, and CSD17318Q2 to evaluate the inherent advantages of Gallium Nitride over traditional silicon technology. By implementing these components within a buck converter topology, the study will provide a rigorous comparative analysis focused on critical metrics such as switching speed, and overall conversion efficiency. To accurately facilitate the simulation, the specialized SPICE models for both the GaN and silicon power MOSFETs have been successfully integrated into the Cadence Virtuoso environment. This importation process ensures that the unique physical characteristics of the EPC2111 and the CSD-series devices including their parasitic capacitances and gate charge profiles are precisely represented within the schematic.

III. Results and Discussions

The design was tested with a primary supply input voltage (VIN) of 25 V and a VDDL of 5 V. The GaN power MOSFET model used is based on the EPC2111 device and for the comparison with Si power MOSFETs are CSD-series. The technology node is 180 nm and the inputs on both the low side and high side drivers are 1.8V from the PWM signals.

A. High side supply and references node

Fig. 7. shows the high side supply behavior (VBOOT) which swing from 5V-30V while Fig. 8. shows the high side references floating node (OUT) which from 0-25V. This result shows that the high side signal for both supply and references node behaves correctly because when high side turns off, the supply of the high side is VBOOT=5V while its charging the capacitor. Since the low side is on, OUT will be pulled down to 0V/VSSL/ground, and the real supply will become VBOOT-OUT = 5V. After that, when the high side turns on, the supply at the high side now becomes VIN+VBOOT=30V while OUT will become 25V which makes the real supply remain at 5V. The results also for the VBOOT when high side turn on is precisely around 4.6V- approximately 30V which makes the VGS of the transistor inside the block is around 4.6V which is good and acceptable as long as it does not go beyond 5V.

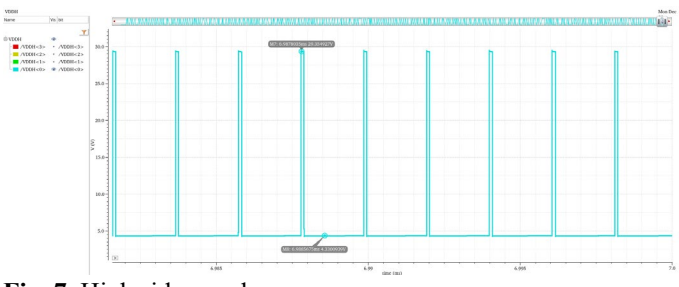

Fig. 7. High side supply.

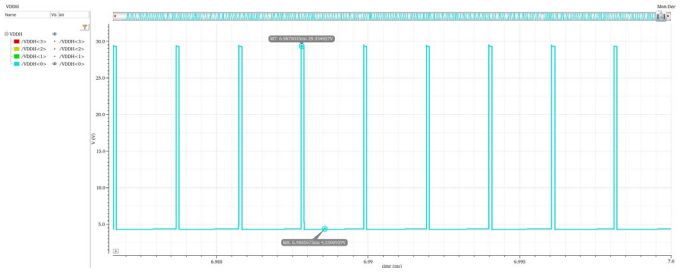

Fig. 8. High side references node.

B. VGS of GaN power MOSFET

Fig. 9. and Fig. 10. shows the VGS for both sides which on the high side results in 0-4.3V while the low side is 0-5V. The low side purely 5V since it fixed to the ground compared to the VGS on high side but 4.3V also is acceptable to fully turn on the GaN power MOSFET.

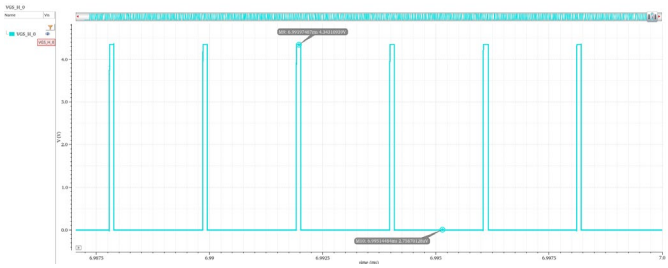

Fig. 9. VGS on high side.

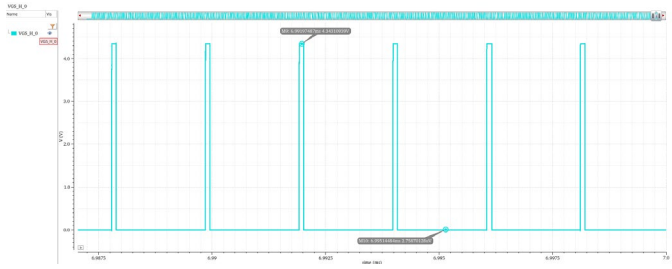

Fig. 10. VGS on low side.

C. Level shifter

Fig. 11. shows the result of the output of the level shifters from 0-1.8V on the high side input from PWM to high voltage level translate of 0-30V. There might be possible questions that said it might destroy the transistors either inside the driver's block and GaN itself with this high gate voltage. The answer is no due to the level shifter not changing the logic information but instead it just translates signal voltage. The VGS amplitude stays same, but the entire signal is shifted upward to ride the floating reference. For the GaN gate when the high side turns on it will be 30V but at the same time its source (OUT) is 25V which has 5V of the effective voltage/real supply. This applied same understanding for the transistors inside the driver.

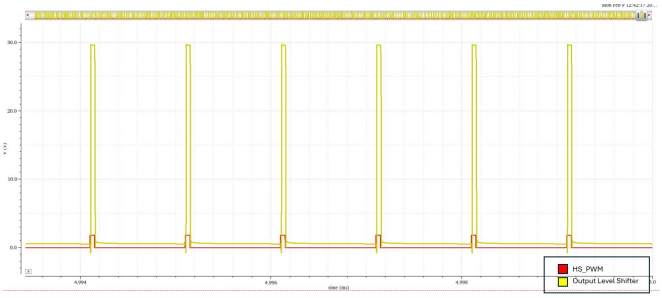

Fig. 11. Level shifter signal.

D. Output of the buck converter

The output converter contained inductor, capacitor, and also resistor for the load. The capacitor, the inductor need proper sizing and same goes to the load resistor using ohm's law. (3) and (4) shows the formula of inductor and capacitor sizing for buck converter. Vout refers to the output of the buck converter, D is the duty cycle, Fsw is the switching frequency, ΔI is the ripple inductor current which typically is 40% below of the load current and ΔVo is the ripple output voltage which typically is 3% of the output voltage.

$$L = \frac{Vout\ (1-D)}{(Fsw)(\Delta I)} \tag{3}$$

$$C = \frac{\Delta I}{8(Fsw)(\Delta Vo)} \tag{4}$$

Fig. 12. shows the output results of the buck converter based on the design requirements. Overall, both the output voltage and output current meet the specified targets. However, at Vout = 1.2 V and Iout = 13 A, a slightly higher overshoot is observed.

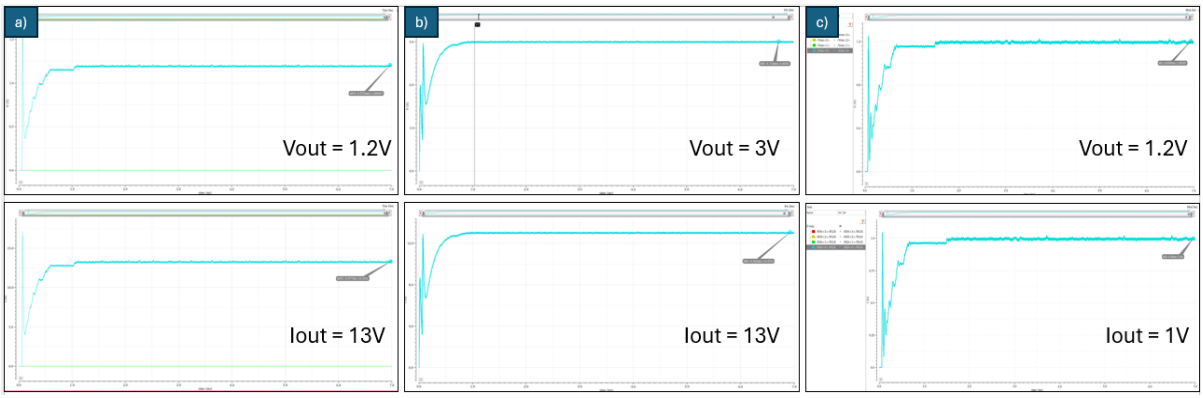

Fig. 12. Output Voltage and current of buck converter: Vout =1.2V and Iout = 13V a), Vout =3V and Iout = 13A b), Vout 1.2V and 1A c).

This overshoot may still be acceptable depending on the user or application requirements.

E. GaN and Si Comparison

1) Switching speed

TABLE I shows the switching speed of the power MOSFETs for both GaN and Si. It can be observed that the rise time and fall time for GaN power MOSFET is lower than the Si power MOSFET which proves that the switching speed for GaN power MOSFET is far greater than the Si power MOSFET. The rise time and fall time for Si MOSFETs around ns while for the GaN MOSFET much less than the Si which is only around ps.

TABLE I
SWITHING SPEED OF RISE TIME AND FALL TIME

MOSFETs	RISE TIME (S)	FALL TIME (S)
Si (CSD18540Q5B)	9n	3n
Si (CSD17318Q)	4.4n	1.7n
Si (CSD16301Q2)	16p	4n
GaN (EPC2111)	594p	719p

2) Converter's Efficiency

TABLE II shows the performance on efficiency that has been tested on GaN and Silicon power MOSFET for Vout = 3V and Iout= 13A on buck converter using 60kHz and 495kHz PWM. a 3% improvement over the CSD17318Q and a 6% advantage over the CSD18540Q5B. When the frequency was increased to 485 kHz, the EPC2111 maintained a high converter efficiency of 91%, sustaining a 3% lead over the CSD17318Q and outperforming the CSD16301Q2 by 5%. Furthermore, an analysis of switching losses confirms the superiority of GaN technology at both low and high frequencies. At 60 kHz, the EPC2111 (GaN) exhibited the lowest switching losses at 12.8 mW, significantly outperforming the Silicon MOSFETs which recorded losses of 17 mW and 50 mW, respectively. This trend intensified at 485 kHz, where the GaN device maintained the lowest loss at 102 mW, while the Silicon alternatives saw their losses climb sharply to 126 mW and 494 mW. These findings confirm that GaN technology provides superior performance and lower power losses in high-frequency applications and the ability to minimize heat dissipation and maintain operational stability in high-speed switching environments. compared to traditional silicon MOSFETs

3) Layout Simulation

Fiq. 13 presents the post-layout simulation results of the driver section, demonstrating that the performance closely matches the pre-layout simulation outcomes. VBOOT is the high side moving supply or also known as VDDH which moves from 5-29V. 5V supply when the high side turn off and charging the capacitor while 29V is VBOOT + VSSH when the high side turn on. The VSSH is the floating references for the high side which is from 0-25V. This is because when the low side turn on the VSSH pulled to the ground (0V) and when the high side turns on the supply VIN flow to VSSH node. The VGSL is the VGS on low side for the GaN power MOSFET which 0-5V where this side is not a problem due to the referenced fix to the ground while VGSH is the VGS of GaN power MOSFET for the high side which is swing form 0 – 4.4V. The analysis reveals

TABLE II
COMPARISON OF GAN AND SI POWER MOSFETS

POWER MOSFET	VIN(V)	VOUT(V)	IOUT(A)	SWITCHING FREQUENCY (HZ)	SWITCHING LOSS (W)	EFFICIENCY (%)
Si (CSD18540Q5B)	25	3	13	60k	17m	87
Si (CSD17318Q)	25	3	13	60k	50m	90
GaN (EPC2111)	25	3	13	60k	12.8m	93
Si (CSD16301Q2)	25	3	13	485k	126m	86
Si (CSD17318Q)	25	3	13	485k	494m	88
GaN (EPC2111)	25	3	13	485k	102m	91

The Silicon MOSFET with ultra-low input and output capacitance has been used in this design. The results demonstrate that the GaN power MOSFET (EPC2111) achieves higher efficiency than silicon-based alternatives, particularly as switching frequencies increase. At a 60 kHz switching frequency, the EPC2111 reached 93% efficiency, representing that the high-side VGS (VGSH) is the most critical parameter compared to the low-side VGS (VGSL) due to its dynamic behavior during operation. Despite it is only 4.4V and not 5V, the results confirm that VGSH remains within safe operating limits, ensuring that the GaN MOSFET is not compromised or destroyed during high-frequency switching. The GateH and

GateL is moving from 0-30V and 0-5V. Regarding the high-side gate voltage (GateH), when the high-side switch is turned off, both GateH and VSSH are 0V, resulting in a difference VGSH of 0V which confirms the off-state. Conversely, when the high-side switch is turned on, the gate voltage (GateH) is determined by the sum of VSSH and the bootstrap voltage VBOOT with VSSH at 25V and a total GateH is 30V, the resulting VGSH is 4.4V, effectively driving the GaN MOSFET into the on-state This consistency indicates that parasitic effects introduced during the layout process, such as routing resistance and capacitance, have been well controlled and do not significantly degrade the circuit behavior. As a result, the driver design can be considered robust and layout accurate. Similarly, in Fig. 14. illustrates the simulated output performance of the buck converter, where the output voltage (Vout) is maintained at 3 V while delivering an output current (Iout) of 13 A. These results confirm that the converter operates as intended under the specified load conditions. Overall, the strong agreement between pre-layout and post-layout simulations, along with the achievement of the desired output specifications, validates that the layout implementation is correct and reliable.

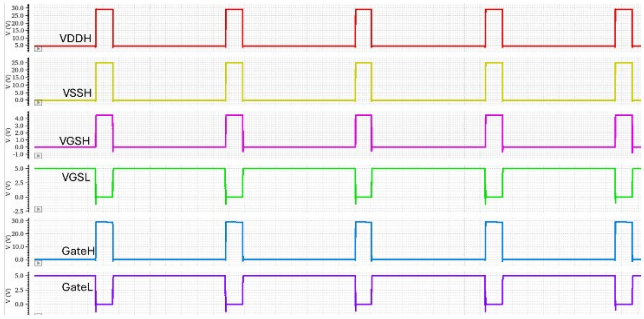

Fig. 13. Driver's parameter for the layout simulation.

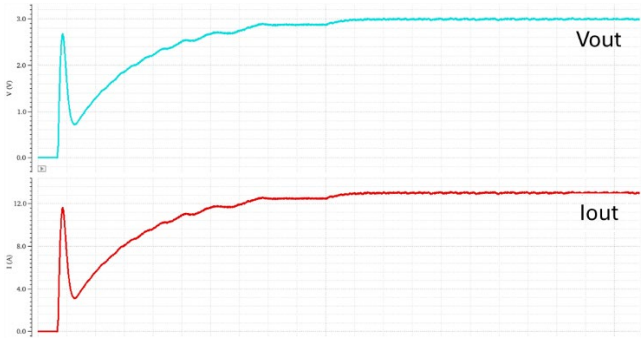

Fig. 14. Buck converter's layout simulation.

IV. Conclusion

The results demonstrate that both the driver's behavior and the buck converter output operate successfully. The system was tested at 485 kHz and also validated at 60 kHz. The gate-to-source voltage (VGS) for both the high-side and low-side switches was successfully maintained below 5 V. Similarly, the supply voltage between VBOOT and OUT remained within a safe range, preventing device damage. These results were obtained without including external gate resistance or parasitic gate inductance. To further ensure reliable operation under practical conditions, additional challenges such as cross-conduction between the switches and high dv/dt effects due to parasitic inductance must be addressed. The efficiency of using GaN power MOSFET is higher than the Silicon power MOSFET especially at high frequency which proved that GaN MOSFET have higher capability on high frequency compared to Silicon MOSFET. The post simulation also has been tested that, the results is work properly as intended same as the pre simulation. Therefore, while the open-loop results demonstrate the feasibility of the design, further validation through closed-loop testing will be carried out to confirm its performance under realistic operating conditions and additional difficulties, including cross-conduction, high dv/dt, and more, while employing GaN power MOSFET in dc-dc converter applications.

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