

UNIVERSITI TEKNOLOGI MARA

**OPTIMIZATION AND MODELING
OF $\text{Si}_{1-x}\text{Ge}_x$ -FINFET STRUCTURE
BASED ON RATIO X, CHANNEL
DIMENSIONS AND WORKING
TEMPERATURE**

YOUSIF ATALLA YOUSIF

PhD

June 2026

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TEMPERATURE**

YOUSIF ATALLA YOUSIF

Thesis submitted in fulfilment
of the requirements for the degree of
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ABSTRACT

The ever-decreasing size of transistors, driven by the Moore Law, has caused serious heat dissipation problems and increased power consumption at the nanoscale. Fin-shaped Field-Effect Transistors (FinFETs) have become an attractive choice since they can be more easily controlled electrically, reduce leakage currents, and be manufactured using existing techniques. At the same time, the classic Complementary Metal-Oxide-Semiconductor (CMOS) technology is nearing its physical limits. Nonetheless, there is a significant concern that can impact the device's accuracy and efficiency, including thermal problems such as self-heating due to low thermal conductivity and a limited device design. In response to these difficulties, this study is designed to evaluate the thermal and electrical characteristics of FinFET transistors developed from silicon-germanium alloys ($\text{Si}_{1-x}\text{Ge}_x$). Specifically, the work investigates how variations in channel length affect the device's response to thermal stress while keeping channel width and oxide thickness fixed. Si-Ge offers promising opportunities to improve thermal sensitivity in nanoscale transistors, due to its ability to form complete solid solutions across the entire composition range and its notable suppression of thermal conductivity. The molar chemical ratios of Si and Ge (such as $\text{Si}_{0.75}/\text{Ge}_{0.25}$ and $\text{Si}_{0.25}/\text{Ge}_{0.75}$) are evaluated to determine performance metrics and determine approaches to improve thermal response as a result of material modification. The MuGFET tool was used to run the simulations at temperatures between 275 and 350 Kelvin. The oxide layer thickness was set to 1 nm, and the channel lengths were 10, 20, and 30 nm. The model included a metal-semiconductor diode junction to improve the accuracy of thermal and electrical predictions. The final results revealed that the ratio ($x = 0.5$) $\text{Si}_{0.5}/\text{Ge}_{0.5}$ yielded good performance, a more balanced state, and improved electrical properties across all tested ratios. In particular, for channel lengths of 20 and 30 nm, these structures and configurations achieved ideal values for both subthreshold slope ($\text{SS} = 93.65$ and 75 mV/decade), drain-induced barrier lowering ($\text{DIBL} = 25.1$ and 4.11 mV/V), and threshold voltage ($V_T = 0.56$ and 0.58 V), respectively. These results indicate excellent electrostatic control and thermal stability. These outcomes were attributed to reduced lattice thermal conductivity, enhanced by alloy scattering and mass disorder, which suppresses phonon transport. The compatibility of $\text{Si}_{1-x}\text{Ge}_x$ with fabrication techniques such as mechanical alloying and spark plasma sintering supports its potential for integration into scalable, thermally aware nano-electronic systems. This study confirms that optimizing both geometric and material parameters enables high-performance, temperature-sensitive nanoscale FinFETs and broadens understanding of $\text{Si}_{1-x}\text{Ge}_x$ behaviour in elevated-temperature environments.

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LIST OF SYMBOLS

Symbols

A	Number Of PLS Or PCA Components In The Model And The Number Of Selected Latent Variables In The Model
a	Number Of The PLS Or PCA Component
b	PLS Regression Coefficient
b	Number Of Blocks ($b = 1, 2, 3, \dots, K$)
C	Coarse APM Block
C_p	Pooled Covariance Matrix For The Two Classes
C_g	Covariance Matrix For Class G
D	Drain
DIBL	Drain-Induced Barrier Lowering
I	Current
I_d	Drain Current
I_{OFF}	OFF Current
I_{ON}	ON Current
K	Scaling Factor
K_B	Boltzmann's Coefficient
L_g	Length Of The Channel
q	Electron Charge
R_{OUT}	Output Resistance

S	Source
SS	Subthreshold Swing
T	Temperature
V_g	Gate Voltage
T_{ox}	Oxide Thickness
V	Voltage
V_d	Drain Voltage
V_{DD}	Drain DC Voltage Source
V_{DS}	Drain To Source Voltage
V_{GS}	Gate To Source Voltage
V_T	Threshold Voltage
ΔL	Effective Channel Length
W_g	Width Of The Channel
T_{fin}	Fin Thickness

LIST OF ABBREVIATIONS

Abbreviations

ALD digital O ₃	Atomic Layer Deposition Using Digital (Pulsed) Ozone As Oxidant
BOX	Buried Oxide
CPU	Central Processing Unit
CLM	Channel Length Modulation
CMOS	Complementary Metal-Oxide-Semiconductor
DELTA	Depleted Lean Channel Transistor
FDSOI	Full-Depleted Si
FDSOI	Depleted Si On Insulator
FET	Field-Effect Transistor
FinFET	Fin-Shaped Field-Effect Transistor
GAA	Gate All Around
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GIDL	Gate-Induced Drain Leakage
IC	Integrated Circuits
InAs	Indium Arsenide
IGFET	Insulated-Gate-Field-Effect Transistor
IGFET	Insulated-Gate-Field-Effect Transistor

I-V	Current-Voltage
IS	Source Current
ID	Drain Current
IGIDL	Increased Gate-Induced Drain Leakage
JFETs	Junction Field-Effect Transistor
LER	Line-Edge Roughness
MESFE	Metal-Semiconductor Field-Effect
MOSFET	Metal-Oxide-Field-Effect Transistor
MuGFET	Multi-Gate-Field-Effect Transistor
NW	Nanowire
PCA	Principal Component Analysis
PDSOI	Partially-Depleted Silicon
PDE	Partial Differential Equation
Rsd	Resistance Source Drain
SOI	Si On Insulator
SCEs	Short Channel Effect
Si	Silicon
SiC	Silicon Carbide
SiNWT	Si Nanowire Transistor
SIT	Static Induction Transistor
VLST-TSA	Technology Systems And Application
VLSI	Very-Large-Scale Integration

Vinj

Effective Carrier Injection Velocity

LIST OF NOMENCLATURES

Nomenclatures

A	Amplitude Ratio (No Units)
C	Centroid of pipe, inches

CHAPTER 1

INTRODUCTION

1.1 Background of the study

Transistors were first used in the 1920s as demand for field-effect device amplification increased. However, a major barrier was the lack of knowledge and understanding regarding the use of semiconductors for this purpose [1]. To this end, scientists began investigating the use of Si in the production of semiconductor materials. These researchers discovered that Si has a property that allows both positive and negative current to flow through Positive-Negative (PN) junctions. The first operational transistor, with enhanced performance and capabilities, was developed and introduced through subsequent research by Shockley, Bardeen, and Brattain. As a result of this discovery, the three scientists from Bell Labs were awarded the prestigious Nobel Prize in Physics.

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is regarded as a fundamental component in the design and manufacturing of electronic circuits, due to its critical role in enabling the transition from analog to digital systems, especially in wireless communication applications. A gate, a source, and a drain are required in the MOSFET configuration. Halfway between the source and the drain is the channel. The gate voltage can be applied by increasing the carrier density in the channel, enabling the flow of electromagnetic current between the electrodes. Applying a voltage to the gate terminal induces the formation of a conductive channel that allows current to flow between the source and drain terminals [2].

Many engineers and researchers have worked diligently to identify a wide range of nanoscale materials based on the Field-Effect Transistor (FET). Its use across a wide range of applications is largely justified by the enhanced properties of the materials used, including lightweight design, exceptional strength, and chemical resistance. The recent extensive use of FET devices in integrated circuits has significantly influenced the design of numerous new electronic tools. Controlling the flow of charges within a semiconductor channel is the fundamental principle behind the operation of a FET, and this flow occurs under the influence of an electric field [3]. A FET consists of a semiconductor channel whose ends are connected to two terminals,

the source and the drain. This configuration controls the flow of current through the channel. The gate is the electrical terminal near the semiconductor channel. The gate of the FET controls the movement of charge carriers from the source to the drain via its electric field. The flow of charge carriers within the semiconductor channel can be controlled by adjusting its geometric dimensions, whether in terms of length, width, or thickness, allowing for precise tuning of conductivity properties [4]. FET structures face fundamental challenges, including increased leakage currents, reduced electrostatic control, and severe side effects as device sizes shrink into the deep nanometre range. These challenges have motivated the transition to multi-gate device architectures, particularly Fin-shaped Field-Effect Transistors (FinFETs), which offer improved gate control by surrounding the channel on multiple sides. Due to their ability to reduce Drain-Induced Barrier Lowering (DIBL) effects, improve subthreshold behaviour compared to planar MOSFETs, and their superior scalability, FinFET structures have become the dominant technology for advanced Complementary Metal-Oxide-Semiconductor (CMOS) nodes [5].

Alongside architectural innovation, material engineering has emerged as a critical factor in enhancing FinFET performance. Development of $\text{Si}_{1-x}\text{Ge}_x$ alloys as channel materials in the FinFET industry has increased, as they offer higher carrier mobility while maintaining compatibility with established CMOS manufacturing processes. The incorporation of Ge into the Si lattice modifies the band structure, enhancing hole and electron transport properties and directly improving drive current and switching speed in nanoscale transistors [6]. Using a Si-Ge mixture provides a balance between thermal reliability and improved mobility, whereas pure germanium suffers from high leakage and thermal instability at elevated temperatures. Therefore, Si-Ge has become suitable for FinFET applications that operate over a wide temperature range [7].

The performance of $\text{Si}_{1-x}\text{Ge}_x$ FinFETs is strongly dependent on the Ge mole fraction (x), channel dimensions, and operating temperature. By varying the carrier confinement and electrostatic behaviour within the channel, the effects of x -ratios on key electrical parameters, such as V_T , SS , and DIBL, were observed. Similarly, channel length scaling plays a decisive role in suppressing short-channel effects, while temperature variations impact carrier mobility, leakage mechanisms, and device stability. Consequently, to achieve an optimal FinFET design, both the material

composition and thermal effects, as well as the geometric gradient, material quality, and conductivity, must be considered jointly and balanced [8].

To accurately analyse these interdependent factors, this work employs the Multi-Gate-Field-Effect Transistor (MuGFET) simulation framework available through nano-HUB. With the development of self-consistent solutions for the Poisson and drift-diffusion equations, MuGFET has become a physics-based, validated tool capable of modelling multi-gate nanoscale transistors. It has been widely validated and adopted in academic research for studying FinFET and nanowire FET behaviour under varying material, dimensional, and thermal conditions [9]. By maintaining computational efficiency, MuGFET enables controlled parametric analysis, making it suitable for exploring improvement trends before experimental manufacturing.

Accordingly, this thesis focuses on the optimization and modelling of $\text{Si}_{1-x}\text{Ge}_x$ FinFET structures by systematically examining the combined effects of Ge composition ratio, channel dimensions, and operating temperature on key electrical performance metrics. The outcomes of this study aim to provide design-level insights that support the development of thermally stable, high-performance FinFET devices for next-generation nano-electronic applications.

1.2 Problem Statement

Guided by Moore's law, the semiconductor industry has pursued aggressive transistor scaling to accommodate more devices per unit area. However, attempts to reduce channel size and length have led to critical challenges, including increased leakage currents even when stopped due to self-conduction. To overcome this challenge, the FinFET technology architecture has been developed as a potential solution that provides better electrostatic control and minimises short-channel effects [5-7]. FinFET transistors employ fins with nanowire-like structures as the conduction path, with the gate electrode surrounding the fins.

Despite these advantages, FinFETs face significant thermal management challenges. The low thermal conductivity of the materials used and the constrained engineering contribute to self-heating, which negatively affects the device's performance in practical applications and its long-term reliability. Optimizing FinFET parameters is thus imperative for achieving robust and thermally stable process technology [12]. Self-Heating Effects (SHE), further exacerbated by shrinking fin sizes,

also impact oxide reliability and performance in Si On Insulator (SOI) and strained-Si technologies with buried oxide (BOX) or Si-Ge (Si-Ge) graded layers [9-10]. The discharge current can deteriorate by up to 15% in extreme cases due to these structures, which increase thermal resistance [11-12].

Due to the growing demand for thermally stable, high-performance nano-electronic devices, it is necessary to understand the behaviour of FinFETs under various thermal and electrical stresses. In this regard, the current research work aims to explore the effect of gate length (L_g) on the thermal and electrical performance of FinFETs with constant gate width (W_g) and gate oxide thickness (T_{ox}). As devices become more sensitive to minor fluctuations in supply voltage and ambient temperature over time, variations in FinFET process parameters during manufacturing introduce uncertainty. These deviations manifest as a gradual increase in power consumption [13-14].

Although prior studies have examined FinFET behaviour under various conditions, they have largely overlooked the sensitivity of Si (Si)-, Ge (Ge)-, and $Si_{1-x}Ge_x$ -based FinFETs to ambient operating temperatures, particularly in the context of nanoscale sensing. The main objective of this thesis is to bridge the gap by demonstrating the suitability of (Si, Ge, $Si_{1-x}Ge_x$) FinFETs for use as nano-temperature sensors. By systematically varying the channel length while keeping the other dimensions fixed, the study isolates the effects of this particular parameter on the thermal and electrical behaviour. In addition, it investigates the effects of the compositional parameter x in $Si_{1-x}Ge_x$ on the structures, advancing the development of more accurate FinFET-based sensing platforms.

1.3 Research Objectives

The specific research objectives are as follows:

- i) To investigate the effect of working temperature on the FinFET channel, reliant on threshold voltage (V_T), subthreshold swing (SS), and drain-induced barrier lowering (DIBL) as limiting factors, using Si, Ge, and $Si_{1-x}Ge_x$ as semiconductors.
- ii) To optimize and minimise FinFET channel dimensions based on V_T , SS, and DIBL as limiting factors using Si, Ge, and $Si_{1-x}Ge_x$ as semiconductors.

- iii) To design a FinFET with Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ as a semiconductor for optimized performance based on electrical and temperature properties.

1.4 Scope and Limitation of Study

The scope of this work is defined into three main stages, concentrating on the design and optimization of (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$)-FinFET channels, taking V_T , SS, and DIBL into account as critical parameters limiting performance:

- i) The first phase investigated the temperature sensitivity and operational stability of (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$)-FinFET structures. Devices were evaluated at four discrete ambient temperatures, 275 K, 300 K, 325 K, and 350 K, to examine the influence of thermal variations on V_T , SS, and DIBL.
- ii) The second phase focused on the dimensional optimization of FinFET architecture. Specifically, the effects of varying channel length ($L_g = 10$ nm, 20 nm, and 30 nm) while maintaining a fixed channel width ($W_g = 10$ nm) and oxide thickness ($T_{ox} = 1$ nm) were analysed to assess their impact on device performance metrics.
- iii) The MuGFET simulation tool for nanoscale MuGFET structures was used in this study.

1.5 Significance of the Study

This study addresses key challenges associated with nanoscale transistor scaling by focusing on the optimization of material composition and device geometry in $\text{Si}_{1-x}\text{Ge}_x$ FinFET structures. Therefore, as devices are reduced in size and distance, and the channel is miniaturized, the challenges related to energy consumption and dissipation, leakage currents, short-channel effects, and the material quality become more important. These factors directly limit performance and long-term reliability.

FinFET layouts are a promising alternative to conventional planar CMOS technology, offering improved electrostatic control and lower leakage current. Nevertheless, thermal issues, such as self-heating due to the compact layout and lower thermal conductivity, remain a significant concern.

Material engineering using $\text{Si}_{1-x}\text{Ge}_x$ alloys plays a central role in this study.

These alloys offer higher carrier mobility than pure silicon while maintaining better thermal reliability than pure Ge. They are suitable for operating FinFETs over a wide range of temperatures, due to their ability to form complete solid solutions across a broad composition range, enabling a tight balance between mobility enhancement and thermal stability.

The impact of Ge mole fraction (x), channel length, and temperature on V_T , SS , and DIBL is investigated. Through maintaining the L_g and T_{ox} constant, the effect of channel length was isolated. The role of scaling in device performance under thermal stress is clearly understood from this study by isolating the impact of channel length. This thesis and research contribute to a deeper understanding of the behaviour of $Si_{1-x}Ge_x$ at high temperatures, making them essential for the development of thermally stable and highly reliable nanodevices. Additionally, by estimating Si-, Ge-, and $Si_{1-x}Ge_x$ -based FinFETs for temperature-sensitive operation, the study supports the possible use of FinFETs in nanoscale thermal sensing applications.

In summary, this study is important as it relates device geometry, material composition, and thermal phenomena within a unified model. This integration enables design-level insights for the development of reliable, high-performance, and thermally robust FinFET technologies for next-generation nano-electronic systems.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

MOSFET, a subtype of FETs, is popular for its high scalability and low noise levels compared to a Bipolar Junction Transistor (BJT) [17]. Unlike a BJT, a MOSFET is a unipolar device, i.e., it can use either electrons or holes as the sole charge carrier, which results in reduced electronic noise and increased signal integrity [18]. Additionally, their planar structure enables the fabrication of a large number of devices on a single Si wafer, making them an ideal fit for high-density integration in modern electronic systems [19]. MOSFETs are very popular in semiconductor and micro-electronic applications, where they act as electronic conduits or signal amplifiers, and their amplification properties underpin the development of digital memory and logic circuits.

At the same time, alloys of $\text{Si}_{1-x}\text{Ge}_x$ have also been identified as promising materials due to their adjustable bandgap and lattice constants [20]. The alloys of $\text{Si}_{1-x}\text{Ge}_x$ form a complete miscible solid solution with a diamond crystal structure and can be epitaxially grown on Si substrates. High-speed microelectronic devices use $\text{Si}_{1-x}\text{Ge}_x$ thin films, and bulk Si-Ge alloys are being considered for X-ray and neutron monochromators, solar cells, and thermoelectric power generation at temperatures up to 1300 K [21]. Especially noteworthy is the use of $\text{Si}_{1-x}\text{Ge}_x$ in deep-space missions, including Voyager and Cassini, where the alloys serve as the core of radioisotope thermoelectric generators to convert the decay energy of plutonium-238 into electricity [22].

Although significant research has been conducted in the field since the 1960s to enhance the thermoelectric characteristics of $\text{Si}_{1-x}\text{Ge}_x$ alloys, few data are known on the quantitative behaviour of carrier mobility at high temperatures. A significant weakness has been the difficulty in producing high-quality, strain-free single crystals of Si-Ge alloys. Recently, the successful development of large, high-purity single crystals across certain compositional domains has been made possible [23].

This chapter presents a concise overview of nanotechnology and its applications in FET development and addresses the associated technical challenges. It discusses the

significance of Moore's Law and recent advancements aimed at reducing transistor dimensions to enhance performance and integration density. The FinFET technology is presented, along with its benefits, and a simplified explanation of the production process is provided. The electrical characteristics of transistors are also described, and the semiconductor materials commonly used in device construction are discussed. A detailed focus is placed on the influence of material composition on FinFET performance, in particular for $\text{Si}_{1-x}\text{Ge}_x$ alloys. In addition, the chapter summarizes the recent literature on the role of scaling down channel dimensions in device behaviour. Finally, the existing research gaps are summarized, outlining the limitations of prior studies and emphasizing the need for further investigation into the combined effects of material composition, structural dimensions, and thermal conditions on FinFET operation.

2.2 Minimization of MOSFET

CMOS (complementary metal-oxide-semiconductor) technology is expected to reduce the number of transistors in each subsequent generation, leading to steady increases in transistor performance. Nonetheless, scaling gate transistor lengths below 22 nm could pose serious problems, including increased sub-threshold leakage, short-channel effects, and device-to-device variations, as stated in the International Technology Roadmap for Semiconductors [24]. Several investigations have sought to address these problems through new transistor architectures, such as Double-Gate FET (DG-FET), FinFET, and Si-nanowire Planar DG-FETs. The difficulty of matching the two gates is addressed by a special form of DG-FET known as a FinFET. The FinFETs are relatively easy to make with no alignment problems that other DG-FET structures have. Furthermore, FinFETs exhibit high resistance to Random Dopant (RD) variations due to their lightly doped channel, as reported in [24].

2.3 Double-gate MOSFET

The schematic of an n-channel DG-FET is displayed in Figure 2.1 [25], where the gate dielectric is illustrated in grey. This structure contains two gates (top and bottom) that control the channel. These settings may lessen short-channel effects by preventing the drain electric field from intruding into the channel. The DG-FET offers

a similar yield in an aggressively scaled standard CMOS technology, reduces leakage, and provides excellent control over short-channel effects [25]. Among the two types of DG-FETs are symmetric DG-FETs, which have two-gate electrode materials with distinct purposes and front- and back-gate dielectric thicknesses.

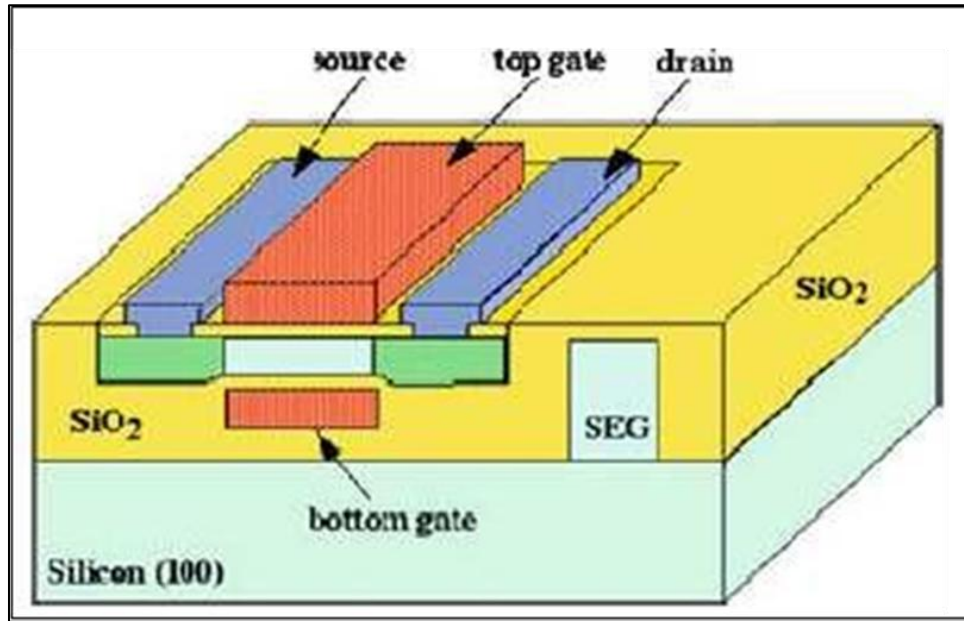


Figure 2.1 DG-FET structure [25].

2.4 Planar CMOS versus FinFET

Short-Channel Effects (SCEs) are becoming more common as device scaling progresses, so precautions must be taken to ensure good device performance for operations below the 50-nm level. Among the methods that have proven increasingly effective in reducing SCEs is the use of FinFET transistors, which feature a symmetrical vertical structure with two gates, unlike traditional planar transistors in CMOS technology. New equations have been developed to accurately describe the current flowing through the channel across different operating modes, including the sub-threshold, linear, and saturation regions. FinFET technologies are distinguished by their ability to reduce the impact of statistical variations in device parameters, resulting from changes in manufacturing processes, temperatures, and voltages, compared to traditional CMOS technologies. Furthermore, vertical double-gate devices greatly improve low-power performance, especially for subthreshold operation [24-25].

Non-traditional architectures, such as devices with multiple independent gates and FinFET transistors, face increasing challenges in maintaining the ongoing miniaturization predicted by Moore's Law. Extreme caution must be used when lowering the minimum gate length below 50 nm in order to minimise undesirable SCEs. Planar CMOS technology encounters fundamental limitations when scaled below 50 nm, including quantum tunneling through the thin gate oxide layer, between the source and drain, and between the drain and the body. Additionally, controlling V_T is challenging since precisely adjusting the doping concentration at this nanoscale is difficult. To overcome these limitations, the FinFET was carefully designed [24-25].

2.5 The Field-Effect Transistor

The credit for the first patents related to the FET goes to Julius Edgar in 1926 and Oscar Heil in 1934. However, this idea did not see practical application until about two decades later, following the discovery of the transistor effect by the Bell Labs team led by William Shockley in 1947, which later initiated the development of semiconductor-based Junction FET (JFET) devices. The first JFET transistor, known as the Static Induction Transistor (SIT), was invented by Jun-ichi Nishizawa and Y Watanabe in 1950. The short channel length is a distinguishing feature of this type of transistor [28]. The MOSFET, invented by Dawon Kahng and Martin Atalla, is better known for its advancements in digital electronics than the JFET. In a device that uses the former, the majority-carriers or minority-carriers typically carry the majority of the current, according to [29]. The active channel, responsible for charge-carrier transport from source to drain, is formed by two terminal conductors electromagnetically interfaced with the semiconductor, facilitating the flow of electrons and holes. The potential that is applied across the gate and source terminals determines whether the active channels can conduct these carriers. There are three terminals in a FET: source, drain, and gate. Carriers (holes and electrons) enter the active channel through the source, denoted by source current (I_S), and exit the channel via the drains, denoted by the drain current (I_D).

The gate terminal (G) of the transistor modulates the channel's conductivity, enabling control of the drain current (I_D) by adjusting the gate voltage. FET-channel doping results in the production of n-type and p-type semiconductors. Unlike depletion-mode FET, enhancement-mode transistors have a configuration in which the source and

drain regions are doped with the same or a different type than the active channel. FET are also classified by the type of insulator separating the active channel from the gate. Figure 2.2 illustrates the cross-section of an n-type MOSFET [30].

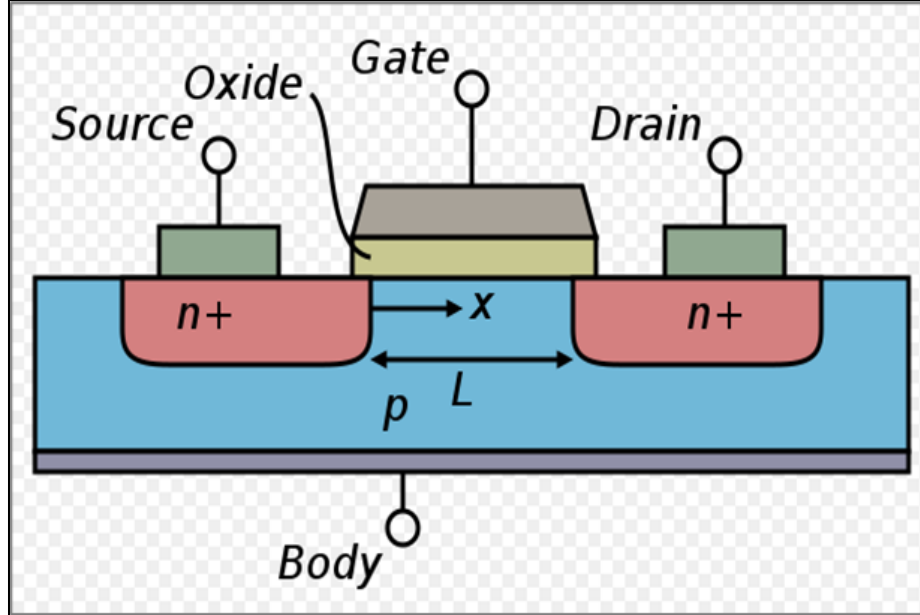


Figure 2.2 Cross-section of an n-type MOSFET [30].

2.5.1 Types of the Field-Effect Transistor

In some types of transistors, the gate terminal is isolated from the main channel by a reverse-biased P-N junction. In contrast, MOSFETs use an insulating material (usually Silicon dioxide [SiO_2]) between the gate and the channel. In metal-nitride-oxide semiconductor transistors, the layer is replaced with a nitride-oxide mixture. Dual-gate MOSFETs feature two separate gate terminals that work together to provide improved control over the channel. A depletion-mode FET is also characterized by the fact that it can amplify the signal of sensor and memory units, and, thus, it will be applicable in photon-sensing applications. The Schottky barrier replaces the P-N junction in a Metal-Semiconductor Field-Effect Transistor (MESFET). These devices are commonly used with III-V semiconductor materials, such as gallium arsenide (GaAs). The other type of FET is the organic memory transistor, which is designed using nanoparticles. Moreover, a graphene nanoribbon FET with a graphene-based active channel has been produced [31]. Vertical-slit FETs are defined as those with a square-shaped structure in which the source and drain terminals are bound together by a thin slit found at two opposing corners. The current flowing through this channel is

controlled by gates placed at these two corners [31]. Furthermore, graphene-based FETs are highly sensitive transistors widely used in chemical and biosensor applications. The two-dimensional (2D) architecture of graphene-based transistors enhances their sensitivity and intrinsic physical properties, while simultaneously reducing the incidence of false positives in sensing applications [32].

2.5.2 The Metal-Oxide-Semiconductor-Field-Effect-Transistor

The MOSFET serves as the cornerstone of contemporary Very-Large-Scale Integration (VLSI) circuits, with the swift advancement of the electronics industry largely driven by the advent of CMOS technology. However, some device topological structures have been investigated since about 1990 to replace the conventional bulk CMOS structure and prevent device size scaling. Electrical engineers undertake extensive research to develop new device structures, as the industry is now beginning to face several difficulties associated with device scaling as technology nodes continue to shrink [33].

For instance, leakage power consumption was not considered a significant problem before the technology node reached 180 nm. On the other hand, the effects of subthreshold leakage current have become increasingly important in manufacturing technologies at 90 nm and 65 nm, due to the substantial increase in transistor density [34]. Nevertheless, the subthreshold leakage current of a single transistor remains extremely low, typically below the nanoampere level. As process technology nodes have scaled down to 45 nm, managing power consumption and subthreshold leakage current has become increasingly challenging due to the rise in gate leakage. To continue shrinking transistor dimensions, Professor Chang-Ho and his colleagues introduced a new design that includes a FinFET transistor and another structure, a MOSFET with an Ultra-Thin Body on a Si-On-Insulator layer (UTB SOI) [35]. A representation of the structure of the UTB SOI MOSFET can be observed in Figure 2.3.

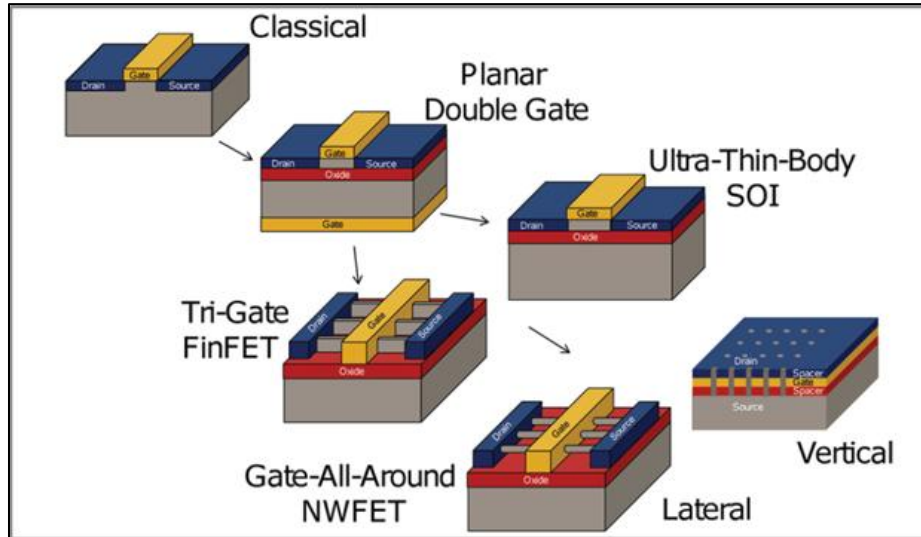


Figure 2.3 Field-Effect Transistor (FET) Architecture Development [35].

The nearly intrinsic doping of the UTB SOI body mitigates dopant-number fluctuations, thereby enabling further downscaling of transistor dimensions. An additional advantage of this structure is its capability to suppress punch-through effects. Nevertheless, the Berkeley Short-Channel IGFET Model (BSIM) group, under the leadership of Professor Chih-Hsiang Ho and Professor Saif Salahuddin, focused on the FinFET transistor architecture rather than the UTB SOI MOSFET, owing to FinFET's superior long-term potential. As illustrated in Figure 2.4, the FinFET structure provides significantly enhanced electrostatic control, reduced short-channel effects, and improved overall device performance, making it a more promising candidate for future technology nodes [36].

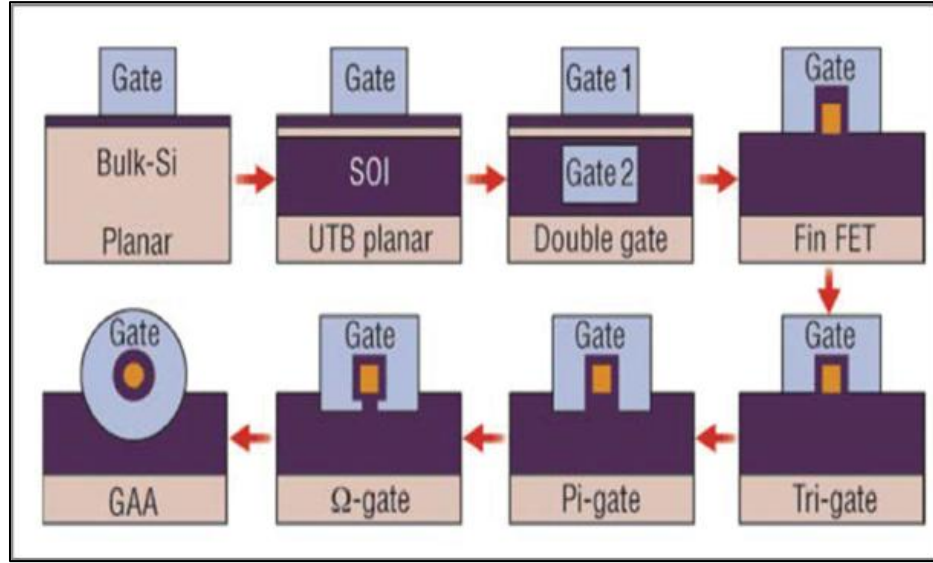


Figure 2.4 Improvements from planar MOSFET to GAA FET [36].

2.5.3 The Short Channel Effects

At nanoscale dimensions, the channel length of a MOSFET becomes comparable to the width of the source and drain depletion regions. This geometric proximity impairs the gate's ability to modulate the channel potential, leading to a range of phenomena known as SCEs. Among the most notable ones is DIBL, in which the drain voltage increases the channel potential, reducing gate control and shifting the threshold voltage [37]. When the channel doping concentration is insufficient and the gate length is short, the source and drain depletion regions may merge, resulting in punch-through. This is coupled with threshold-voltage roll-off, where the devices' threshold voltage steadily decreases with decreasing gate length. The degradation of devices by high-energy carriers further reduces device longevity, as these carriers damage the gate oxide and reduce mobility over time. Moreover, leakage across the gate oxide increases at smaller dimensions due to quantum tunneling processes, including trap-assisted tunneling, Fowler-Nordheim tunneling, and direct tunneling. In heavily doped regions where the gate overlaps the source, band-to-band tunneling can occur, leading to Gate-Induced Drain Leakage (GIDL). Collectively, these SCEs degrade device performance by increasing OFF-state leakage, reducing ON-state drive current, and weakening electrostatic gate control.

High-k dielectrics and metal gate electrodes in new planar MOSFETs have significantly reduced gate leakage currents and improved carrier mobility using fabricated source/drain stressors and new implantation methods [38]. Although these

have been achieved, planar MOSFETs face significant constraints as device dimensions are reduced below 30 nm. In particular, they exhibit poor suboptimal subthreshold swing (> 80 mV/dec) and high OFF-state leakage (> 100 nA/M), and do not support further downscaling of planar bulk architectures. As planar device geometries approach their scaling limits, mitigating short-channel effects through improved gate electrostatics has become essential. A potential solution is to make the body thinner to maximize electrostatic control while adding more gate interfaces. This approach underpins the transition toward multi-gate architectures, such as FinFETs, which offer superior gate-channel coupling and more effective suppression of short-channel phenomena in deeply scaled regimes.

2.6 FinFET Device

FinFET devices are classified based on a vertical double-gate configuration, often implemented on SOI platforms. These arrangements generally appear in two different designs. One is a three-terminal, symmetric, double-gate device, and the other is a four-terminal, front-gate-controlled channel-conduction device with a back-gate-controlled design, with a fixed rate or independently controlled bias [39]. The reduction in both the gate lengths allows for better electrostatic control over the channel and greater drive current. Notably, independent back-gate biasing enables fine-tuning of the V_T , thereby improving robustness against variations in temperature, supply voltage, and fabrication processes.

Transistors are largely of two types: planar, which are flat or two-dimensional, and non-planar, which have multiple gates. Among the latter, FinFETs (vertical fin-shaped channels) have superior gate-channel coupling since they enclose the conduction path on three sides. This tri-gate design provides better control over electric fields, faster charge-carrier mobility, and reduced short-channel effects. Compared to conventional planar MOSFETs, FinFETs offer lower leakage current, higher ON-state drive current, and more efficient switching behaviour, resulting in reduced power consumption and higher operating speed [40].

Non-planar MOS transistors, such as Double Gate (DG) and Gate All Around (GAA) transistors, promise to make significant progress in scalability, carrier transport, and packing density. Even though they were difficult to build at first and people did not use them much, they returned as viable options in sub-100 nm CMOS tech, where flat

designs ran into limits. Among these, FinFETs, which were first proposed in 1999 as double-gate 'folded-channel' devices, attracted considerable attention due to their quasi-planar shape and ease of manufacture on both SOI and bulk substrates [36, 37].

Although any device, so long as it has a Si fin on an oxide base, can loosely be described as a FinFET, there is a real distinction between GAA structures and a FinFET. A good example is the Tri-Gate (TG) MOSFET, a practical implementation of the FinFET family. It is technically known as a TG FinFET. The increased control over gate flow and the simplified fabrication of the device compared to other non-planar devices have made FinFET technology a top CMOS choice to address the performance scalability limitations of aggressive downscaling [42-43].

Although Si MOSFETs have a long history of development in VLSI, their inherent physical limitations impose traditional limitations on further performance improvement. Compared to FinFET architectures, however, they offer a viable future and are more effectively controlled, scalable, and energy-efficient for the further development of nanoscale electronics.

2.7 Strained FinFET

Strain engineering is the systematic application of strain to semiconductor components to improve their electrical and physical characteristics [45]. In FinFET devices, this technique is widely used to enhance carrier transport by varying the materials' band structures and, consequently, carrier mobility. A good example is the epitaxial deposition of a Si layer on a Si-Ge substrate, forming strained Si. Under this geometry, the tensile strain in the upper Si layer is caused by the larger lattice constant of Ge (5.65 Å) than that of Si (5.40 Å). This strain increases the interatomic distance, reducing electron scattering and increasing carrier mobility. Therefore, electron velocities can be increased by about 70%, and strained-Si transistors can operate up to 35% faster than aggressive counterparts [46].

Epitaxial growth of strained Si is a very important aspect in the development of FinFET channels and source/drain regions. High-performance, defect-free epitaxial layers are necessary to avoid detrimental effects such as strain relaxation, abnormal dopant redistribution, and reduced device reliability [47]. A common implementation involves introducing compressive strain in the channel by incorporating ~20% Ge into the Si-Ge alloy. During epitaxial growth, Ge atoms are inserted into the Si lattice,

causing compressive stress in the channel. This strained environment, as illustrated in Figure 2.5, is a key factor in optimizing the electrical properties and performance of FinFET architectures.

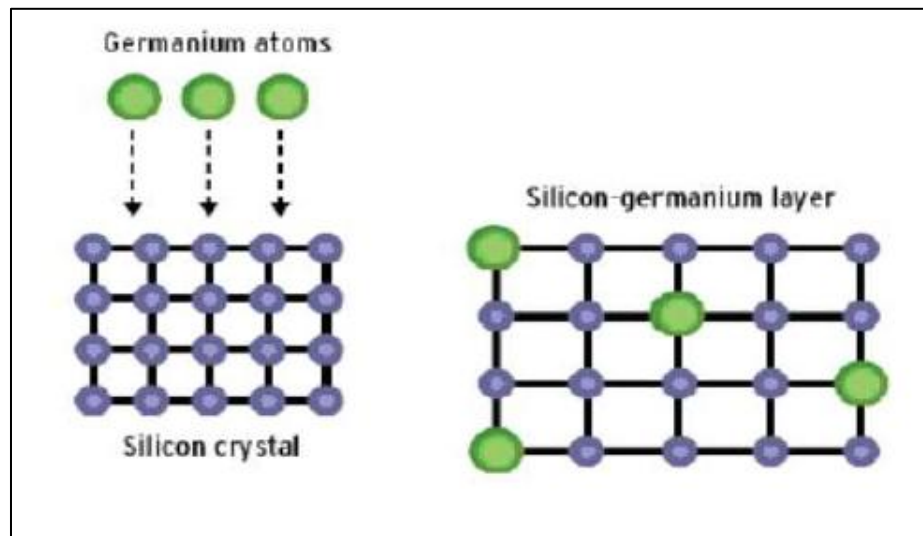


Figure 2.5 Strained Si-Ge structure.

Strain engineering exploits the fact that interatomic distances within a substance vary, and this shift can modify the substance's electronic properties. Such modifications can alter the bandgap and reduce scattering in a semiconductor such as Si, thereby enhancing electron and hole mobility. This is especially beneficial for contemporary transistor technologies, where reduced power consumption and quicker switching are essential. The incorporation of Si-Ge and other materials into epitaxial growth processes underscores the precision required in semiconductor fabrication to achieve the desired mechanical and electrical properties. Table 2.1 presents the comparison between the conventional FinFET and the strained FinFET.

Table 2.1

Comparison between the conventional FinFET and the strained FinFET.

Parameters	Strained FinFET	Conventional FinFET
Features sizes	Smaller	Larger
Operation speed	Faster	Slower
Dynamic power consumption	Lower	Higher
Rate of current flows	Higher	Lower
Trans-conductance	Higher	Lower
Operating voltage	Lower	Higher

Recent performance gains in Si-Ge FinFET technology have revealed that introducing a moderate Ge mole fraction ($x \sim 0.3-0.6$) enables improved carrier mobility resulting from strain-induced band-structure modification while preserving acceptable electrostatic control at sub-30 nm nodes [48]. Experimental reports in advanced nodes of the CMOS industry reveal that the subthreshold swing value of Si-Ge channel FinFETs can reach 70-90 mV/dec, and the DIBL value is less than 50 mV/V when the channel length is more than 20 nm [49]. However, for aggressively scaled devices (below 15 nm), electrochemical degradation will become significant due to enhanced drain-field penetration and charge-sharing effects. Structural optimization, such as fin-height engineering and a high-k gate stack, is usually adopted to overcome mobility-induced electrostatic penalties [36]. As summarized in Table 2.2, the reported experimental data clearly demonstrate that electrostatic integrity degrades significantly under aggressive channel scaling, especially below 20 nm, thereby confirming the scaling issues considered in this work.

Table 2.2

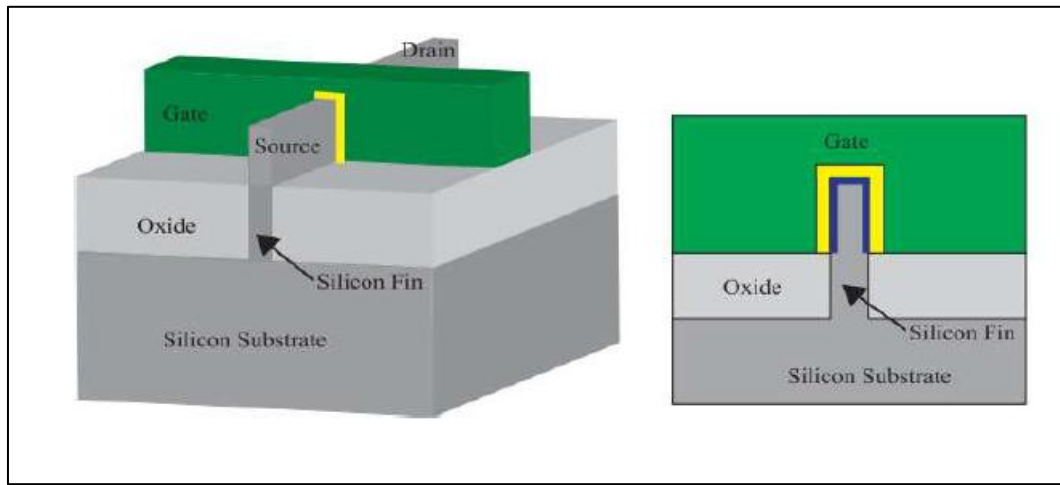
Comparison of SS and DIBL Values of Reported Si-Ge FinFET Technologies

Reference	Node	SS (mV/dec)	DIBL (mV/V)	Key Finding
[48]	22 nm	70–85	< 50	Strong electrostatic control
[36]	< 20 nm	100–150	120–180	Electrostatic degradation at aggressive scaling

2.8 Working Principle of FinFET

FinFET is generally regarded as a three-terminal device whose body is made of the Si fin and substrate and is not electrically connected in terminology, as it has the following three terminals: the gate (G), source (S), and drain (D), as in 3D and cross-sectional views in Figure 2.6 [50]. It performs tasks similar to those of MOSFETs, in which the input voltage controls the device's conductivity. Since no input current is needed to regulate the load current, it is superior to a BJT. There are two types of FinFETs: negative-channel (NMOS) and positive-channel (PMOS). When a positive potential is applied to a negatively doped drain and source (i.e., an NMOS transistor), it repels the positive charges (holes) in the substrate while attracting negative carriers from the substrate to form a channel inversion beneath the insulator material between the source and drain terminals. The gate and drain terminals need a potential applied to them for this device to work. It is necessary for the potential applied to the gate terminal, V_G , to exceed the threshold voltage, V_T . If V_G is less than V_T , no channel forms between the source and drain terminals, preventing current from flowing between them. "OFF" refers to the device's state. The potential difference across the gate-insulator interface also decreases as one approaches the drain terminal for a constant gate potential, since the applied drain voltage exceeds the source voltage. When $V_G - V_D \leq V_T$, a phenomenon called "pinched off" may occur. Pinch-off occurs when the channel stops before it is attached to the drain. However, since the depletion region attracts electrons to the drain terminal, the transistor continues to conduct. The operating principle for positively doped drain and source terminals (i.e., a PMOS transistor) is similar, except for a negative gate potential. To create the inversion channel that connects the drain and source terminals, the P-substrate's negative charges (electrons) are repelled, while positive carriers (holes) are attracted. FinFETs operate differently depending on the operating region. When the device is in the cutoff region, no current passes through it, and it is in the OFF state. On the other hand, the device can turn on since steady currents flow from the drain to the source, even though the voltage increases. In these two operating regions, FinFET can therefore act as a switch. Additionally, it can be employed in the linear/ohmic region as an amplifier. The amplifier increases the current across the drain-to-source terminal as the voltage across the drain-to-source path increases. In its "ON" state, an ideal transistor permits the maximum amount of current

to flow, while in its "OFF" state, virtually no current flows. Fast switching between the "ON" and "OFF" states is necessary to improve device performance.



(a) 3D structure (b) Cross-sectional view
Figure 2.6 3D structure and Cross-sectional view of FinFET.

2.9 Design Rule of FinFET model

There are design rules for FinFET construction that must be followed to achieve the expected functionality. Fin (drain, source, and channel), gate, oxide layer, and substrate layers comprise the FinFET design suggested in this project. The ratio of the fin width, W_{FIN} , to the channel length, L_g , must be configured to be less than (1:2) [51], as demonstrated in Table 2.3 [52]. This is an extremely important configuration. The sub-threshold swing is essentially the best-case scenario, and the short-channel effect is effectively suppressed.

Table 2.3
Design Rule of the FinFET Structure.

Regions	Ratio
Channel length	$L_g = \alpha \text{ nm}$
Fin Width	$W_{FIN} = \frac{\alpha}{2} \text{ nm}$

2.10 Si-Ge (Si-Ge) characteristics

The electron current density (J_n) in a transistor can be described by the following relation:

$$J_n = q \mu_n n \varepsilon, \quad (2.1)$$

where q is the elementary charge, μ_n is the electron mobility, n is the electron density in the channel, and ε is the electric field. To enhance transistor performance, both carrier concentration (n) and mobility (μ_n) must be maximized. Higher mobility can be achieved by reducing the carrier's effective mass, which is intrinsically linked to the material's band structure. Figure 2.7 presents the band gaps of various candidate channel materials as a function of lattice constant, with circle size indicating the relative effective mass of electrons or holes [53]. Ge, in comparison to Si, exhibits a lower hole effective mass and a smaller bandgap, resulting in superior hole mobility and a higher intrinsic carrier density. Moreover, the Ge lattice constant closely matches that of Si, reducing strain mismatch and enabling seamless integration into p-type MOSFETs [49-50].

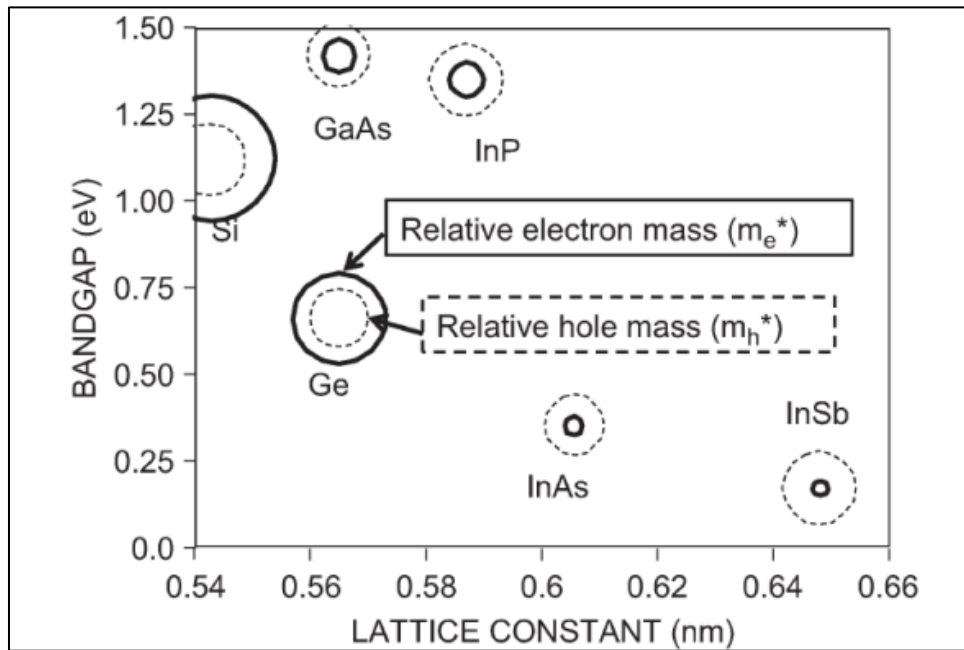


Figure 2.7 Bandgap according to various materials with lattice constant [53].

Strain engineering has been a critical approach in performance improvement since the CMOS technology incorporated the concept [51-52]. As illustrated in Figure 2.8 and 2.9, strain-induced modulation can significantly increase hole mobility in both Si and Ge, with the effect being much larger in Ge, highlighting its applicability for strain engineering. Given these advantages, Si-Ge has become a widely adopted channel material in modern transistor design. Figure 2.9 illustrates that CMOS inverters with Si-

Ge channels exhibit lower gate delay at the same Drain DC Voltage Source (V_{DD}) than their Si-based counterparts [58]. These qualities, taken together, make Si-Ge one of the chief competitors for next-generation transistor channels. In this respect, the FinFET devices modelled in this dissertation use Si-Ge as the channel material to leverage its excellent electrical properties and compatibility with strain-engineering methods.

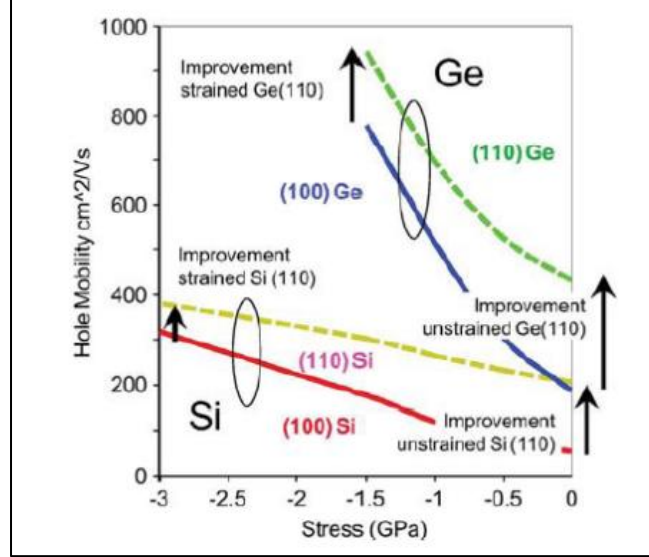


Figure 2.8 Comparison of hole mobility according to stress at Si and Ge [59].

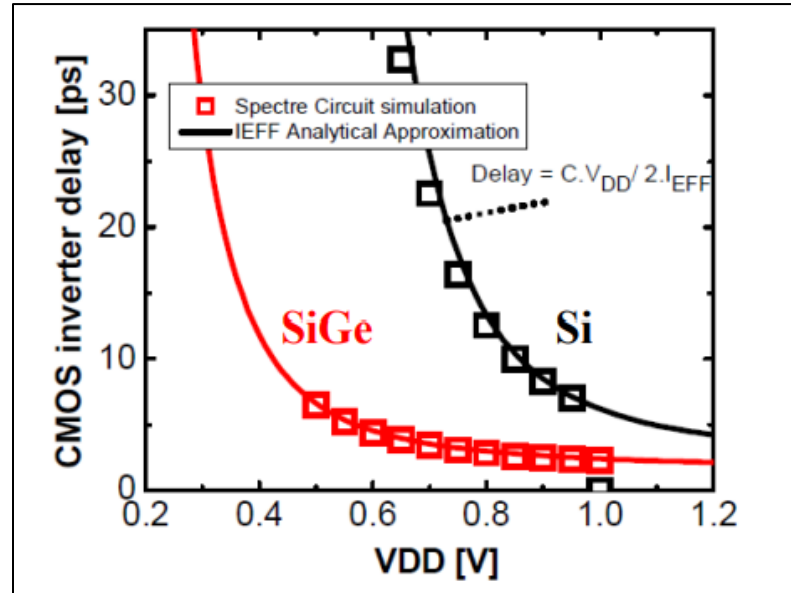


Figure 2.9 Comparison of CMOS inverter delay according to V_{DD} at Si and Ge [58].

2.11 FinFET- (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$) Structure Benefits

FinFET technology has emerged as a transformative solution to address the scaling limitations inherent in conventional planar MOSFET architectures. Its three-

dimensional geometry, in which the channel is surrounded by the gate on multiple sides, provides better electrostatic control, effectively suppressing SCEs (i.e., DIBL, SS degradation, and threshold voltage roll-off). The architecture is also used to achieve reduced leakage currents, improved switching behaviour, and the ability to scale down to sub-5 nm technology nodes [60]. One of the benefits of the FinFET design is that it can provide greater output impedance and reduced drain-to-source conductance, thereby improving voltage gain. Furthermore, FinFETs exhibit high transconductance, reduced Parasitic Capacitance (PC), and insensitivity to the body effect, all of which are highly desirable for high-speed, low-power electronics [61].

The choice of channel content also enhances device performance. Along with Si, although it remains the industry standard since it is compatible with the process, other materials, including Ge and $\text{Si}_{1-x}\text{Ge}_x$ alloys, are also prominent. The materials put strain in the channel, accelerating a carrier movement and generating a current. $\text{Si}_{1-x}\text{Ge}_x$ also allows the engineering of metal-gate work-functionality through threshold-voltage tuning [62]. In addition to group-IV semiconductors, there are II-VI semiconductor materials such as GaAs, GaSb, and GaN that can provide high electron mobility and very broad band gaps, which are useful for suppressing DIBL and minimizing band-to-band tunneling. It is worth noting that GaN FinFETs indicated better SS and DIBL at both longer and shorter gate lengths, especially at aggressively scaled gate lengths [63].

To conclude, FinFETs with Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$, or III-V semiconductor materials represent a flexible and scalable platform for the next-generation semiconductor technologies. High performance, high electrostatic integrity, and compatibility with future low-power, high-speed integrated circuits: Their improvements make them important enablers of the future.

Current research trends suggest that Si-Ge FinFETs are widely explored for low-power, high-mobility applications at sub-20 nm technology nodes. Most studies highlight the increased mobility achieved through Ge incorporation but note the associated increase in electrostatic sensitivity [64]. Recent literature highlights the importance of balancing the strain-induced mobility improvement with the short-channel suppression effect, especially in thermally constrained environments. Industrial implementations target moderate Ge ratios to work with existing semiconductor-processing methods [65]. According to Table 2.4, while the current literature is largely devoted to mobility improvement and short-channel suppression, several shortcomings remain apparent in aggressive scaling.

Table 2.4

Review of Si-Ge FinFET Studies State-of-the-Art Review of Si-Ge FinFET Studies
Highlighting Key Research Focus and Reported Limitations.

Study	Focus	Limitation Identified
[64]	Short-channel effects	Increased DIBL below 20 nm
[65]	Mobility enhancement	Ge-rich channels
	Thermal sensitivity in	

2.12 FinFET Fabrication

The initial and most critical step in FinFET fabrication is the design and formation of the fin structure. As illustrated in Figure 2.10, conventional lithographic techniques are employed to define the fin patterns. This is initiated by the deposition of stacked hard masks, usually Si nitride (Si_3N_4) and Si dioxide (SiO_2), using Chemical Vapor Deposition (CVD) [66]. Self-Aligned Double Patterning (SADP) is used at the state-of-the-art technology nodes to enhance resolution and density. The spacer formation achieves this through anisotropic etching. The main benefit of spacer-based lithography is that it allows a variety of fin pitches in a single lithographic step, thereby increasing both scale and pattern fidelity. Following fin patterning and etching, an oxide fill step is performed to isolate the fins. The oxide deposition must be conformal and void-free, and it must fill the deep trench without defects. The etching of the oxide is then done to an exact height of the Si fins. High-dose, angled ion implantation at the fin base to induce a punch-through stop layer completes electrical isolation and suppresses punch-through.

The resulting FinFET architecture is essentially identical in process to the conventional MOSFET process, i.e., source/drain implantation and gate stack deposition. In the case of bulk FinFETs, the main manufacturing challenge is maintaining even fin width and vertical sidewalls (which remain vertical) during anisotropic etching. Precision in these steps is critical for ensuring consistent electrical characteristics across the device array.

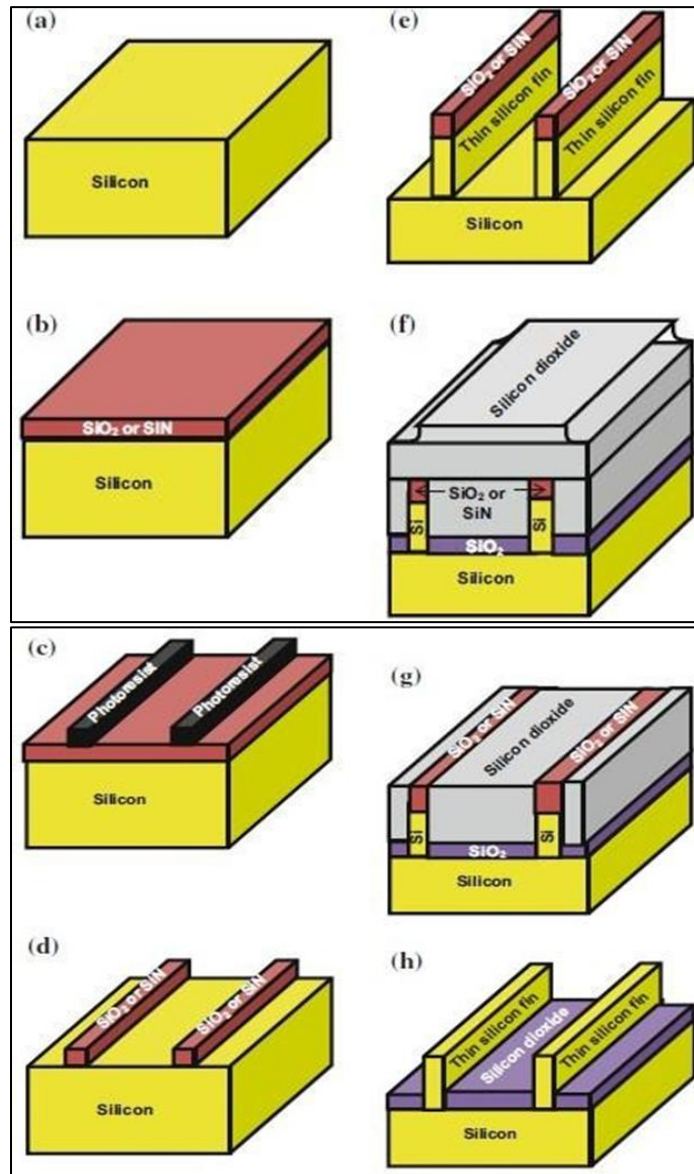


Figure 2.10 Conventional bulk FinFET process flow [66].

2.13 FinFET Electrical Characteristics

2.13.1 Characteristics of FinFET

The FinFET is a fin-like structure that has a distinctive channel connected to a thin Si "fin," hence the name. The fin thickness determines the channel's effective length. Additionally, standard fins are positioned vertically between the drain and the source. The gate provides an interface with three sides of the fin or channel, as it is positioned 90 degrees from the fin. This design mitigates short-channel effects by enhancing electrical control in the conduction channel, thereby reducing current

leakage. The FinFET is typically described as a multi-gate transistor architecture, regardless of the number of gates present. The advantages of FinFET are presented in Table 2.5 [67].

Table 2.5
Advantages of FinFET.

Parameters	Details
Power	Low power consumption enables higher levels of integration. Early adopters reported a 150% improvement.
Operating voltage	FinFETs operate at low voltage due to their low V_T .
Feature size	Enables passing through the 20 nm barrier, which was previously thought to be an endpoint.
Static leakage current	Typically reduced by up to 90%.
Operating speed	The performance is over 30% better than that of non-FinFET counterparts.

2.13.2 Short-channel Effects

FinFET devices exhibit a wide range of short-channel effects, including CMOS, Channel Length Modulation (CLM), DIBL, SS, punch-through, and mobility degradation. The majority of short-channel devices use CLM [60]. Typically, reducing the effective channel length (ΔL) while increasing the Drain-to-source voltage (V_{DS}) results in a near-linear increase in current in the saturation region. Moreover, the drain voltage influences the inversion channel, inducing significant shifts in V_T and current, a phenomenon known as drain-induced barrier lowering [60]. Punch-through is an extreme case of CLM or DIBL that occurs at the point of depletion when the drain and source are both large. Potential drain-to-source variations are slightly altered, and the current varies significantly due to merging into a single depletion region. It should be noted that a significant factor in determining the maximum threshold operating voltage of many devices is punch-through. The electrons near the device surfaces are therefore shielded from the higher electrical field and surface roughness, due to the higher bulk mobility compared to the layer. At higher vertical fields, degradation is the main cause of this decrease in mobility on the device surface. The approximate linearity that existed between the electric field and velocity is therefore no longer present when the electric

field is increased [60]. The establishment of a saturation electron velocity region is a consequence of this, and its existence is contingent upon the materials that are utilized in the device. Moreover, the SS is defined as the voltage changes required to convert the drain current by a factor of 10. Scaling down this technology increases leakage, thereby degrading SS. At this stage, it becomes challenging to control the channel and turn off the device. The energy barrier between the drain and the source is also controlled by the gates in double-gate MOSFETs, which allows independent adjustment of the barrier based on channel doping concentration [68].

To reduce the statistical effects of dopant fluctuations, lower the SCEs without adding impurities to the channel. The SCEs cause a spike in the SS as the channel narrows. Even when the fin width is appropriately sized, a larger SS of the device does not affect the excessive leakage. The fin width and the SS are therefore directly proportional. Although there is a corresponding subthreshold leakage, a lower SS value demonstrates good channel control. Therefore, an increase in drain current results from a wider Si fin. Furthermore, as the drain-to-source voltage increases, the devices' V_{TS} decrease, leading to a predominant DIBL effect. The DIBL effects are therefore reduced when the Si fin width is fabricated with a shorter channel length [66]. Therefore, the shorter the device gate length, the more quasi-linearly the V_T reduces, but at a specific critical gate length. In addition, V_T has a strong roll-off beyond this point, which diminishes sharply. For vertical double-gate devices, tight control of V_T via body doping is insufficient. Instead, a careful selection of the gate work function is needed to maintain satisfactory threshold voltage levels. This approach aims to minimise the effects of floating bodies, improve carrier mobility, and reduce variability arising from RD fluctuations. To further reduce PCs and resistance, and to be in the best position to control the channel, the double-gate devices must have well-controlled gate alignment [68]. Some of the back-gate control parameters include V_T , SS, and DIBL, as described in [69]. In ultra-short-channel devices, to reduce DIBL, extra substrate doping is typically applied around the edges of the source and drain junctions. These highly doped regions are usually called "halo" regions. As the channel length decreases in such configurations, the average channel doping concentration increases, resulting in a corresponding increase in the threshold voltage. The "reverse short-channel effect" is the term for the phenomenon. However, the threshold voltage decreases as the channel length decreases, and the regular SCE takes over at shorter channel lengths.

2.13.3 Drain Current of FinFET

The performance of a MOS device can be improved by increasing the carrier mobility or the channel saturation velocity [24-25]. The drain current and carrier mobility are positively correlated. Therefore, increased mobility improves the device's current and voltage characteristics. The gate electrode voltage range widens as the saturation velocity increases, since the current increases linearly with it. When the voltage is above this range, the current decreases, reducing power efficiency. It is crucial to reduce the gate oxide thickness, as this minimises SCEs, thereby maximizing channel charge mobility while lowering power supply voltages [70]. Increasing the thickness of the insulating oxide, on the other hand, helps expand the channel under the gate electrodes. As the channel is controlled indirectly, the device's efficiency is primarily determined by the SS, with little impact from the source and drain electrodes. The depletion, inversion, and oxide capacitances are the three main capacitances used to determine the electrical strength of the inversion layer [71]. The strength of the inversion layer increases as the oxide thickness decreases, thereby increasing the oxide capacitance. With an increase in drain current, the mobility of additional charges results in a more powerful inversion layer per unit of time. The double-gate device is typically operated with both gates on simultaneously. However, adaptive regulation is possible when the back gate is biased, enabling V_T shifting. In the context of any application highly sensitive to process shifting, this method might prove useful. In a symmetrically gated device with a typical channel thickness exceeding 5 nm, the two inversion layers do not interact, so two distinct inversion charge peaks are observed [24-25]. As the channel thickness decreases, these two channels will fuse into a single conduction channel. The SS slope is brought to a near-perfect condition with the two gates providing better channel control and lowering SCEs.

2.13.4 FinFET Subthreshold Operation

Sub-threshold devices have been used in the last few years in products such as pacemakers, Radio-Frequency Identification (RFID) tags, and hearing aids, which have essential low-power usage needs. The inherent delay in sub-threshold operation is a drawback that is primarily dependent on the power supply voltage [72]. To guarantee a steady power supply during transitional switching, careful consideration is required.

The sub-threshold operation of FinFET devices is a crucial area of study, as biasing devices in the sub-threshold region is frequently necessary to achieve lower-power circuits. The device speed being slower than biased devices is a significant issue [73]. The strong inversion resulting from the circuits' PCs, which requires less current to charge and discharge, is the cause. For high-frequency applications, most devices are currently made with strong inversion for optimal performance [74].

Retrograde and halo doping are commonly used to reduce short-channel effects, with particular emphasis on the DIBL effect when using punch-through for voltage adjustments. An implant may be unnecessary if a device already has a lower drain-to-source voltage, which always reduces DIBL and punch-through. Eliminating these doping processes, including retrograde and halo doping, reduces the PC in the channel region under the source and drain. FinFET and gate oxide thickness can both be optimized to increase sub-threshold operation speed and switching energy [73]. In the sub-threshold region, the gate capacitance is significantly lower than in strong inversion [74]. The fact that the gate capacitance depends on the oxide and depletion capacitances contributes to this condition. On the other hand, the gate and oxide capacitances are related in strong inversion. When designing the sub-threshold region, it is crucial to minimise PCs under bias conditions, as the devices' optimal frequency decreases as the current drops. In sub-threshold operation, long-channel double-gate devices appear to be well-suited for applications without compromising performance [60]. Within the strong-inversion region, the delay scales proportionally with the square of the gate length, whereas in the sub-threshold region, the delay scales linearly with the gate length. As the gate capacitance in the MOSFET is significantly lower, the delay is typically associated with the device's ON-current. An improved match in device operations results from increasing the gate length without causing a discernible delay penalty. When compared to long-channel devices from SCEs, this typically results in a robust design with greater variations in the ON-current of short-channel devices. For sub-threshold operations, it is therefore recommended to use a long-channel device rather than a short-channel device. Double-gate MOSFETs have significantly improved operating characteristics in sub-threshold operation compared to traditional planar CMOS devices. The negligible intrinsic capacitance of double-gate devices during sub-threshold operation is the cause. Between the two gates, there is typically a very thin structure that lowers the capacitance at the source and drain p-n junctions, enabling greater channel control [68-55]. Increasing the gate area also results in a significant

decrease in mismatch. The effects of adding more fingers are greater than those of adding more fins. Since the fin width is usually smaller than the channel length, reducing this width exacerbates the SCE. On the other hand, the intrinsic channel helps reduce random doping fluctuations that cause mismatch errors in traditional planar CMOS devices, thereby reducing issues of performance variation and mismatch. Furthermore, the enhancement of the control channels via the double-gate structure makes sub-threshold operation easier in FinFETs. The justification for a disruptive process is the need to conduct operational analyses and model the vertical double gate. Therefore, the benefits of employing the vertical double-gate architecture exceed the drawbacks of switching to a new technology. With significant performance, the suppression of SCE aids in navigating toward the use of a shorter gate length. In conclusion, a vertical double-gate device that has been designed correctly will invariably result in an improved performance margin [60].

2.14 Electrical Properties of a Transistor

2.14.1 Sub-threshold Swing

The subthreshold slope of the specified FinFET structure clearly improves as the device's gate work function increases. The higher device threshold voltage results in improved SS characteristics. This requires a change in the gate voltage, which in turn changes the drain current. With a surge in the ion current, the SS value decreases, so it should be as low as possible to turn the transistor ON or OFF more quickly. The fact that SS is measured in millivolts per decade (mV/dec) means that an enhanced transconductance must be considered mathematically. A decrease in the I_{OFF} corresponds to a steeper SS, which is defined as the inverse of the slope of the I_d plotted logarithmically against the gate voltage V_g . This parameter measures the sharpness of the transistors' transition from the OFF-state to the ON-state, with an ideal theoretical minimum value of indicating optimal switching performance. When the temperature is at room temperature, equation 2.2 can be used to calculate SS as follows [69-70]:

$$SS = \left(\frac{kBT}{q} \right) \ln 10. \quad (2.2)$$

KB is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge.

2.14.2 ON-to-OFF Current Ratio

The key parameters of FinFET performance assessment are the I_{ON} and I_{OFF} . I_{ON} , recorded at a gate voltage of 1 V, indicates the devices' speed, and I_{OFF} , the leakage in the off-state, affects standby power consumption. The ratio between them (I_{ON}/I_{OFF}) is a figure of merit, particularly in Low-Standby-Power (LSTP) applications. Large I_{ON}/I_{OFF} ratios indicate good switching and minimum leakage. This ratio is influenced by carrier mobility (μ), with values such as $\mu_{Si} = 1,500 \text{ cm}^2/\text{V}\cdot\text{s}$, $\mu_{Ge} = 3,900 \text{ cm}^2/\text{V}\cdot\text{s}$, $\mu_{GaAs} = 8,500 \text{ cm}^2/\text{V}\cdot\text{s}$, and $\mu_{InAs} = 40,000 \text{ cm}^2/\text{V}\cdot\text{s}$.

The FinFETs enhance this ratio by providing better control of short-channel effects, reducing threshold voltage roll-off and subthreshold slope decay. Moreover, a metal gate work-tuning function increases the threshold voltage and lowers the I_{OFF} . All in all, FinFETs offer a major benefit in their high I_{ON}/I_{OFF} ratio, which makes them suitable for power-saving nanoelectronics.

2.14.3 Threshold Voltage

The ideal threshold voltage in low-power electronic circuits is typically 0.4-0.8 V, which guarantees reliable switching behaviour with minimal static power dissipation. This voltage defines the gate-source voltage at which the FinFET switches between OFF and ON states, which is highly significant for trade-offs between speed and energy consumption. FinFET designs with $\text{Si}_{1-x}\text{Ge}_x$ exhibit threshold voltages that also vary with Ge concentration in the channel, device geometry, and oxide thickness. Greater Ge concentrations are prone to alter the band structure, shifting the Fermi level and thereby altering the threshold voltage. Moreover, carrier transport and threshold control can be influenced by strain arising from lattice mismatch in the Si-Ge layers. Useful modelling of the threshold-voltage behaviour across different compositions and operating temperatures is required to optimise device performance, particularly in scaled, thermally sensitive conditions.

2.14.4 Drain-Induced Barrier Lowering

The I_{OFF} and DIBL are two interrelated processes that play a vital role in the performance and scalability of nanoscale MOS devices. The extent of gate control over channel electrostatics is another important parameter of SCEs: DIBL. It appears as a decrease in V_T due to the change in the source-to-drain potential barrier of the source by V_d , which in turn allows channel conduction at lower gate voltages. Surgery to include enhancement of the gate work role also eliminates DIBL. The effect of this phenomenon is explained by the fact that, as observed in short-channel FinFET devices, lowering barrier heights in a particular channel is counteracted by the rise in V_T caused by a higher gate work function. The decrease in V_T due to DIBL, however, directly affects the leakage current I_{OFF} , an important design issue in logic circuits. High I_{OFF} also adds to static power dissipation and limits the performance of scaled-down devices. The effect of DIBL is greater at high and low drain voltages since the potential barrier at the source-channel interface decreases, thereby worsening electrostatic control and increasing leakage. Depicted by [78], the relation is quantitatively modelled through equation 2.3 in [79], which focuses on the interaction between DIBL, and in setting efficiency and scalability of nanoscale devices:

$$\text{DIBL} = \frac{\Delta V_T}{\Delta V_d}. \quad (2.3)$$

The shift in V_T relative to the drain voltage is measured in DIBL, which is usually expressed in millivolts per volt (mV/V).

2.15 Effects of FinFET Dimensions

The performance of FinFET devices is often affected by variations in V_T , channel length, and oxide thickness [73]. In long-channel devices, where the SS approaches its theoretical limit of ~ 60 mV/dec at room temperature, threshold-voltage differences are the most important factor in current mismatch [80]. Under these conditions, the mismatch is largely independent of gate voltage fluctuations. In contrast, for short-channel devices, the SS becomes dependent on channel length, and threshold-voltage variations are only one of several factors contributing to current mismatch [80]. The fluctuations in the SS are typically the cause of this phenomenon as well.

The fluctuations in V_T are mainly caused by Random Dopant Fluctuation (RDF) in FinFET devices. The mismatch issue is no longer a major concern for a properly designed FinFET, as a decrease in dopant density in the fin tends to reduce the impact of RDF, the main cause of current mismatch. It is necessary to consider additional sources of mismatch, such as variations in metal-gate work function and Line Edge Roughness (LER). The drain current mismatch in the sub-threshold region is typically estimated using the threshold voltage standard deviation. In short-channel FinFET devices, this deviation may not be a reliable indicator of drain current mismatch, as other significant components of mismatch besides threshold voltage fluctuations contribute [80]. The primary source of mismatch in long-channel FinFET devices, however, is threshold-voltage fluctuations.

In the FinFET fabrication process, gate length and Si film thickness represent the most critical sources of variation [81]. Enhancing drain current performance requires reducing the gate length [82]. This reduction, however, exacerbates the problem of SCEs, and this is a fundamental trade-off in device design. On the contrary, increasing the gate length will also enhance SS. The distance of the gate demonstrates the proximity of a value to an important ideal value. The critical length is most affected by the fin width; therefore, minimizing it is important for controlling SCE, as it reduces the mismatch impact at sub-threshold [82]. The critical length of a device is the length at which its deviation from the ideal SS is 10%. Then, additional device dimensions can be scaled. In addition, extinction due to current variation is minimised in areas with high inversion in the channel compared to the drain current [82]. The average current is lower in the sub-threshold region. The state of this condition indicates that both FinFET devices are widely mismatched in drain current, and this may take up to a decade to resolve. An example of the doped poly-Si used as the gate material is highly doped [83]. For an intrinsic body, the threshold voltages for the NMOS and PMOS devices are negative and positive, respectively, resulting in a depletion mode. The power consumption increases dramatically since the devices cannot be turned off, a problem that can be addressed by doping the channel in planar devices. Thus, adjusting the gate work function is preferable to channel implantation in FinFET devices. The randomised dopant effects resulting from ion implantation cause a significant mismatch. In the case of an intrinsic channel, the influence of RDF is markedly reduced. One of the major challenges remains the identification of an appropriate metal gate material to effectively replace the traditional poly-Si gate. Additionally, intrinsic channels enhance carrier

mobility by eliminating the need for high doping concentration, which are known to degrade mobility. Nevertheless, the effects of DIBL are mitigated in planar CMOS devices since increased doping increases substrate control of the channel. Carrier mobility is higher in non-doped channels. This effect can be mitigated through the introduction of a back gate, which enhances electrostatic control. In planar CMOS devices, however, controlling the threshold voltage by adjusting the gate work function is ineffective due to the pronounced influence of SCEs.

FinFET structures remain subject to Pilgrim's law, which asserts that variability is inversely proportional to the gate area, whereas the variability in the effective width of multiple parallel minimum-width devices is substantially lower than that of a single device possessing an equivalent total width [77-78]. Therefore, adding more fingers to a device is a better idea than adding more fins. Channel width expands with the addition of more fins, as the total device width is defined by the fin number. A pronounced increase in threshold voltage occurs as the body becomes thinner. However, reducing the device length induces threshold-voltage roll-off and exacerbates SCEs. The gates get closer together, and the channel is more controllable as the body thickness decreases. So, adding fingers to a device instead of fins makes more sense. In a FinFET structure, increasing the number of fins effectively broadens the channel, as the overall device width is directly proportional to the number of fins. Furthermore, a reduction in body thickness results in a noticeable increase in threshold voltage, attributed to improved electrostatic control. As the body becomes thinner, the gates are brought closer together, enhancing channel control and thereby mitigating both SCEs and threshold voltage roll-off, which are typically associated with reduced device length.

SS strongly depends on body thickness [77-78]. The channel is challenging to invert since the threshold voltage increases as the body thickness decreases. DIBL grows quickly as body thickness increases. There was a 13% increase in sub-threshold leakage for every 20% increase in gate oxide thickness [73]. This condition makes intuitive sense when using an SOI device as a model since the sub-threshold swing term has been included in the sub-threshold drain current equations, and the gate-to-source voltage term. The parameter results from the device's surface potential being indirectly regulated. As the oxide thickness increases, the sub-threshold swing increases due to reduced gate control.

2.16 Semiconductor Materials

Semiconductors are materials that can behave either as insulators or conductors, depending on the conditions in which they operate. This behaviour arises from the interactions between the outer electrons of atoms and the nature of chemical bonding within the bulk material, which collectively determine the material's electrical properties. In the same way that all other atoms have a predetermined structure, the individual atoms that make up semiconductor materials have a predetermined structure that determines how they bond with various other atoms. The performance of FinFETs is greatly influenced by the semiconductor materials used. Thus, four semiconductors have been used to study these effects.

2.16.1 Si Semiconductor

Si has long served as the foundational material in Integrated Circuits (IC) design due to its electronic versatility, manufacturing maturity, and physical reliability. The initial transistor was made using bulk Si substrates, and the ever-shrinking geometric dimensions of MOSFETs have enabled geometric increases in chip density and computational speed. However, aggressive scaling beyond the 20 nm regime led to significant SCEs, limiting the effectiveness of conventional bulk Si MOSFETs in advanced nodes [85]. To overcome these drawbacks, the semiconductor industry shifted to SOI technology, which improves control of electrostatic gates and reduces PC. The transistors in SOI architectures are fabricated on a buried oxide, which reduces junction leakage and increases switching efficiency. SOI devices with Fully Depleted SOI (FD-SOI) are also more desirable, as they are better in terms of gate-to-channel coupling, and are useful in cases of low-voltage and high-frequency operation [86]. Figure 2.11 below conceptually illustrates the fabrication process of a SOI wafer using the smart cut technique [87]. This is performed by first oxidizing the surface of a Si wafer and then implanting it with hydrogen ions. This wafer is inverted and attached to a second wafer known as a handle [87]. Bubbles are generated in the hydrogen-implanted layer during thermal annealing, ultimately causing a break and transfer of the Topmost Si layer. The outcome is an SOI wafer consisting of a thin active layer of Si on a layer of BOX that is to be utilized to improve isolation and minimise parasitic in high-tech transistor hidden handing.

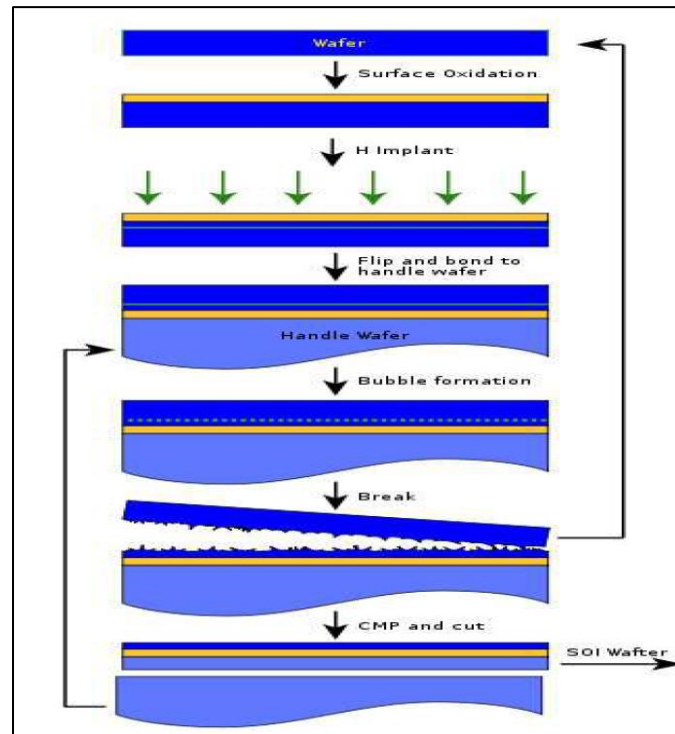


Figure 2.11 Fabrication of SOI through oxidation [87].

FinFETs are three-dimensional multi-gate transistors that are an evolution of the SOI concept and are often made using silicon fins. The conductors are these fins, and the conduction channel is bound on three sides, with the gate electrode coiled around it, thus increasing electrostatic integrity compared to planar device architectures. The resultant geometry provides greater control over the channel potential, thereby minimizing SCEs such as DIBL and threshold-voltage roll-off [88]. Si is ideal for FinFET channels, with a medium bandgap (~ 1.12 eV), decent electron and hole mobilities, and compatibility with high-k/metal gate stacks. The fin geometry, especially fin width and height, is also crucial for calculating drive current and gate control. Fins with narrow cross-sections and high aspect ratios provide improved electrostatic control but require extremely precise etching to reduce surface scattering and decrease variability in sub-band energy states. Experimental fabrication efforts have realized FinFET devices with silicon fins as narrow as 3 nm, thereby confirming the technology's scalability [83-84]. Although there are benefits, there are some challenges. For example, ultra-thin gate oxides used to maintain gate control could increase gate-to-channel capacitance and encourage direct tunneling. Likewise, channel doping, in practice, to suppress SCEs, can impair carrier mobility and raise GIDL, becoming detrimental in nanodevices [91]. Finally, FinFET architecture continues to use Si in current electronics. It enables high-performance transistors and extends their

compatibility with the CMOS manufacturing infrastructure. Its applicability to the next sub-5 nm and below nodes is guaranteed by the continuous improvement of Si-based FinFETs on SOI substrates, strain engineering, and nanometric channel designs [92].

2.16.2 Ge Semiconductor

Ge has now taken on new significance in the manufacture of semiconductor devices, thanks to its high electronic properties, which enable improvements in carrier transport and threshold voltage control. Although Si remains the predominant material in CMOS construction, Ge offers important benefits, particularly for $\text{Si}_{1-x}\text{Ge}_x$ FinFET devices, as it provides better channel behaviour in strongly scaled structures. Among Ge's major contributions to electronics is its significant impact on carrier mobility. Ge disturbs the lattice structure when placed in strained Si channels, thereby improving hole and electron mobilities [93]. This strain increases drive current and modifies the material's band structure, often leading to lower threshold voltages and improved subthreshold swing. These advantages are especially applicable to FinFETs with low supply voltages, where leakage has become a major problem and switching efficiency is of great concern. Ge is also critical to the gate-stack engineering. Ultrathin body devices have adopted Si-Ge-based gate materials to achieve optimal modulation of the threshold voltage and low resistivity simultaneously [94]. Indicatively, highly boron-doped poly-Si-Ge with a high Ge composition (e.g., 60% Ge) has revealed a work function of 4.75 eV, in addition to enhanced conductivity compared with traditional poly-Si-Ge gates with equal levels [95]. These gate materials are compatible with existing CMOS flows and enable continuous modulation of electronic parameters via Ge composition.

Moreover, comparative simulation studies have also compared Ge and Ge-containing materials (e.g., GaSb) with other semiconductor alternatives, including GaAs, GaN, and Si. Despite reduced DIBL behaviour in the GaSb channel, positive subthreshold swing was observed in narrow channels less than 18 nm, with a selective Ge benefit observed in some design regimes [90-91]. This helps substantiate that Ge may not perform as well as Si in all measurements, but when judiciously utilized, it offers specific electronic advantages. To conclude, FinFET technology is refined by Ge in two aspects: (1) it allows strain engineering that leads to enhanced carrier mobility, and (2) it is used as a functional component in gate and channel materials that provide

a chance to achieve precise electronic control. The fact that it can be integrated into $\text{Si}_{1-x}\text{Ge}_x$ systems supports the ongoing need for scalable, high-performance transistor layouts under a range of temperature and size conditions, in line with the targets of contemporary nanoscale CMOS development [98].

2.16.3 Si- Ge Semiconductor

The electron mobility in $\text{Si}_{1-x}\text{Ge}_x$ alloys at low electric fields is relatively low in mechanically strained materials. However, hole mobility has been significantly improved, which has motivated its widespread use in state-of-the-art transistor technology [99]. $\text{Si}_{1-x}\text{Ge}_x$ (x = mole fraction of Ge) is a completely miscible solid-solution semiconductor with a diamond cubic crystal structure. As illustrated in Figure 2.12, the atomic strain induced by compositional variations within the alloy is predominantly accommodated through systematic adjustments in both bond lengths and bond angles [100].

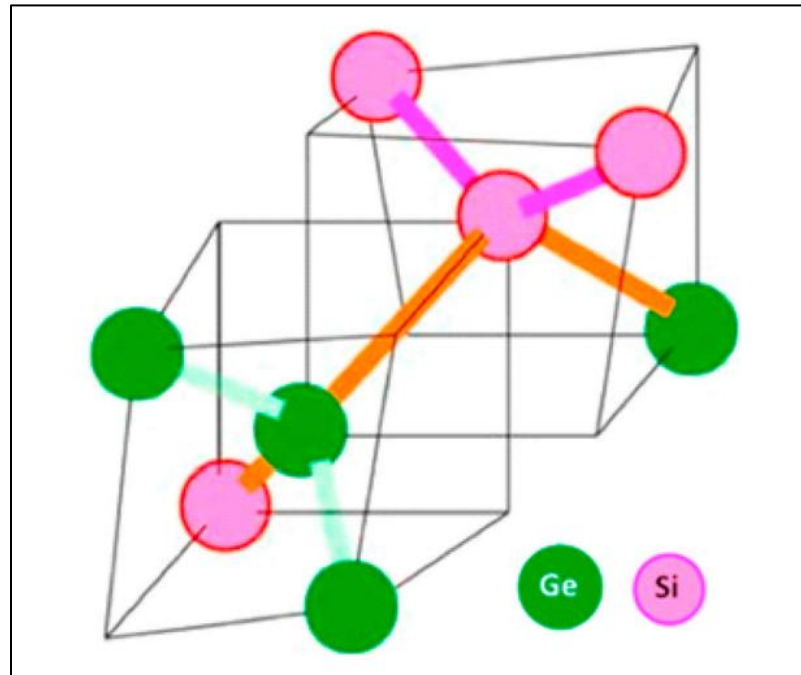


Figure 2.12 The local atomistic structure of Si-Ge alloy [100].

The Si-Ge alloy is known to exhibit unique fundamental properties, such as atomistic bonding configurations, electron and hole mobilities, thermal conductivity, local vibrational modes of oxygen impurities, and muonium behaviour, which are not present in its constituent components, Si and Ge. It should also be noted that the Si-Ge

alloy is a prototypical disordered material that exhibits quasi-Pauling behaviour, with composition-dependent distortions in bond lengths and bond angles. The mechanical strength of the binary alloy Si-Ge becomes temperature-insensitive at high temperatures. Instead, it becomes a composition-dependent property, revealing a proportional correlation of $x(1-x)$ across the entire compositional spectrum [101]. The lower thermal conductivity (k) of Si-Ge alloys improves thermoelectric performance compared to both single-crystal and polycrystalline Si. In addition, Si and Ge can be completely mixed over a wide range of compositions to form a solid-solution semiconductor. This has been empirically demonstrated through experimental research, e.g., [102], and other modelling techniques, that Ge can substantially improve the performance and efficiency of CMOS devices. Ge has greater channel mobility than Si tri-gate MOSFETs (TG-MOSFETs), which exhibit higher electron and hole mobility [102]. There is a high probability that Ge will increase the variety of CMOS circuit applications. Ge offers several inherent and procedural benefits that make it an attractive alternative to Si channels in future high-tech CMOS devices. It is fully compatible with well-established Si fabrication processes and can be easily integrated into through-silicon manufacturing. Ge oxynitride (GeON) offers a high dielectric constant and flexibility, and is compatible with advanced metal gate stacks. Transport-wise, Ge has a much higher carrier mobility than Si, and hole mobility is almost twice that of Si, allowing Ge hole devices to perform better. Moreover, Ge-based TG-MOSFETs offer significantly higher channel mobility than Si-based TG-MOSFETs, with enhanced drive current capability and overall transistor behaviour [102].

The p-channel device has a characteristic advantage over the n-channel in Ge bulk MOSFETs since the latter provides a driving current that is 1 to 2 orders of magnitude lower than that of the former [103]. Si-Ge material is used to provide high-efficiency electron transport in the channel region of FETs, as it offers enhanced carrier mobility and a reduced effective carrier mass. The proposed device architecture includes a Si-Ge channel. To understand device performance as a function of Ge mole fraction in the Si-Ge channel region of FinFETs, a theoretical analysis is conducted. Compared with traditional Si-channel FinFETs, the Si-Ge channel FinFET exhibits superior ON-state characteristics.

2.16.4 Effect of Semiconductor Materials on the Electrical Properties of Transistors

The role of nonconventional semiconductor materials is becoming increasingly prominent as transistor dimensions approach the nanoscale, since their properties can vary significantly at the nanoparticle scale. Si-based CMOS technology has been the driving force of the semiconductor industry since its introduction in the late 1970s. A variety of evolutionary design techniques have been implemented over time to improve device performance. Some of the techniques employed include high-k gate dielectrics to eliminate leakage currents, multi-core design to reduce power consumption, and strain engineering to increase carrier mobility via enhanced gate control. The last method for improving device reliability is the use of SOI substrates, which are more resistant to the effects of multi-gate 3D substructures, thereby enhancing gate control. Notably, to improve device performance, increase integration density, reduce production costs, and lower power consumption, the critical lengths of MOSFET transistors have undergone significant development, transitioning from the micron level to the sub-micron node, then to the very small node, and finally to the currently available 14-nm node [104]. However, the performance gain obtained by scaling down becomes increasingly limited. The power density on the chip will rise in tandem with the Central Processing Unit (CPU) decreasing pitch size. The power density trend of the CPU over the past decade is depicted in Figure 2.13 [105]. To prevent overheating, the power density is maintained at or below 100 W/cm². This indicates that the trend of reducing MOSFET transistor size has shifted towards focusing on power consumption as a key factor in scaling [106].

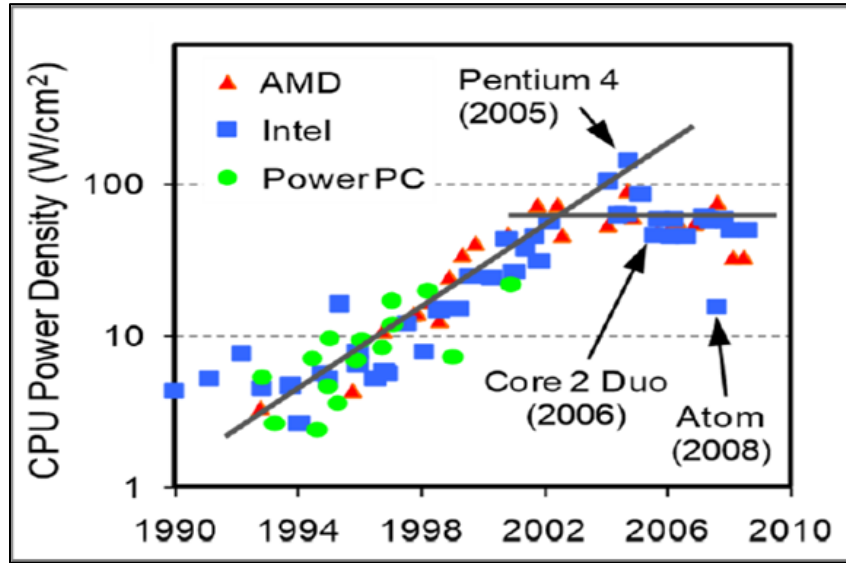


Figure 2.13 Trend of CPU power density over the past decade [105].

The CPU clock rate has not changed significantly since the switch from a single-core to a multi-core CPU architecture. A decrease in the supply voltage is necessary as the device scales, since the number of transistors continues to grow [107]. However, reducing the supply voltage would decrease drive current, slowing down circuits. The drive current must be maintained or increased as the operating voltage decreases to resolve this [108]. In a MOSFET transistor, the carrier injection velocity near the source and along the channel direction is denoted by, while represents the total charge. This straightforward analysis suggests that increasing carrier injection velocity could enhance the drive current. Higher injection velocities can be maintained even at lower operating voltages by using high-mobility channel materials [109].

The fundamental electrical characteristics of different semiconductor materials are listed in Table 2.6 [107]. Compared to Si, the hole and electron mobility of Ge and III-V compounds are significantly greater. High-mobility channel materials are crucial for meeting the demands of next-generation low-power and high-speed circuits [107].

Table 2.6
Fundamental electrical properties of Si-Ge alloys and III-V compound semiconductors.

T = 300 K	Si	GaAs	InAs	GaSb	Ge
μ_p (cm ² /V.s)	450	400	500	1000	1900
μ_n (cm ² /V.s)	1500	8500	40000	3000	3900
ni (cm ⁻³)	1 × 10 ¹⁰	2.1 × 10 ⁶	1 × 10 ¹⁵	1.5 × 10 ¹²	2 × 10 ¹³
Eg (eV)	1.12	1.42	0.36	0.726	0.66

2.17 Comparative Summary of Previous Studies

This discussion summarizes recent research on the impact of nanoscale dimensions on the electrical properties of FinFET devices. Simulation of FinFET operation is also critical for making design decisions, as channel dimensions can be further scaled and device performance improves. Over the past decade, extensive investigations have been conducted into the fabrication of FinFET transistors with varying nanoscale dimensions. These studies encompass various semiconductor and dielectric materials and a range of manufacturing techniques, all aimed at forecasting and optimizing FinFET performance [110]. However, it was identified from the review of this section that some studies were limited to a one-dimensional analysis of the channel, such as length, width, or oxide thickness, and relied on only one property, such as the I_{ON}/I_{OFF} , SS, or DIBL, and were limited to one type of semiconductor, such as Si-FinFET or Ge-FinFET. Additionally, these studies did not focus on a comprehensive understanding of the subject. Theoretical performance estimates for Si-Ge nanotransistors and Si-Ge wire FinFETs were analysed by [111]. Two of their candidates are listed: the Si-Ge and Si-Ge nanowire FinFETs. To analyse and verify short-channel effects, including DIBL and the I_{ON}/I_{OFF} ratio for switching, the effects of doping concentration, channel length, and dielectric thickness were investigated. Researchers reported that the Si structure indicates significant improvements in logic performance metrics, including reduced I_{ON}/I_{OFF} and DIBL, compared to two other structures. The results also demonstrated that increasing the doping concentration improves the on-state current, thereby increasing the I_{ON}/I_{OFF} ratio in these structures. It also affects DIBL. For each of the three simulated devices, they also compared the analogy performance

parameters, such as the voltage gain (A_v), output conductance (g_d), and Tran's conductance (g_m). The results reveal that the Si-Ge FinFET transistor is suitable for analog applications, achieving a channel length of 7 nm, an I_{ON}/I_{OFF} ratio of 10^9 , and a DIBL value of 28. However, the study did not address the effect of channel width and did not provide data on SS, which directly affects transistor speed.

The physical principles underlying the scaling of junction-less FinFETs with Gaussian channel design have been explored [112]. In their study, a junction-less FinFET incorporating a Gaussian-distributed channel was proposed and analysed to assess its viability for scaling to nanoscale dimensions. Performance parameters I_{OFF} , I_{ON}/I_{OFF} , DIBL, and SS were analysed with respect to the physical gate length L_g , gate oxide thickness T_{ox} , and fin thickness, which are the most critical device parameters. Comparison has been made between a conventional Uniformly Doped Junction Less FinFET (UD-JL FinFET) structure and this proposed graded FinFET structure. The I_{ON}/I_{OFF} ratio and SS of the Graded Channel-Junction Less (GC-JL) FinFET transistor structure (design without channel junction $\times$ Gaussian) are superior when the gate length is scaled down to 7 nm. However, DIBL performance degrades significantly when the gate length is reduced below 14 nm. At a gate length of 10 nm, the GC-JL FinFET transistor can achieve an SS value of up to 85 mV/dec and a DIBL value of up to 100 mV/V, as previously noted. The limit of reducing the gate dielectric thickness, which is mainly affected by the current due to the gate tunneling phenomenon, was also studied for both GC-JL FinFET and UD-JL FinFET structures. Despite reaching a gate length of 10 nm, the SS value remains relatively high at 85 mV/dec, and the DIBL is 100 mV/V. The effect of cross-sectional shape on the performance and variability of 10 nm gate-length InGaAs FET has been investigated [113]. Three-dimensional simulation models based on the finite element method with quantum correction using the drift-diffusion technique based on density gradient, in addition to Monte Carlo simulation, were used to study the performance of FinFET transistors with a gate length of 10.4 nm. The influence of cross-sectional geometry on the (I_d - V_g) characteristics was examined, along with an assessment of variations arising from Metal Gate Granularity (MGG), LER, and RD effects, and a comparative analysis of their combined impact. The results implied that a more triangular cross-section is associated with lower off-state current, reduced DIBL, and improved SS. Compared to the rectangular FinFET, the triangular FinFET has a three-fold higher I_{ON}/I_{OFF} ratio. The main fluctuations influencing the FinFETs, regardless of cross section, are the MGG variations, which have V_T that are

four to two times larger than those from the LER and the RD fluctuations, respectively. However, the MGG depicts a very small variability-induced V_T shift (about 2 mV), whereas the LER and RDs demonstrate V_T shifts that are 4 and 15 times larger, respectively. The standard deviation across different device geometries is only ~4%, indicating that cross-sectional shape exerts a negligible influence on both threshold voltage V_T and I_{OFF} , whether MGG, LER, and RDs are considered independently or in combination. Lastly, simulated combined variability can be predicted with only a slight overestimation using the statistical sum of the three sources of variability. The results that were obtained, however, were $I_{ON}/I_{OFF} = 4.70 \times 10^4$, $DIBL = 67.3$ mV/V, and $SS = 61.3$ mV/dec. Notably, while the SS value is good, the energy was dissipated due to the low I_{ON}/I_{OFF} ratio. The application of tri-gate Ge FinFET, gate-source overlap, dual-stacked gate dielectrics, and dual-material gates was examined by [114]. A novel dual-material-gate, dual-stacked-gate dielectric gate-source that overlaps the Ge-FinFET was proposed in the study, and its properties were compared with those of the traditional FinFET. The device demonstrated a high ratio ($\sim 10^{13}$), a low subthreshold swing (71 mV/dec), and a 40 nm channel length. These features resulted in a greatly reduced leakage current ($\sim 10^{-17}$ A), which, in turn, affected the drain current, which was approximately 10^{-4} A. There were hypotheses that the transfer characteristics of the devices could be altered by changes in T_{ox} and back-gate bias (V_{gb}). Further, the channel-doping concentration effect on major performance parameters, including the I_{ON}/I_{OFF} ratio, V_T , gm, and SS, was examined. The influence of the overlap length (L_{ov}) on the gate-to-source capacitance (C_{gs}), a significant analog parameter, was also studied. Besides, the effect of fin thickness (T_{fin}) on V_T and SS was considered. The BOX height is one of the major factors considered in reducing the I_{OFF} . It was indicated that the digital application that uses the proposed device as a digital inverter circuit was identified. Mixed-mode simulation was applied to make this a reality. Additionally, an experiment was conducted to investigate how changes in the geometry parameters of the Sub-50 nm FinFET affect its performance (as noted by [115]). Several parameters, including DIBL, SS, and I_{ON}/I_{OFF} , vary with gate length up to 5 nm and an oxide thickness of 0.9 nm. These findings suggest that the device parameters improve significantly with a reduced gate length. It is worth noting that leakage current remains within the acceptable range at gate lengths larger than about 10 nm, and a 20 nm gate length also provides significant improvements in transfer characteristics. However, when the gate becomes very small, just a few nanometres, then the leakage current is

an enormous issue that can no longer be overlooked. In the sub-10 nm world, the only way to achieve optimal performance is to meticulously adjust the mesh spacing and doping concentration to ensure the electric field is not excessive while minimizing leakage. As an example, an I_{ON}/I_{OFF} current ratio of 3.6×10^8 , a DIBL of 69.96 mV/V, and a sub-threshold slope of 69.11 mV/dec can be achieved. Such design optimizations improve performance at shorter gate lengths and enable analysis of the impact of mesh spacing and gate activity variation. However, aside from the new contribution of oxide thickness, the overall performance improvements in the data were not very high.

A comparative analysis of FinFET and GAA Nanowire FETs was conducted to assess scaling behaviour and variability, as reported by [116]. The variability and scalability in performance of Si-based devices with 25/10.7 nm (FinFETs) and 22/10 nm (GAA NW FETs) gate lengths were tested. This was conducted by comparing results from a mixed three-dimensional quantum-corrected Monte Carlo (MC) and Finite-Element Device Design (FEDD) with channel lengths spanning 25 to 10 nm. The best performance measures were observed at the scale of 10 nm, with the following I_{ON}/I_{OFF} ratio of 1.53×10^5 , V_T of 26 mV, and SS of 68 mV/dec, with reference to both MGG and LER. It was observed that FinFETs had SS in the OFF-state region about 9% higher than that of GAA NW. However, the GAA NW devices demonstrated OFF-state currents that were an order of magnitude greater. In the ON-state, FinFETs with gate lengths of 25 nm and 10.7 nm delivered 20% and 58% higher ON currents, respectively, compared to GAA NW devices with equivalent gate lengths of 22 nm and 10 nm. Nevertheless, the I_{ON}/I_{OFF} of the gate-all-around GAA NW device, reaching approximately 1.3×10^4 at L_g of 10 nm, surpasses that of the FinFET, which exhibits a ratio of 1×10^4 at $L_g = 10.7$ nm, by more than an order of magnitude. When scaling the devices, performance degrades, especially in the I_{ON}/I_{OFF} ratio, leading to extreme energy dissipation as I_{OFF} increases at the expense of I_{ON} . In CMOS inverter setups, recent developments, including the use of Ge surface treatments, have improved the electrical properties of GeN and planar FinFETs [117]. Digital ozone (O_3) exposure of the sidewalls of the Ge-Fin structure through in-situ Atomic Layer Deposition (ALD) was used to reduce the damage and surface roughness induced by etching, and to enable Ge oxide (GeO) desorption. The n-FinFET and p-FinFET transistors, as well as the Ge-CMOS inverters, all revealed a significant increase in SS values and I_{ON}/I_{OFF} ratios when the proposed processing was combined with the improved Microwave Annealing (MWA) technique. At a low supply voltage of 0.6 V (V_d), a high voltage gain of 50.3

was attained. In a quest to enhance the operations of Ge-based FinFET transistors, a novel manufacturing procedure has been suggested which incorporates MWA and in-situ processing which utilizes ALD furnished with digital O₃ technology. This has proved to be effective in achieving CMOS inverters with transistors of Ge-FinFET based transistors with increased performance. The n-FinFET and p-FinFET transistors exhibited superior SS characteristics of 71 mV/dec and 88 mV/dec, respectively, with an I_{ON}/I_{OFF} ratio of 10 at a channel width of 20 nm and a channel length of 200 nm. The good electrical characteristics, especially the ability to achieve a voltage gain of 50.3 in the CMOS inverter circuit, are due to the qualitative improvement of the Ge/gate oxide interface enabled by ozone-based digital ALD in the fabrication chamber. Previous studies emphasized that prior design methods led to large transistor sizes, high manufacturing costs, and low integration density, and were therefore not viable for contemporary nano-electronic applications.

In a study by [118], the effect of various semiconductor materials used in FinFET channel FinFETs, namely Si, Ge, GaAs, and InAs, on thermal performance was examined. The simulation examined temperature sensitivity by analysing the transfer characteristics of FinFET devices operating at $V_d = 1$ V over a temperature range of $-25, 0, 25, 50, 75, 100,$ and 125°C . The findings revealed that GaAs-based FinFETs demonstrated the highest current variation (ΔI) of 10.9% at 25°C , indicating a strong temperature-dependent response. In contrast, Si-based FinFETs exhibited superior thermal stability, with the lowest current variation (ΔI) of only 6% across the temperature range, reflecting minimal performance degradation under thermal stress. Furthermore, it is classified as a Type II device at 25°C , indicating favourable thermal performance characteristics. However, it is important to consider the value of SS and the I_{OFF} , particularly in contemporary complex sensor systems with millions of sensors. In a study reported by [2], Prashant investigated the electrostatic analysis of GAA NW using FinFET. Planar MOSFET devices have been replaced by FinFETs, bringing the CMOS technology down to 7 nm. The FinFET structure was created to achieve the desired current drive and to improve electrostatic control over planar MOSFETs, mitigating sub-threshold leakage and saturation current due to short-channel effects. As the gate length (L_g) is scaled down from 23 nm to 13 nm, the SS in FinFETs increases from 67.03 mV/dec to 89.7 mV/dec. In contrast, the SS in nanowire FETs demonstrates less variation, ranging from 64.42 mV/dec to 76.13 mV/dec across the same scaling range. Notably, when scaled to 5 nm and at $L\text{-gate} = 15$ nm, the nanowire device

maintains an SS of approximately 71 mV/dec. Interestingly, the FinFET at L-gate = 21 nm exhibits an SS equivalent to that of the nanowire at L-gate = 15 nm. Although the SS value of 64.2 mV/dec is already significant, it is too small to account for the leakage current, namely, the I_{ON}/I_{OFF} ratio, which is a very important parameter in determining the device's overall switching efficiency and performance. A summary of the previous studies is presented in Table 2.7.

Table 2.7
Summary of previous studies' main findings.

References	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	V_T (V)	Length (nm)	Material	Drawbacks
[111]	10^9	—	28	—	7	Si & Ge	Only two electrical characteristics of two different semiconductor types were examined in the study, along with the channel length.
[112]	—	85	10.0	—	10	Si	The study considered only a single-dimensional configuration for the Si-FinFET device.
[113]	4.7×10^4	—	67	—	10.4	InGaAs	The analysis was limited to channel length and two key electrical properties, specifically for the In GaAs device.
[114]	10^{13}	71	—	0.46	40	Ge	A Ge-FinFET with a 40 nm channel length was the only subject of the study; DIBL was not considered.
[119]	1.37×10^1 ₃	66.94	63.03	0.2	20	Si	The metal gate work function depends on the crystallographic orientation of the metal grains, causing random voltage threshold differences in the FinFET.
[115]	3.6×10^8	69	69	—	20	Si	The investigation was limited to a minimum channel length of 20 nm, examined only a single semiconductor material, and neglected V_T .
[116]	15.3×10^4	68	—	0.26	10	Si	The study focused on one device dimension and two electrical properties, noting a relatively low I_{ON}/I_{OFF} ratio for the Si-FinFET.
[120]	-	72.43	139.52	0.50	85	Si	FinFET still has higher SS values as oxide thickness increases, indicating that thicker oxides cannot achieve optimal performance.
[121]	10^6	73.82	84.93	-	10	Si-Ge	challenges in achieving low off-state leakage currents while maintaining high performance.
[117]	10^5	71	—	0.6	200	Ge	One semiconductor was examined, but the very long channel length produced no noteworthy findings.
[92]	2.75×10^7	63.21	207.67		7	Si	Issues with SCEs and temperature sensitivity remain in the FinFET.

2.18 FinFET Device Structure and Operation

Circuit designs based on finite FinFET I-V behaviour are generally designed using the electrical properties of FinFET I-V behaviour [117-120]. In diode mode, Bipolar transistors are used with base-to-collector connections, whereas MOSFET-based systems use a source-to-gate or drain-to-gate connection. The continuous scaling of circuits has made the efficient combination of diodes, transistors, capacitors, and resistors, the electronic components, more difficult. Their I-V characteristics significantly impact the electrical properties of these nanoscale devices, and these characteristics directly affect the performance and stability of the achievable ultra-scaled transistors. FinFET fabrication is a fairly new technology that demonstrates better performance than traditional MOSFET technology but still needs optimization.

2.19 Temperature Effects of (Si, Ge, Si_{1-x}Ge_x) FinFET

The influence of temperature is one of the most fundamental factors that directly affect the operation of FinFET transistors, particularly given the current trend toward reducing device size and the emergence of new materials, such as Ge and Si_{1-x}Ge_x alloys, as possible substitutes for traditional Si. Among the most noticeable processes accompanying the rise in temperature in these transistors is the Self-Heating Effect (SHE), which increases with decreasing device size and increasing channel current density. This effect can raise chip temperature to levels that degrade electrical performance, increase leakage currents, and shorten the operational life of electronic equipment.

The analyses of FinFET transistors built on Si_{1-x}Ge_x materials revealed that the SHE increases significantly with increasing Ge concentration [124]. Calibrated simulations demonstrated that, in Ge transistors, the temperature can be about 50°C higher than in Si counterparts. This large disparity is explained by Ge's low thermal conductivity, one of its undesirable natural properties in such a situation. Even though Ge and Si_{1-x}Ge_x compounds exhibit high carrier mobility, a strong point for enhancing device speed and minimizing performance loss, this is offset by a major thermal problem: poor thermal dissipation [125]. To improve the accuracy of computational models for thermal analysis, the thermal characteristics of the materials, especially the thermal conductivity coefficient (k), were initially calibrated using experimental

thermo-electrical measurements. The findings indicated that several factors, such as operating temperature, material thickness, and impurity concentration, influence this coefficient. These variables underscore the need for accurate thermal modelling at the material level to provide a realistic physical model of thermal behaviour in FinFET transistors [126].

Notably, the rise in chip temperature is observed to cause instantaneous performance degradation and to alter device properties, including I_{OFF} and time-to-failure rate. Effective cooling and thermal device design are critical issues in advanced manufacturing technologies. The high carrier mobility of $\text{Si}_{1-x}\text{Ge}_x$ materials could also be used to reduce thermal losses by lowering the operating voltage to below 0.8 V, which has been reported to help mitigate self-heating [127].

With this in mind, the thermal characteristics of FinFET transistors composed of Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ represent a significant milestone toward the development of more reliable and efficient logic technologies. The extensive body of research on self-heating, whether experimental or theoretical, provides a strong scientific basis for setting limits to technological miniaturization without compromising thermal stability or operational reliability [128].

2.20 Simulation of FinFET Characteristic

FinFETs have been proposed as an alternative to the venerable planar MOSFETs for the design of nanoscale devices. Their multi-gate format provides enhanced electrostatic control of the channel, which helps reduce irritating short-channel effects such as threshold-voltage roll-off and DIBL. Simulation tools are essential for analysing and optimizing these devices in any research laboratory or classroom project.

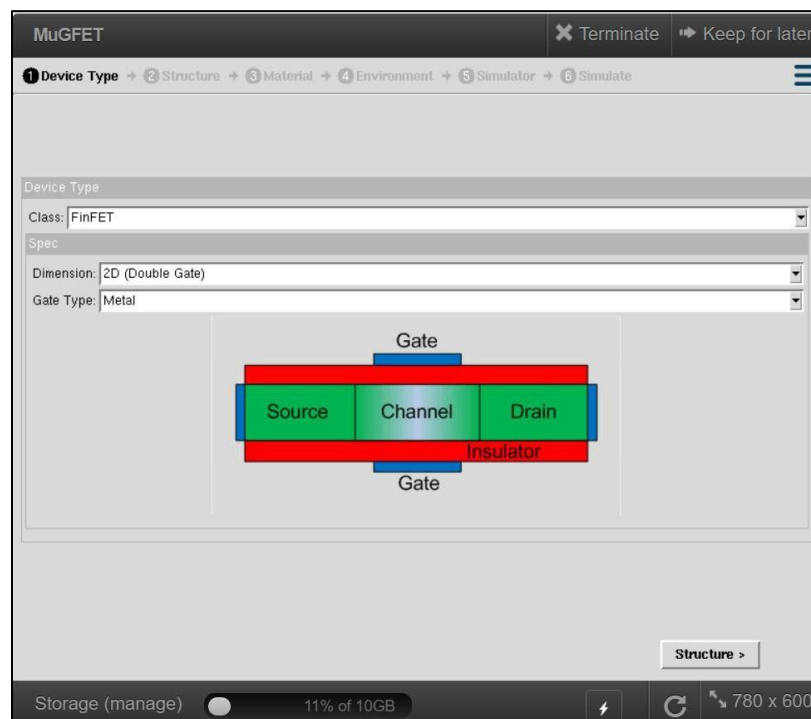
A popular platform is nanoHUB.org, which offers access to advanced semiconductor simulation tools in the cloud. The best of them is the MuGFET (Multigate FET) simulator, which is highly flexible in simulating FinFET behaviour at the nanometre scale. MuGFET allows users to design and test FinFET structures using an interactive, browser-based interface without installing software.

The simulator has been designed to support both the two-gate and three-gate designs, and device parameters, such as gate length, fin size, doping, and operating temperature, can be adjusted. It can produce current-voltage characteristics and be used to model the influence of material properties and geometry on device performance.

These characteristics are necessary for determining key parameters such as threshold voltage, sub-threshold slope, and the on-to-off current ratio.

Figure 2.14 illustrates the basic components of the simulation process. The presented screenshots represent common results from MuGFET: the transfer characteristic (I_d - V_g) curve, indicating the current response to different gate voltages, the electrical characteristics of carrier mobilities and dielectric constants, and a simplified schematic of a double-gate FinFET detector. All these constitute the progression from structural configuration to material choice to performance analysis.

The MuGFET tool is especially well-suited to investigate FinFETs based on $\text{Si}_{1-x}\text{Ge}_x$, as it allows exploration of channels with mixed materials of different compositions and temperatures. It is possible to model accurately the effects of Ge content and structural dimensions on electronic behaviour, which are important for optimising FinFETs at leading technology nodes.



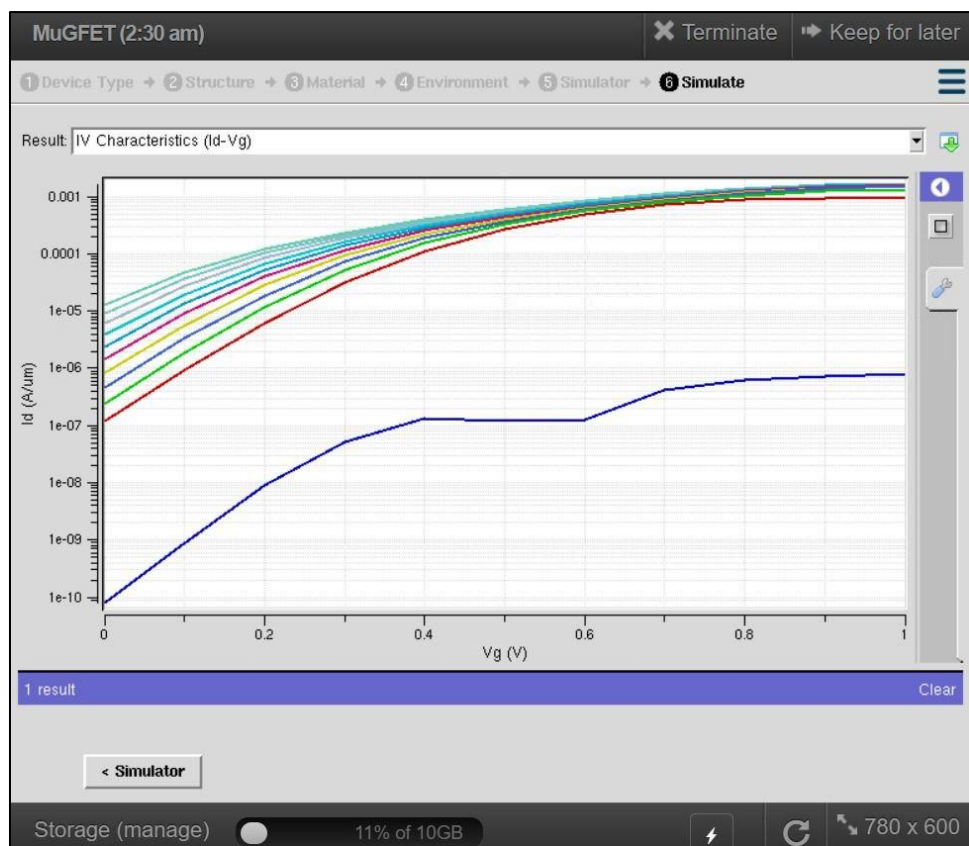
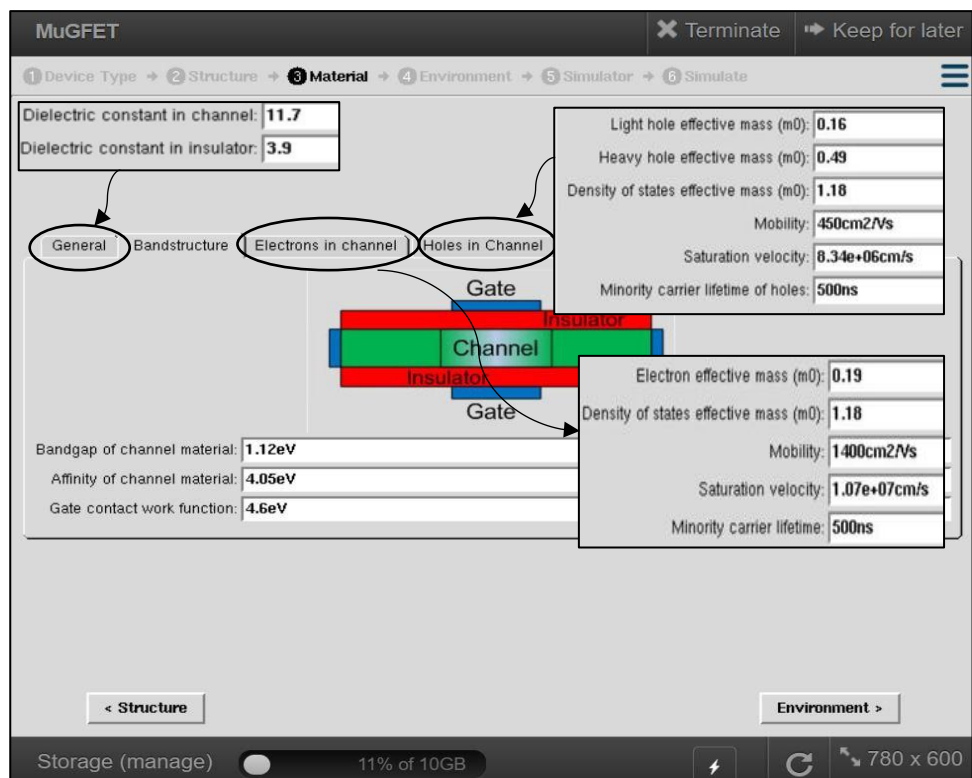


Figure 2.14 Screen shots of MuGFET device simulator.

2.21 Summary

This chapter discussed the fundamentals of FETs and the development of the MOSFET, the most popular FET. The concept of FinFET technology has brought about tremendous improvements in device design, fabrication methods, and overall performance. The implications of SCEs were briefly reviewed, which occur due to the aggressive scaling of FET transistors, and specifically the effects they have on electrical power consumption. The functionality of CMOS devices and the advanced features of FinFET transistors were also described. In 2017, Intel demonstrated new FinFET technologies in line with Moore's Law, where transistors are miniaturized to a channel length of 10 nm. It concerned the electrical properties of transistors, which are the main standards for measuring FinFET quality and determining its advantages and disadvantages. Important parameters in performance diagnosis include the I_{ON}/I_{OFF} ratio, SS, DIBL, and V_T . This chapter involved a comparative study to examine the role of various semiconducting materials, such as Si, Ge, and $Si_{1-x}Ge_x$, on the electrical properties of transistors, with the view presented in earlier literature in mind.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Introduction

The chapter presents the research methods and theoretical basis. The characteristics of FinFETs are discussed, along with key variables that influence transistor performance, such as DIBL, SS, and V_T .

In this study, MUGFET, a simulation tool, was used. To begin with, appropriate parameters and measurements were selected for the FinFET simulation: T , T_{ox} , W_g , and L_g . The I-V data were obtained after the simulation was run with the specified parameters. The I-V dependence on V_T , SS, and DIBL was examined after identifying all geometric parameters (L_g , W_g , T_{ox}) and the operating temperatures. When the selection of dimensions was inaccurate or incomplete in the first round, the simulation was repeated to narrow and refine the parameters. This iterative method provided proper modelling and allowed optimal channel configurations to be identified. The optimized values eventually provided were those that optimized the thermal and electrical performance of the FinFET structure. Figure 3.1 summarizes the whole process of the research.

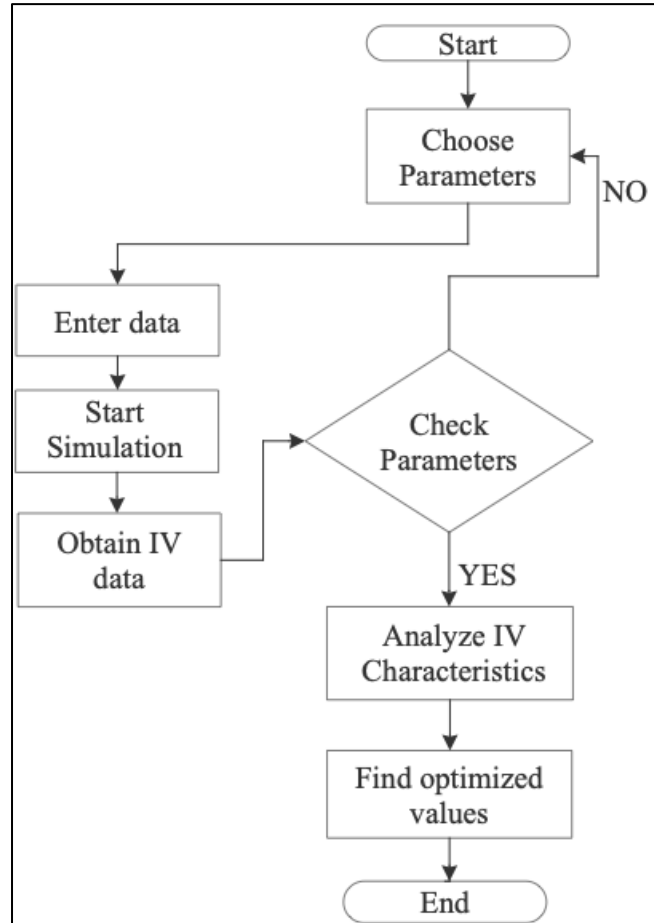


Figure 3.1 Methodology flowchart of this research.

3.2 Simulation Model

The most important technique for comprehending machine operations and assessing FinFET performance is simulation. The use of simulation tools significantly accelerates FinFET technology development and complements experimental research efforts [129]. The benefits of using simulation tools include cost savings and the ability to pinpoint strengths and weaknesses. This also illustrates the feasibility of nanoscale materials. A sufficient level of quantum mechanical modelling accuracy that captures atomic-scale phenomena is essential for reliable computer-aided design of semiconductor devices at the nanometre scale. Figure 3.2 depicts an illustration of the MuGFET simulation tool for nanoscale multi-gate FET structures [126-127]. The study computed the I-V characteristics of the driver and/or load transistors of the FinFET inverters with specific physical parameters. The MuGFET uses either the Bell Laboratories PROPHET or PADRE simulators, as presented in Figure 3.2. The abbreviated form PROPHET refers to a PDE solver designed to address problems in one, two, or three dimensions. One device-oriented simulator is PADRE, which can

simulate 2D and 3D devices with any geometry [131]. While this simulator produces many helpful graphs for engineers, it requires a deep understanding of physics. The drift-diffusion and Poisson equations are self-consistently solved by MuGFET [130]. The simulation of electrical devices is becoming increasingly important for a full understanding of device physics. In this study, the performance limits of FinFET structures are analysed and evaluated using simulation techniques. This experimental work can be supplemented with simulation tools that enable the development of MuGFETs at micro-scale dimensions [132]. In addition to identifying their advantages and disadvantages, simulation tools can also demonstrate their extensibility down to the nm range and the cost of retrenchment devices [129-130]. The FinFET simulation tool homepage is illustrated in Figure 3.2.

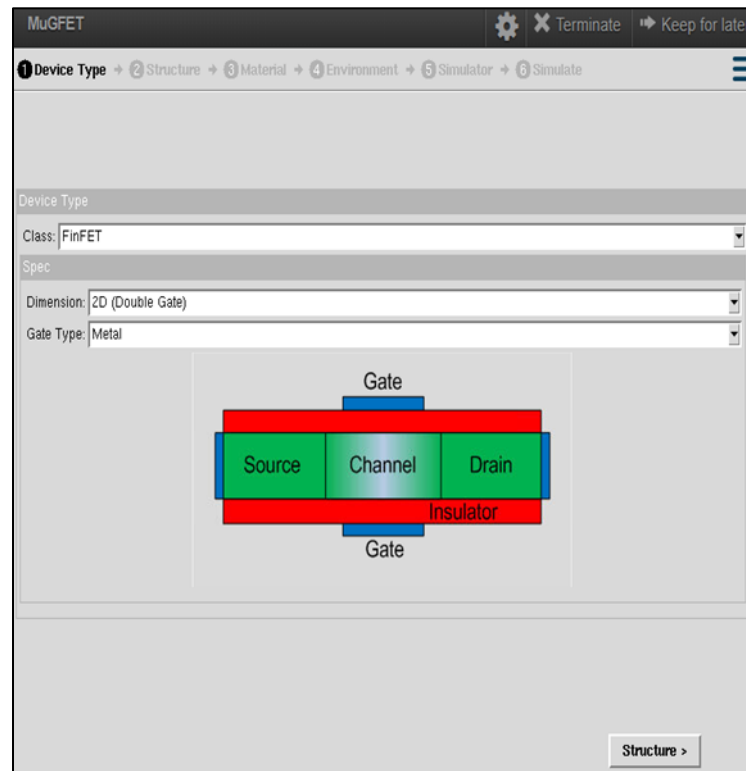


Figure 3.2 Homepage of FinFET simulation tool.

3.3 Simulation Design

As part of the electrical characterization of $\text{Si}_{1-x}\text{Ge}_x$ -based FinFET structures, a structured simulation methodology was adopted to analyse the influence of device dimensions and thermal operating conditions. This study focuses on understanding how variations in gate length, under fixed material and physical constraints, affect the performance of nanoscale FinFETs. The simulations were conducted by varying the

gate length to 10, 20, and 30 nm to demonstrate how features shrink in sub-35 nm tech. These numbers were of interest for studying short-channel effects, such as DIBL and threshold-voltage roll-off, which are more severe with shorter gates. Channel lengths of 10, 20, and 30 nm were chosen to represent three scaling ranges: aggressively scaled (10 nm), moderately scaled (20 nm), and near long-channel behaviour (30 nm). At 100 nm, short-channel effects are negligible, and the device behaves as a long-channel MOS transistor with minimal electrostatic coupling between the source and drain. Therefore, 100 nm is not an advanced nanoscale operation relevant to modern CMO nodes [71]. The gate width was kept constant at 10 nm to maintain the fin shape. The oxide thickness was also held constant at 1 nm, maintaining gate control and avoiding additional variability due to dielectric scaling. The simulation framework was also temperature-dependent at 275, 300, 325, and 350 K. This allows us to experiment under realistic conditions, and the sweep allows us to test the effect of heat, leakage current, and general device behaviour on carrier mobility. The chosen temperature interval (275-350 K) corresponds to practical working conditions for the use of the devices (CMOS). It includes temperatures slightly below room temperature (~ 300 K) and up to high on-chip hotspot temperatures (~ 350 K). This range is usually used in the reliability and thermal performance assessments of nanoscale transistors [135]. Above 350 K, the intrinsic carrier concentration increases significantly, leading to subthreshold swing degradation, V_T instability, and increased leakage current. Supra-400 K standard CMOS processes are limited by the reliability and integrity of the materials used, as well as by oxide [136]. Figure 3.3 presents the environment for the MuGFET simulation used to implement the defined simulation framework.

The doping levels in the channels were designed to ascertain consistency in electrostatic conductivity in both p and n regions, which meet industry-grade specifications of devices. The gate voltage ranged from 0 to 1 V, and important electrical parameters could be extracted, such as threshold voltage, subthreshold swing, and on/off current ratio. The simulation parameters were consistently applied across three major test cases targeting one of the selected channel lengths. All modelling and characterization activities in this research are based on the summary of these simulation settings presented in Table 3.1. Optimal parameters were chosen to minimise SS and DIBL while maintaining V_T within the acceptable switching window (0.3-0.6 V) for low-power CMOS design.

Table 3.1
Simulation Parameters.

Parameters	Value
Channel length (L_g)	10, 20, and 30 nm
Channel width (W_g)	10 nm
Channel oxide thickness (T_{ox})	1 nm
Temperature (T)	275, 300, 325, and 350 K
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}
Gate voltage	0 – 1 V
Drain voltage	0 – 1 V

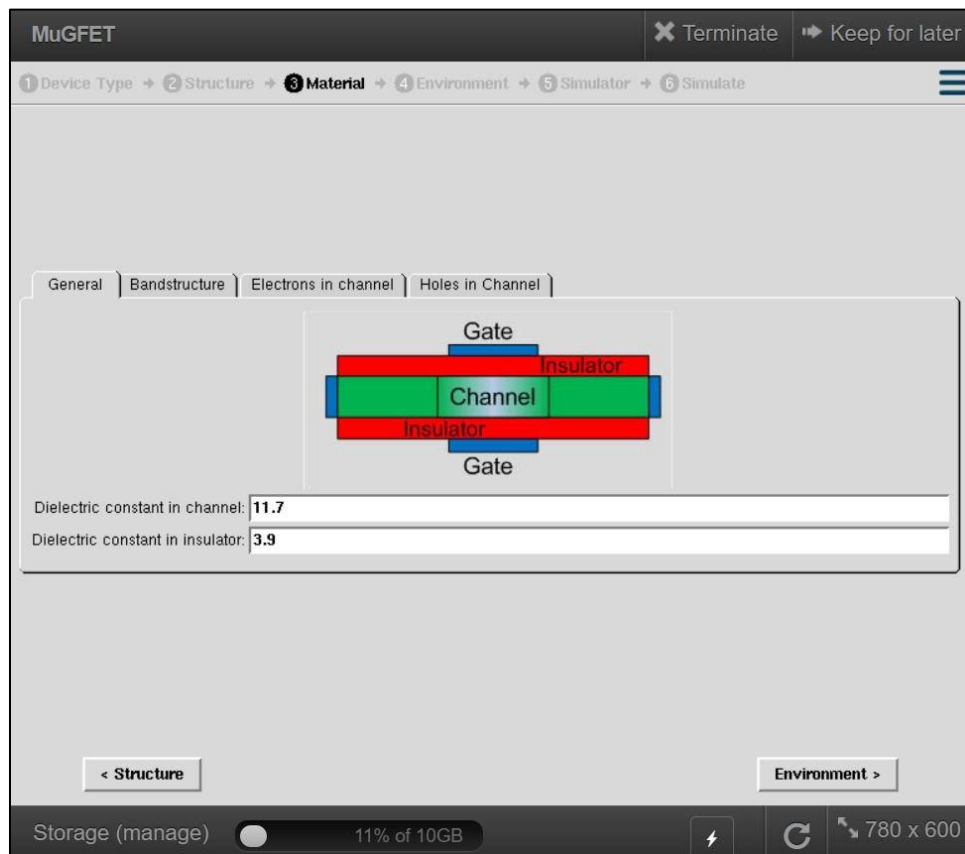


Figure 3.3 Homepage of MuGFET simulation tool.

The MuGFET simulation tool is a physics-based, nanoscale device multi-gate transistor simulator. Poisson and drift-diffusion equations are solved self-consistently, and they have been extensively employed for FinFET electrostatic analysis in academic research. MuGFET is particularly tailored for multi-gate nanoscale structures and

provides computational efficiency for parameter sweeps with compositional and geometrical variations. The focus was on electrostatic scaling rather than process-level TCAD (Technology Computer-Aided Design) calibration [36].

To implement the stipulated simulation model, the MuGFET tool was used to assess the I_d - V_g transfer properties of the $\text{Si}_{1-x}\text{Ge}_x$ -FinFET structures at different temperatures. Although systematic variation in gate length was applied throughout the simulations, the importance of the Ge composition factor (x) in the Si-Ge alloy channel was specifically considered. This enabled the close evaluation of the effects of physical scaling and material composition on device performance. Other important parameters, such as oxide thickness, channel width, and doping concentrations, were kept constant in Table 3.1 to isolate the combined effects of channel length and the Ge fraction on current conduction, threshold voltage behaviour, and subthreshold performance. The source and doping profile, as well as the drain dimension, were fixed so that all cases would be identical. Figure 3.4 below illustrates the simulation setup used to model the standardized FinFET design, enabling a consistent comparison of central FinFET structures across devices with different gate lengths and material bases. This bilateral analysis in terms of L_g and x underlies the characterization and modelling strategy used in this work.

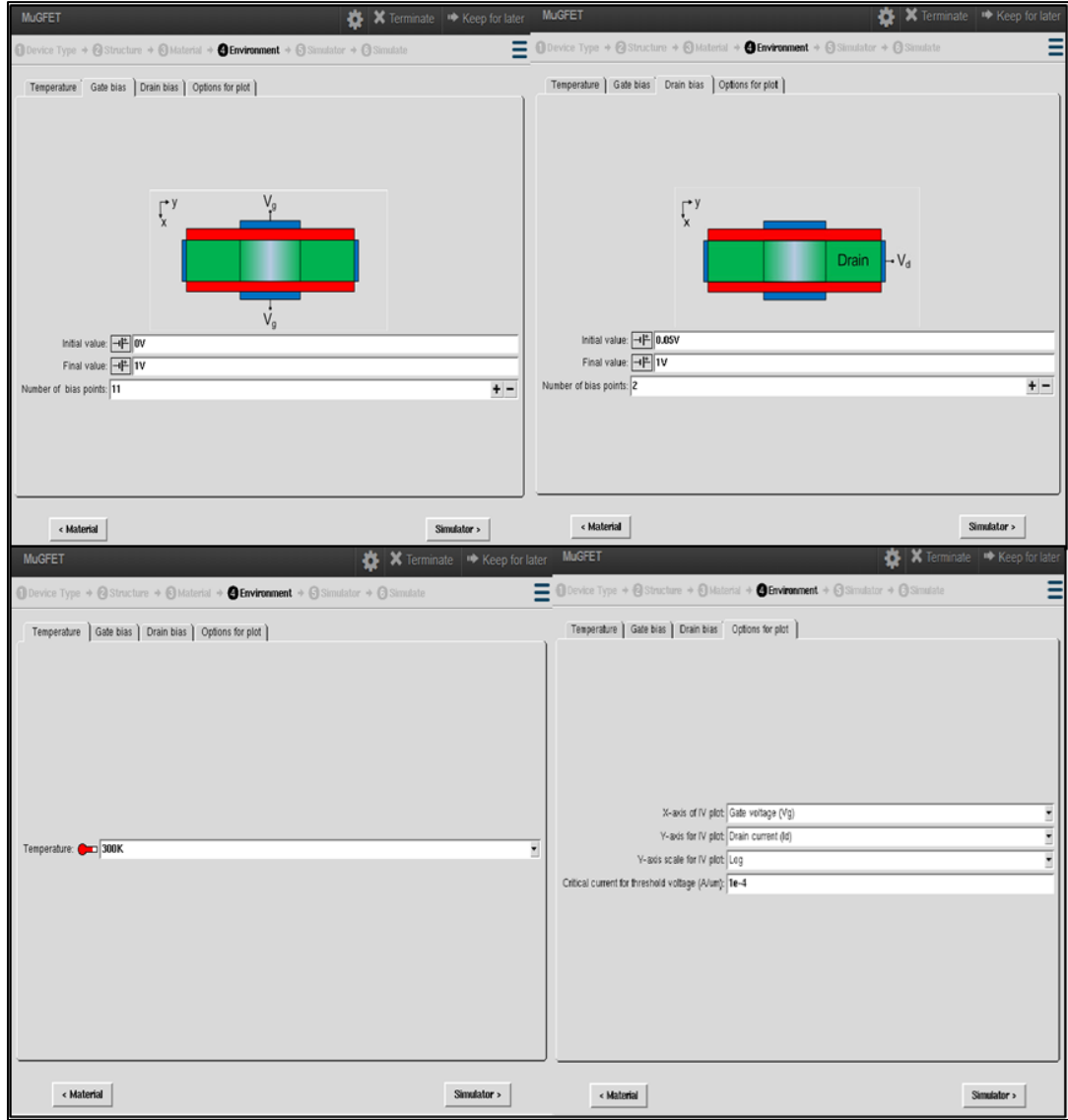


Figure 3.4 Environment of FinFET on MuGFET simulation tool homepage.

3.4 Selection of Channel Dimensions

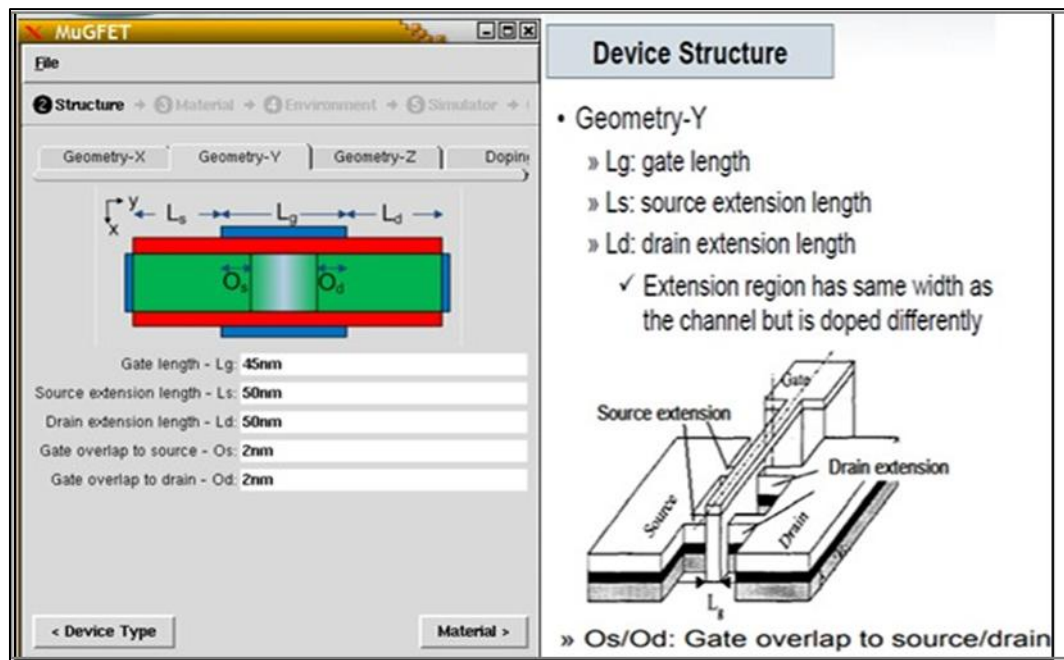
The channel dimensions used in the present study were chosen to analyse FinFET structures of $\text{Si}_{1-x}\text{Ge}_x$ under real-scale and thermal conditions. Channel length was also chosen as the primary dimensional parameter, with values of 10, 20, and 30 nm to meet the needs of advanced technology nodes. Conversely, the channel width (10 nm) and the oxide thickness (1 nm) were kept constant throughout all simulations to ensure structural integrity and isolate the contributing factors (length and material composition). It was implemented to explore the effects of mutual interference between gate length and Ge mole fraction (x) on key electrical properties, including threshold voltage, leakage current, and subthreshold swing. The interplay between the physical scaling changes and band structure changes with incorporation of Ge was also examined

as a variable of temperature under a specified range of 275-350 K. Using such a dimensional framework, the research demonstrates a direct relationship between device geometries, material structures and thermal performance upon which real modelling and characterization of the FinFET behaviour under aggressive scaling environments can be prepared.

3.5 Channel Length

The gate length (L_g), or channel length, is one of the basic parameters in the design and operation of FinFET transistors [137]. It is defined as the physical distance between the drain and the source. As transistor dimensions decrease, channel length reduction is very important for improving device performance and integration. Nevertheless, this miniaturization poses great challenges, especially in the development of SCEs [138]. Short-channel effects observed in FinFET structures include threshold-voltage roll-off, SS degradation, and DIBL. When the channel length is shorter, the gates' electrostatic control is weaker, leading to lower switching efficiency and greater sensitivity to the drain voltage. On-current increases with shorter channel resistance, whereas transconductance generally decreases with longer channel length due to reduced carrier speed [139]. Three FinFET layouts were used to examine the effect of L_g , with channel lengths of 10, 20, and 30 nm. The gate width ($W_g = 10$ nm) and T_{ox} (1 nm) were held constant in all cases, isolating the effects of channel-length variation. Figure 3.5 illustrates the simulated FinFET device structure and the geometrical parameters employed in this study: the L_g , the source and drain extension lengths (L_s and L_d), and the gate overlap regions. Based on the device geometry, electrical characteristics, including V_T , SS, DIBL, and I_{ON} , were then obtained under favourable biasing conditions, as addressed in the following sections.

FinFET technology is efficient at controlling short-channel effects, with the added benefit of a 3D gate structure and excellent electrostatic control. Additional optimization of the thermal stability and performance of the devices can be achieved through fin-geometry and gate-length design, as well as material engineering (e.g., the use of $Si_{1-x}Ge_x$ alloys) [140]. Optimized channel dimensions, especially 20 nm and 30 nm, coupled with an appropriate x-ratio in Si-Ge, enable FinFET devices to operate over a wide range of thermal conditions. This renders them viable candidates for sophisticated nanoscale applications sensitive to temperature.



3.6 Channel Width

The most basic design aspect of FinFET transistors is channel width, which is usually determined by the fin thickness. With triple-gate FinFETs, the calculation of the effective channel width is given as $2H_{\text{fin}}$ (fin height) + W_{fin} (fin width).

Narrow fins improve electrostatic control by the gate and help suppress short-channel effects [141]. With a decrease in fin width, stability in threshold voltage, subthreshold slope, and switching efficiency is enhanced [142]. Nonetheless, a smaller fin contributes to higher parasitic resistance, which reduces the on-current and transconductance [143]. When the fin width scales down to nanoscale dimensions, the quantum confinement effect begins to dominate, affecting carrier transport and tunneling behaviour [144].

The channel width and oxide thickness were held constant at 10 nm and 1 nm, respectively, in this study. The effect that these fixed dimensions had on device behaviour was evaluated through electrical simulations. In this study, the fin width is defined and illustrated in Figure 3.6 of the device geometry. This number is used to explain the structural parameters applied in the simulations, and the effects of fin-width optimization on electrostatic control and current drive will be determined in another results section. This equilibrium is necessary for efficient FinFET design in $\text{Si}_{1-x}\text{Ge}_x$ channel material across different temperature regimes [145].

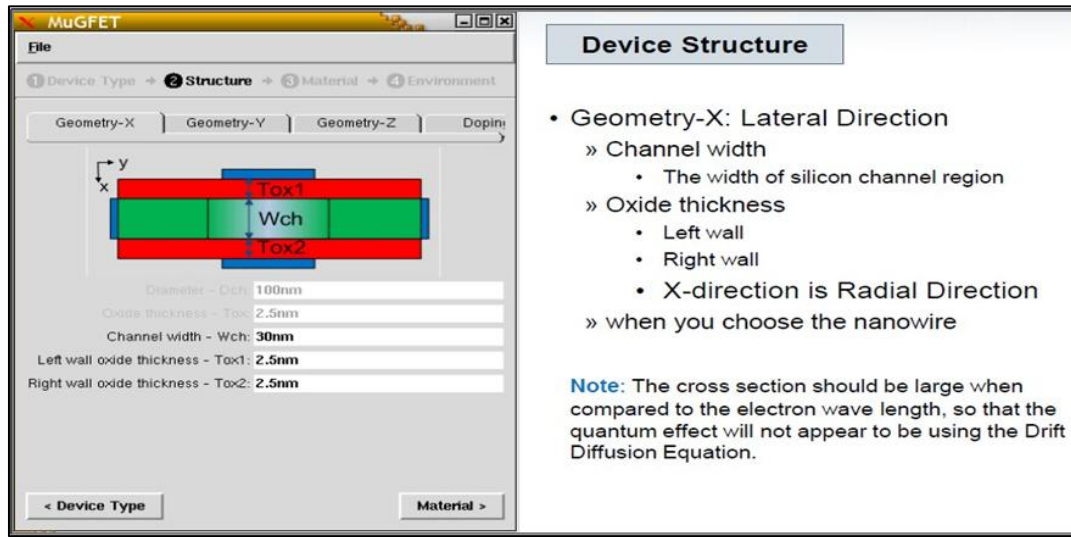


Figure 3.6 Variation in channel width and corresponding oxide thickness.

3.7 Oxide Thickness

The oxide thickness, also known as the gate oxide thickness or Equivalent Oxide Thickness (EOT), in FinFET transistor design is an important design parameter. It affects electrostatic channel regulation, gate leakage, and the device's overall performance [146].

In the given experiment, the oxide thickness is maintained at 1 nm to eliminate its variability and examine the impact of other variables. This constant enables a closer analysis of the impact of the L_g , W_g , and $\text{Si}_{1-x}\text{Ge}_x$ composition ratio on the device's behaviour across various temperature regimes. An oxide coating 1 nm in thickness provides a high level of gate control, virtually suppressing SCEs and enhancing electrostatic stability [147]. Tunneling leakage through the gate dielectric, however, can be important at this scale. To reduce this problem, high-k materials such as HfO_2 are used. These materials have low EOT and less leakage current [148].

The simulated structure has symmetrical oxide layers 1 nm thick on both gate sidewalls, as depicted in Figure 3.6. This design ensures that all models of the equipment have similar electrostatic conditions. The simulation findings are valid for isolating the effects of geometric and material parameters on the main performance indicators of threshold voltage, subthreshold slope, DIBL, and I_{ON} by maintaining a constant oxide thickness. This modelling approach provides better insight into the operation of $\text{Si}_{1-x}\text{Ge}_x$ -FinFET at nanoscale conditions and aids in optimizing the structure for thermally stable, high-performance applications [149].

3.8 I–V Characteristics

Current-voltage (I_g - V_d) characteristics are another key feature of transistor behaviour. They explain the behaviour of the current in terms of the applied voltages and help evaluate the device's behaviour across various operating regions, such as subthreshold, linear, and saturation [150]. The simulation feature of the MuGFET tool has been used in this study to systematically extract and analyse the electrical properties of the proposed FinFET structure. The methodology used in the characterization of I and V and the extraction of parameters is summarized in Figure 3.7-3.9. Figure 3.7 illustrates how the major short-channel performance measures, V_T , SS , and $DIBL$, can be obtained from transfer characteristics extracted under well-defined biasing conditions. Figure 3.8 introduces a selection of suitable transfer (I_d - V_g) and output (I_d - V_d) properties, which are key to the proper evaluation of gate electrostatic control and current-delivery capacity. Figure 3.9 depicts the channel-length scaling effect on device performance, enabling a systematic evaluation of electrostatic integrity, short-channel effects, and scaling behaviour across different FinFET configurations, with all three variables directly related to switching efficiency, leakage behaviour, and overall device reliability. The extracted values were thoroughly analysed and compared across the studied device geometries using the basic properties of the current-voltage characteristics.

1. Transfer Characteristics (I_d - V_g): These are used to obtain SS and V_T . The shorter the channel gates are, the worse the channel performance is at subthreshold. Nevertheless, narrowing of the fin enhances control on the gate and switching characteristics [151].
2. Output Characteristics (I_d - V_d): These help characterize the saturation behaviour and measure the on-current. The smaller the gate length, the higher the drain current is usually, since there is less channel resistance [152].

Parameters such as the fin thickness, doping levels, and the gate work function directly influence these traits. For example, while increasing the gate work function enhances SS , $DIBL$, and the on/off current ratio, this can decrease the overall drive current [153]. There are also corner effects, which may cause unwanted kink behaviour in the transfer curve, particularly in narrow fins. Using these I - V curves, the thesis demonstrates the effects of major geometric and material parameters on FinFET performance. This modelling helps streamline the optimization of the FinFET

architecture of $\text{Si}_{1-x}\text{Ge}_x$ -based structures to support device operation at reduced size and across different temperatures.

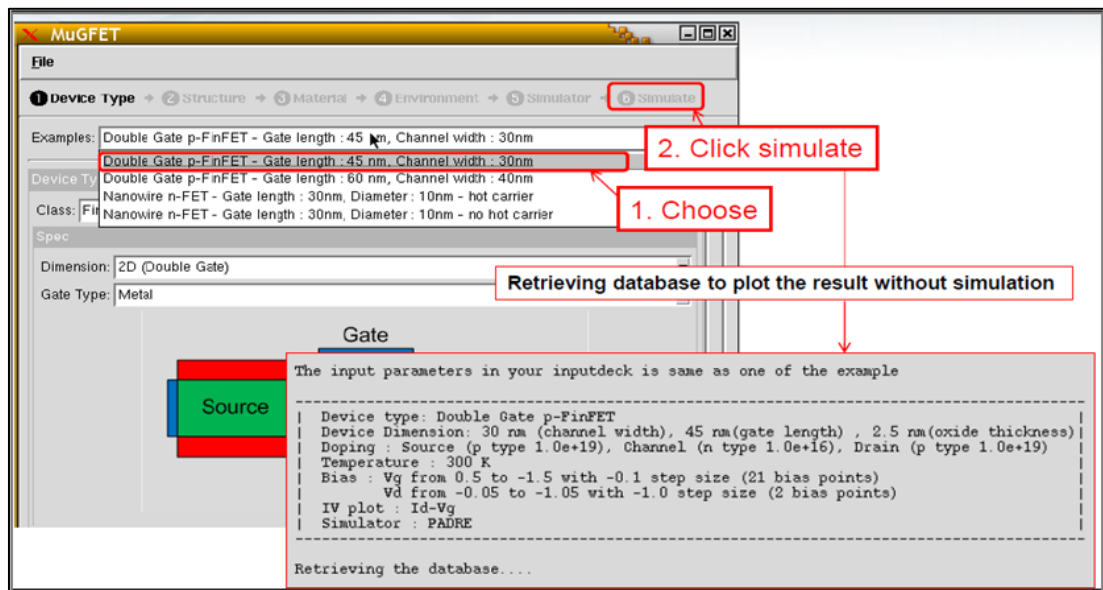


Figure 3.7 Extraction of S_S , V_T , and DIBL parameters via the 'simulate' function.

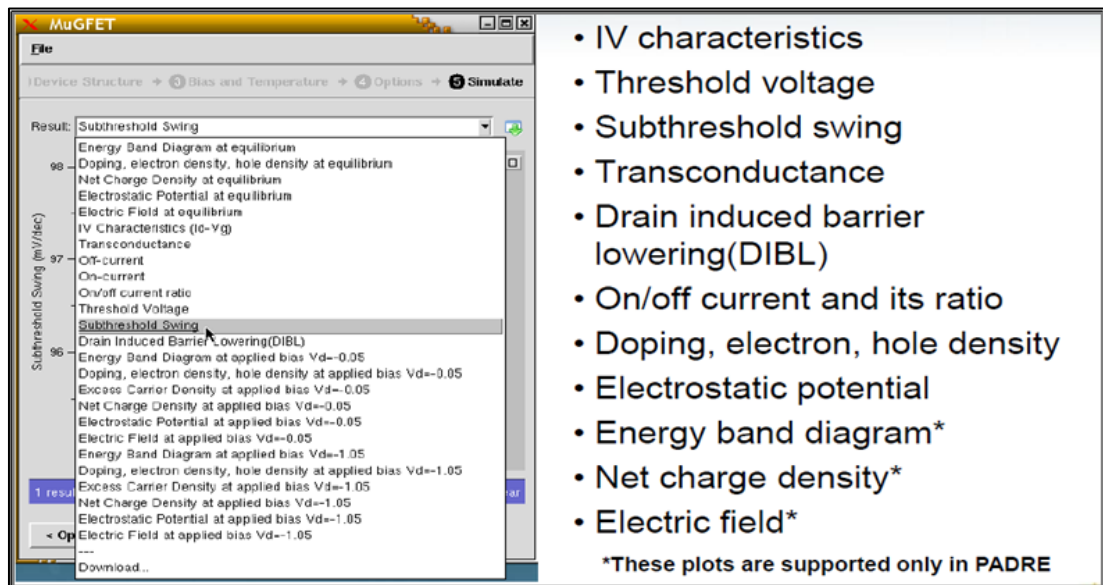


Figure 3.8 Specification of the electrical characteristic type selected for analysis.

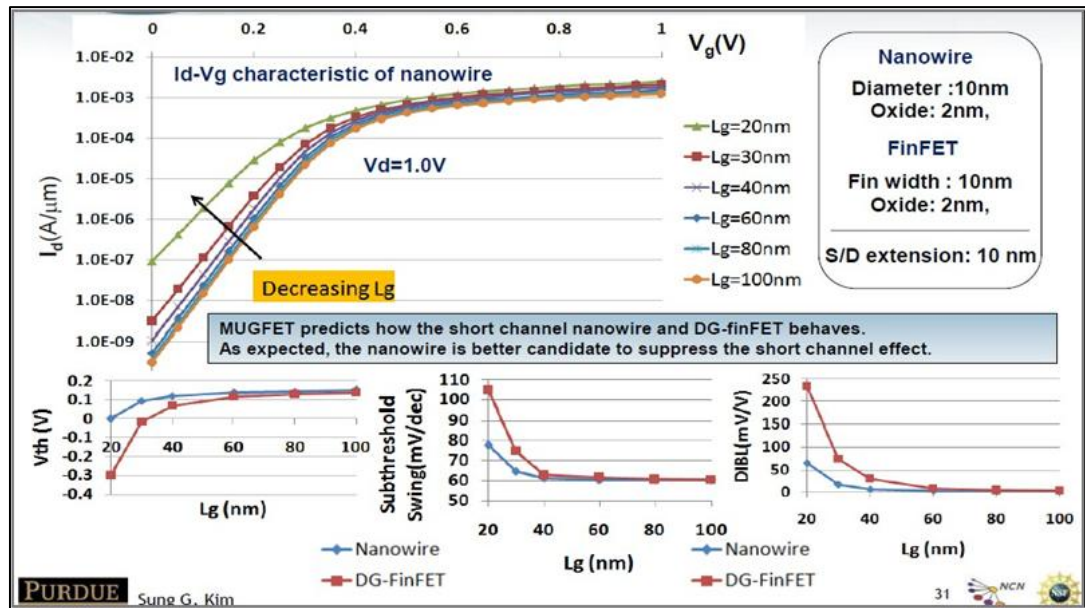


Figure 3.9 Procedure for extracting and plotting electrical characteristics as a function of channel length variation (20–100 nm) in FinFET and nanowire structures.

3.9 Summary

In this chapter, the simulation methodology and the theoretical framework used to analyse the electrical properties of $Si_{1-x}Ge_x$ FinFET designs were presented. It focused on the important design parameters (channel length, channel width, and oxide thickness) and analysed their impact on device performance under different temperature conditions. The I-V characteristics were also studied, and therefore critical features such as V_T , SS, and DIBL were measured. Furthermore, the chapter described the simulation tools employed and the processes undertaken to extract and plot the appropriate electrical characteristics. The results of these analyses serve as a basis for modelling and optimizing FinFET devices used in high-performance, thermally stable applications.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

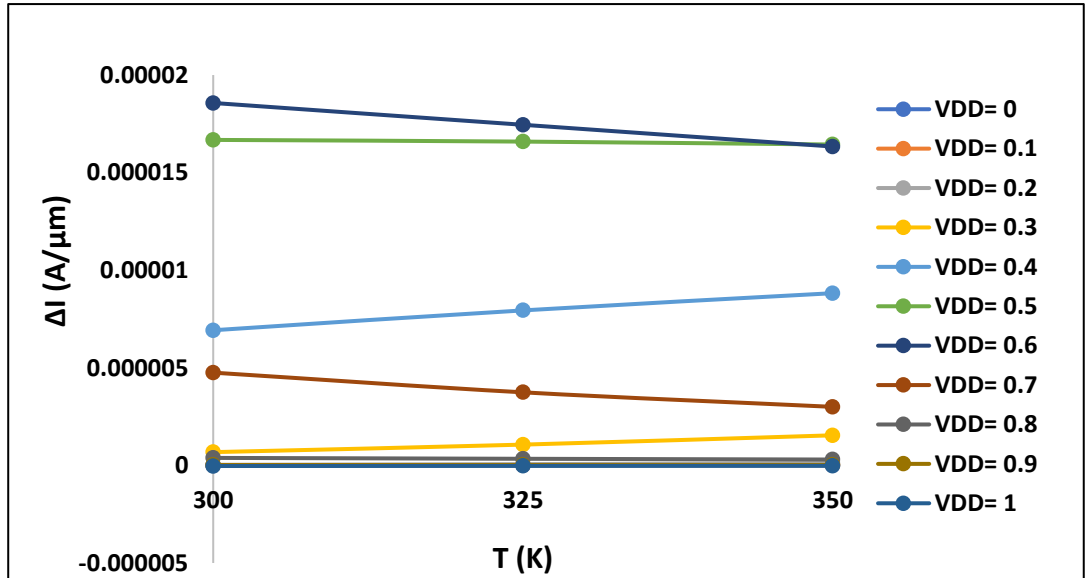
This chapter examined simulation results and the relative electrical properties of FinFET transistors made of Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ under various channel lengths. The transistor I-V behaviour has been investigated using predefined simulation parameters and conditions. It analyses the effects of channel length, width, oxide thickness, and the oxide gradient factor on the overall efficiency of FinFET devices, with a focus on material selection. I_d - V_g characteristics of Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ transistors were simulated under normal conditions and at 300 K. The theoretical minimum subthreshold swing, SS_{ideal} , at room temperature was recorded to be 59.5 mV/dec. Furthermore, the four simulation experiments were aimed at comparing the performance of (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$)-based FinFETs based on the chosen performance parameters. In the former case, the effect of temperature on FinFET properties was examined by varying the operating temperature while keeping L_g , W_g , and T_{ox} constant. The second case maintained the same physical size and used Si as the base material, with temperature variation used to further determine its influence on device behaviour. The third case examined the interplay between temperature and the addition of 0.25% Ge on FinFET characteristics. The third and fourth cases set the Ge content to 0.50 and 0.75, respectively, to determine the gradual changes in performance. In the latter, the material was 100% Ge, which enabled the investigation of temperature-dependent trends in an all-Ge FinFET. In addition to the effects of material composition and temperature, this work also examines the impact of critical physical dimensions (gate length and channel geometry) on the I-V characteristics of FinFET devices. This kind of analysis is necessary to analyse the performance, especially as these transistors are made in the deep-nanometre regime. It is observed that subthreshold behaviour is highly sensitive to changes in channel length and fin thickness, underscoring the need for tight control over these dimensions. A more specific analysis of the subthreshold behaviour of (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$)-FinFETs, focusing on the interactions among T , L_g , and channel composition, is presented in the following sections using the methodology outlined in Chapter 3.

4.2 Effects of Channel Length on Si-FinFET Characteristics

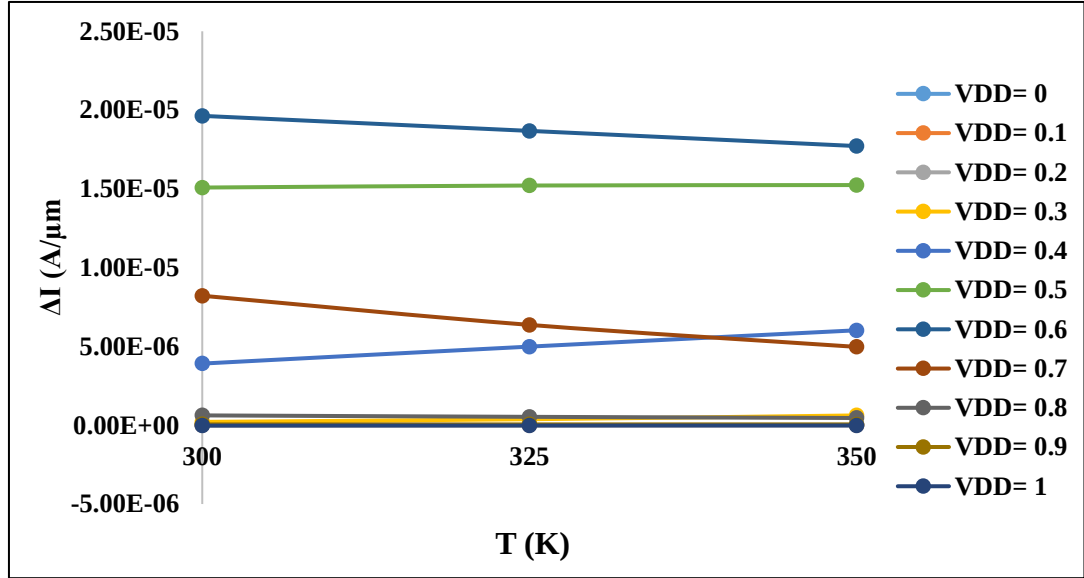
The I_d - V_g properties of FinFETs were modelled at different temperatures (275, 300, 325, and 350 K) with the following parameters: channel concentration (P-type) = 10^{16} cm^{-3} , source length = 50 nm, drain length = 50 nm, source and drain concentration (N-type) = 10^{19} cm^{-3} , oxide thickness = 1 nm. The L_g values considered are 7, 10, and 20 nm. Figure 4.1, 4.2, 4.3, 4.4, 4.5, and 4.6 display these characteristics.

4.3 The Si-FinFET Scenarios

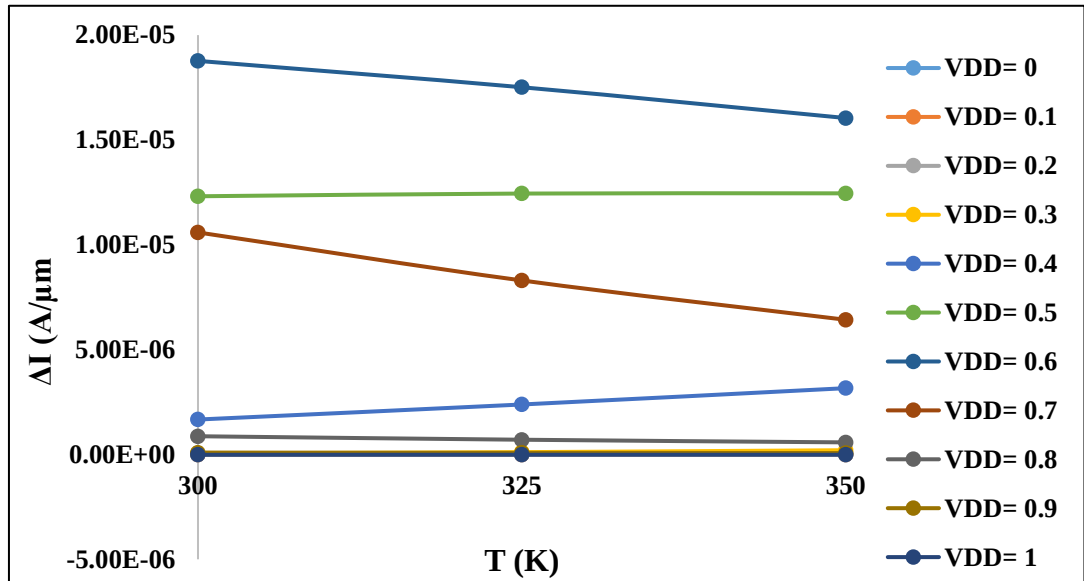
Figure 4.1(a–c) illustrate current (I) variation with L_g of 7, 10, and 20 nm with a voltage change of 0.1 V. As temperature increases, the values indicate a reduction in sensitivity in some instances, but in others, a small increment in sensitivity is recorded with peak sensitivity (maximum ΔI) at lower temperatures. Figure 4.1(a) and (b) depict the best temperature sensitivity coefficients at $V_{DD} = 0.6 \text{ V}$ in L_g values of 7 nm and 10 nm, respectively, and Figure 4.1(c) displays the lowest sensitivity at $L_g = 20 \text{ nm}$ at $V_{DD} = 0.6 \text{ V}$. The above findings indicate that the transistor can operate at an optimal condition, which is stable over the 325–350 K temperature span and corresponds to a V_{DD} of 0.6 V, as portrayed in Figure 4.1(a–c).



(a)



(b)

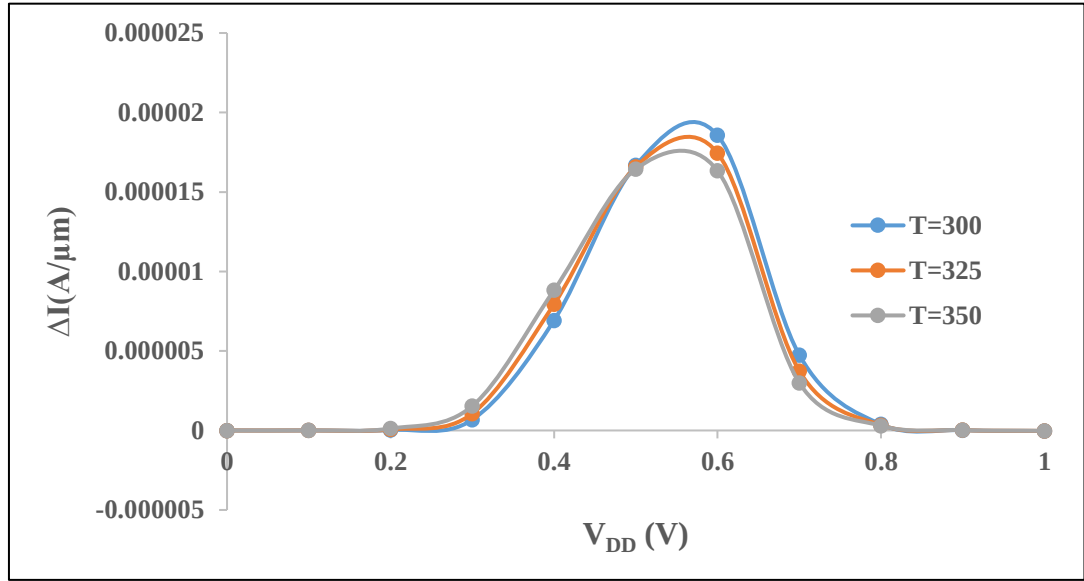


(c)

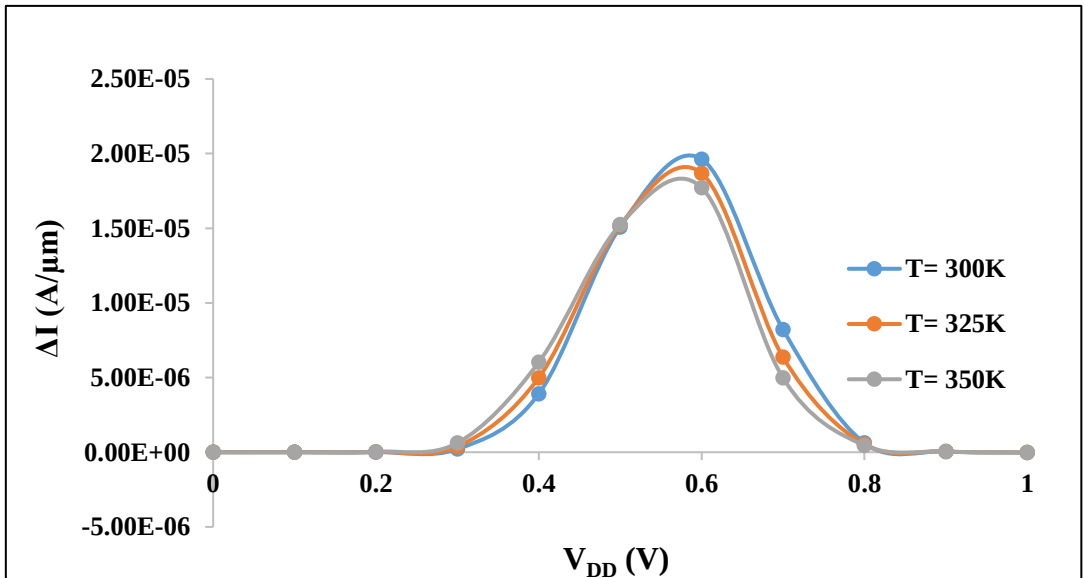
Figure 4.1 ΔI -T characteristics of FinFET (a) $L_g = 7$ nm; (b) $L_g = 10$ nm; (c) $L_g = 20$ nm.

Figure 4.2(a-c) illustrate the variation of ΔI with V_{DD} at temperatures of 275, 300, 325, and 350 K for L_g values of 7, 10, and 20 nm. Even though V_{DD} is held constant at 0.6 V, variations in L_g have a strong influence on ΔI . The maximum sensitivity (ΔI

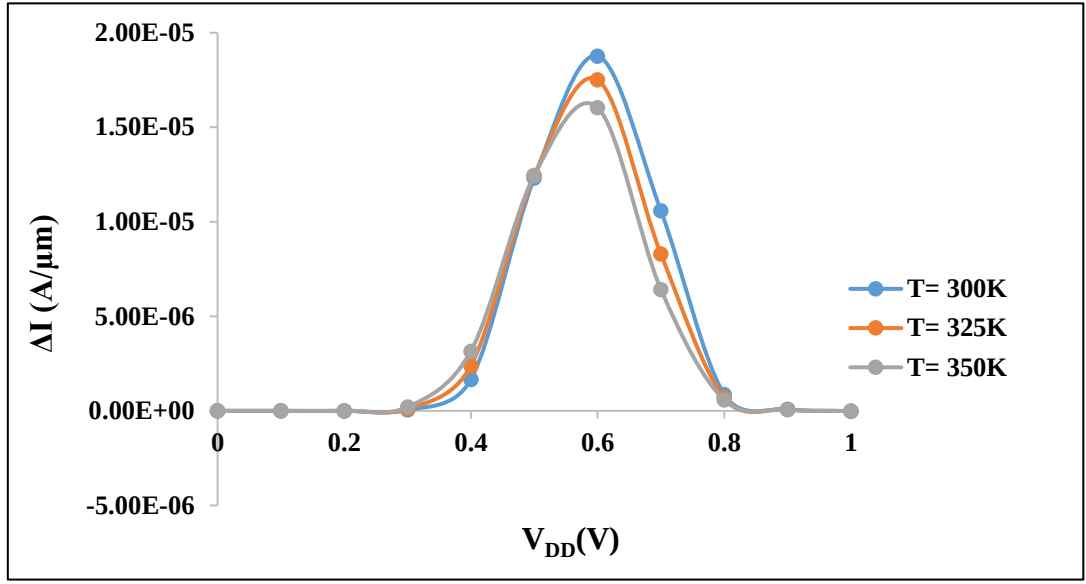
max) is observed at $L_g = 10$ nm, and with increases in L_g to 10 and 20 nm, its sensitivity declines. These observations indicate that although ΔI rises with temperature, changes in gate length are the main determinants of ΔI , with all other factors remaining constant. This aligns with earlier research, which indicates that ΔI is coherent with L_g , and that longer gate lengths yield a more stable current response under constant-voltage conditions, similar to that of other related semiconductor devices [154].



(a)



(b)



(c)

Figure 4.2 Characteristics of ΔI with V_{DD} at (a) $L_g = 7$ nm, (b) $L_g = 10$ nm, (c) $L_g = 20$ nm.

The relationship between ΔI and L_g is illustrated in Figure 4.3, which reveals that ΔI varies with channel length. As depicted in the graph, the initial increase in ΔI reaches a L_g of 10 nm, after which the peak value declines as the channel length increases further. In particular, channel lengths of 7, 10, and 20 nm yield ΔI values of 1.86, 1.96, and 1.88 A/ μ m, respectively. The trend indicates that as the channel length increases, the initial effect is an enhancement of electrostatic control and current. The current then decreases slowly as the channel length increases further. The decrease in current is mainly due to the increased resistance with increasing gate length, thereby reducing the total current. Longer gate lengths increase device stability and reduce short-channel effects, reducing drive current, which is a vital element in performance optimization, particularly in low-power applications.

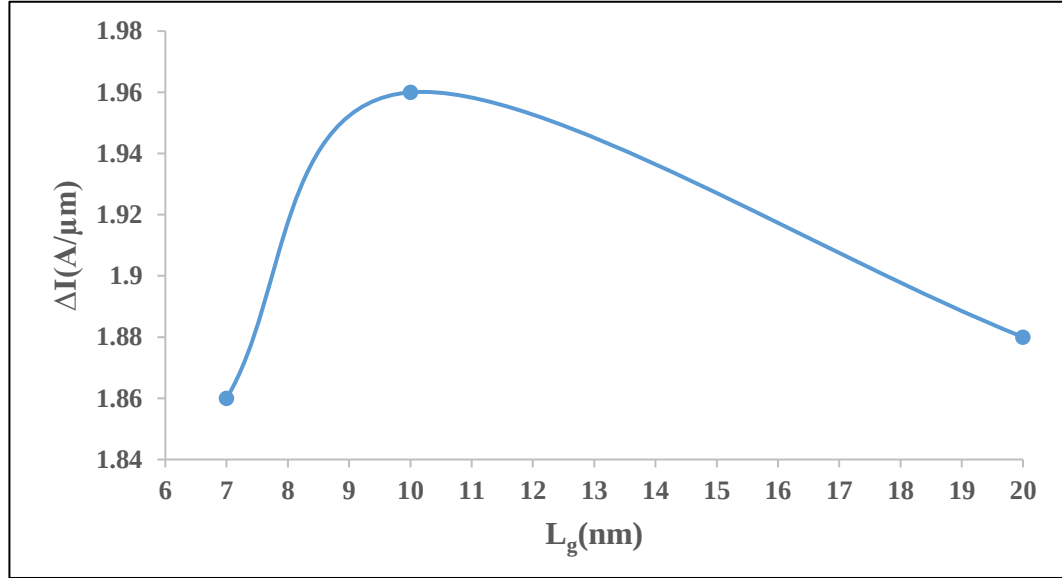


Figure 4.3 Characteristics of ΔI with L_g .

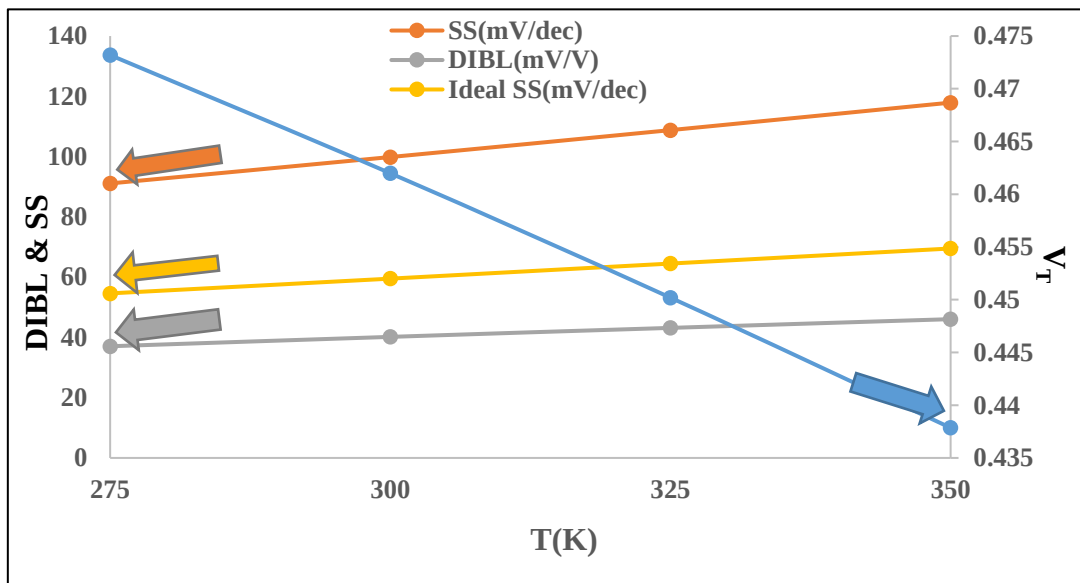
Figure 4.4(a) demonstrates the temperature-related trend of DIBL, V_T , and SS of one FinFET device with L_g of 7 nm, at temperatures of 275, 300, 325, and 350 K. V_T had a linear decrease with temperature, with a decrease of 0.47 V at 275 K and 0.43 V at 350 K. At 275 K, the SS value was 91 mV/dec and, as the temperature rose, the value rose steadily. At 350 K, its value was 117.9 mV/dec. The latter value slightly deviates from the ideal SS value of 69.5 mV/dec. Nevertheless, the SS value at $L_g = 7$ nm (91 mV/dec) was not close to 54.6 mV/dec, which would be expected at 275 K, but was within an acceptable range of SS values. The temperature dependence of DIBL also increased steadily, suggesting that the drain voltage has a more pronounced influence on the threshold voltage in a high-thermal environment. These findings confirm that both SS and DIBL are very sensitive to temperature changes, and that the electrostatic performance of FinFET devices at the nanoscale is therefore highly sensitive.

Figure 4.4(b) illustrates the FinFETs V_T , SS, and DIBL behaviour at temperatures of 275, 300, 325, and 350 K and a L_g of 10 nm. The graph displays that these parameters decrease linearly with increasing temperature between 275 and 350 K. In particular, the SS is between 77.7 and 104 mV/dec, the DIBL is between 12.7 and 17.3 mV/V and the V_T is between 0.50 and 0.47 V. At 325 K, SS has the largest deviation of 77.77 mV/dec, the highest value of SS, indicating that SS depends on temperature, with a higher value of 85.34 mV/dec at higher temperatures. This suggests

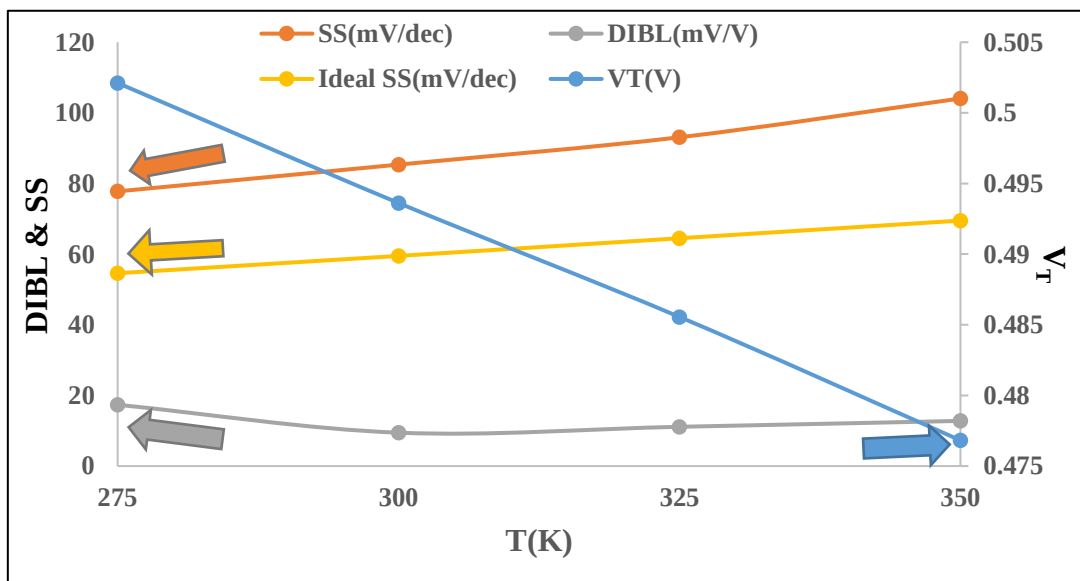
the SS distance is closest to the optimal value of 54.6 mV/dec. Likewise, DIBL exhibits an upward trend with increasing temperature.

The temperature profiles of key parameters, such as SS, V_T , and DIBL, for the FinFET at 275, 300, 325, and 350 K with $L_g = 20$ nm are provided in Figure 4.4(c). V_T or temperature displayed linear dependence and values decreased with temperature and at 275 K, V_T exhibited value of 0.53 V and at 350 K, the value was 0.49 V. This decrease in V_T caused by the decrease in the potential barrier in the channel at the source leads to a larger V_{DD} , and larger leakage current in the OFF state, since DIBL decreases V_T . At the minimum temperature of 275 K, SS was recorded at 69.5 mV/dec, increasing to 89.2 mV/dec at 350 K, which is the maximum deviation from the desired SS of 69.5 mV/dec. On the other hand, 350 K was close to the maximum SS of 54.6 mV/dec, and DIBL increased gradually with increasing temperature. Accordingly, this study determines the optimal dimensions of the transistor at $L_g = 7$ and 20 nm. As T_{ox} increased, SS gradually increased, DIBL grew slowly, and V_T had a slow growth curve.

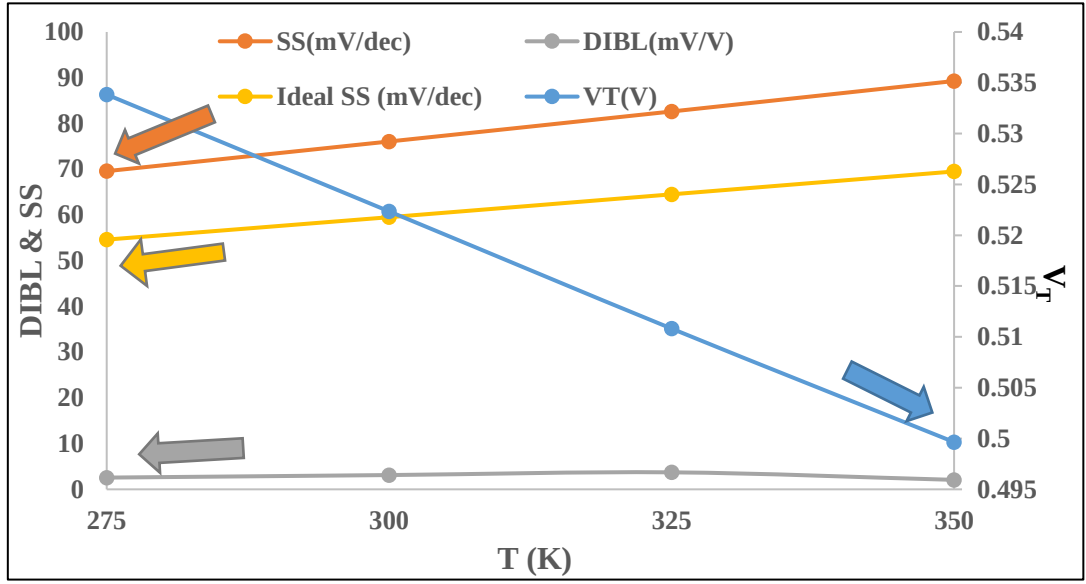
Figure 4.4(a-c) indicate that, with the increase in temperature, the SS also increases, whereas the V_T and the DIBL also decline. These trends indicate that an optimal L_g of 7-10 nm is associated with maximum device performance. Moreover, the derived results are comparable with the reported literature [120], which indicates that FinFET channel sizes in the 7-20 nm range are linearly related to their electrical properties. The most influential factor in current FinFETs has been temperature, primarily since carrier velocity increases in n-type FinFETs as the fin diameter decreases. It is also important to note that scaling the channel cross-section has a minimal effect on carrier velocities in n-type FinFETs. In strongly scaled MOSFETs, the saturation current between the drain and the channel is controlled by V_{inj} . This carrier injection velocity, unlike mobility, is a material property vital for calculating the drive current in ballistic transport [155].



(a)



(b)



(c)
Figure 4.4 V_T , SS, and DIBL at (a) $L_g = 7$ nm; (b) $L_g = 10$ nm; (c) $L_g = 20$ nm.

Figure 4.5 presents how V_T , DIBL, and SS change with L_g of FinFET channels between 7 and 20 nm at 300 K. With the length of the channel, V_T demonstrates a slow rise, especially at L_g longer than 10 nm. This may be explained by the damping of short-channel effects and by better gate control. This is consistent with earlier reported FinFET work, in which longer-channel devices indicated better threshold-voltage stability due to fewer electrostatic interactions between the drain and channel [137]. Conversely, DIBL demonstrates an exponential decline with increasing L_g , indicating stronger electrostatic integrity and successful elimination of short-channel effects, consistent with trends observed in more sophisticated tri-gate FinFET designs in the literature [156]. Moreover, the SS curves downwards with increasing channel length, approaching its near-ideal value of 54.6 mV/dec at $L_g = 20$ nm. Likewise, increases in SS with channel length across the 10-20 nm range have been observed in both experimental and simulated FinFET designs, demonstrating the usefulness of the multi-gate design in achieving near-ideal subthreshold performance [137-120]. On the whole, the behaviour of V_T , DIBL, and SS trends is roughly consistent with the scaling behaviour described in previous studies, providing physical consistency and validating the obtained simulation results.

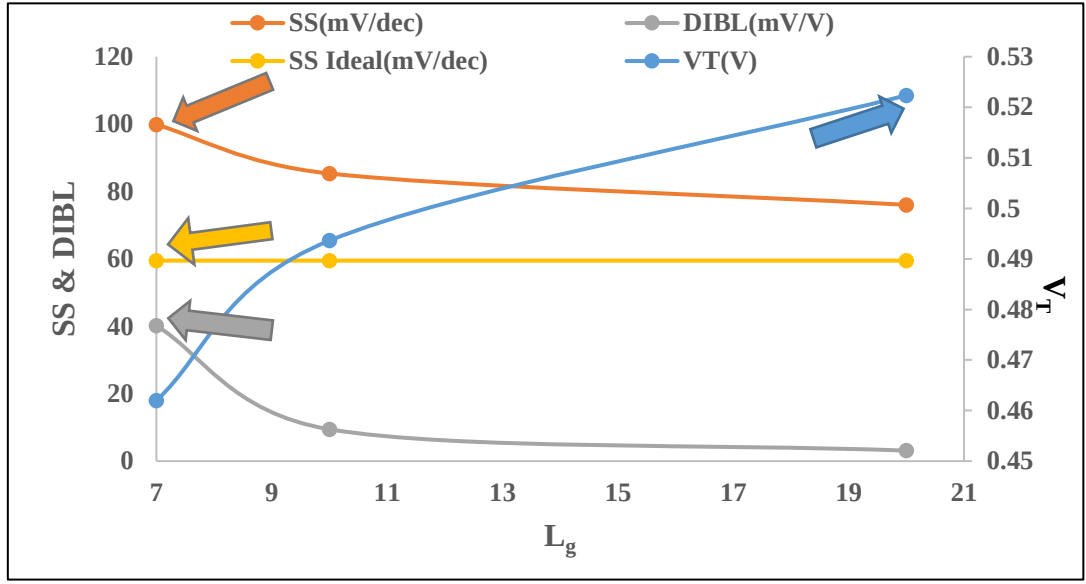


Figure 4.5 V_T , SS, and DIBL with L_g .

4.4 Effects of Temperature and Channel Length on Si-FinFET ($x = 0$) Characteristics

Figure 4.6-4.8 depict the dependence of ΔI on the temperature of the Si-FinFET devices with L_g of 10, 20, and 30 nm at various supply V_{DD} of 0 V to 1 V. The device with $L_g = 10$ nm has the greatest temperature sensitivity (see Figure 4.6), with ΔI peaking at $V_{DD} = 0.6$ V, and carrier transport modulation occurs at much shorter channel lengths. Figure 4.7 reveals that at $L_g = 20$ nm, the same trend is observed. Nevertheless, the total magnitude of ΔI is smaller than at the 10 nm device, as evidenced by higher electrostatic stability and lower temperature-induced variation. However, Figure 4.8 presents that the FinFET with $L_g = 30$ nm has the lowest ΔI values over the temperature range studied, indicating greater thermal stability yet lower sensitivity. Across all channel lengths, ΔI generally decreases with temperature, with small exceptions at certain bias conditions, suggesting that thermal behaviour is dominated by mobility degradation. It is important to note that Figure 4.6, 4.7, and 4.8 all demonstrate that $V_{DD} = 0.6$ V offers an optimal operating point with which the device can perform reliably as long as the temperature does not exceed 325-350 K. This comparative study points out to the trade-off between sensitivity and thermal stability as the channel length is extended, where it has been established that shorter channel devices are more sensitive, and longer channels are more thermally reliable.

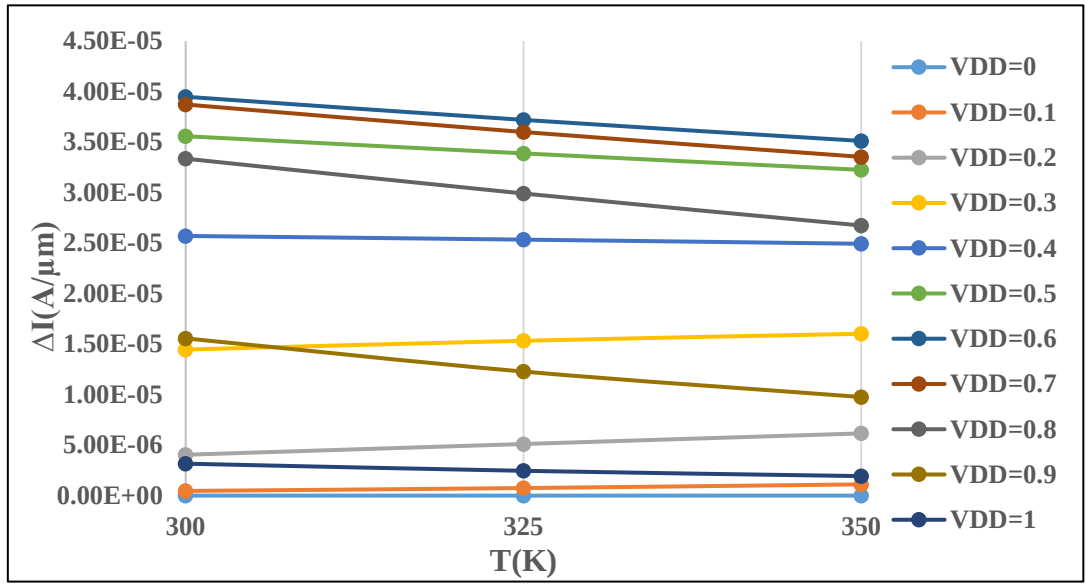


Figure 4.6 ΔI -T FINFET characteristics ($L_g = 10$ nm).

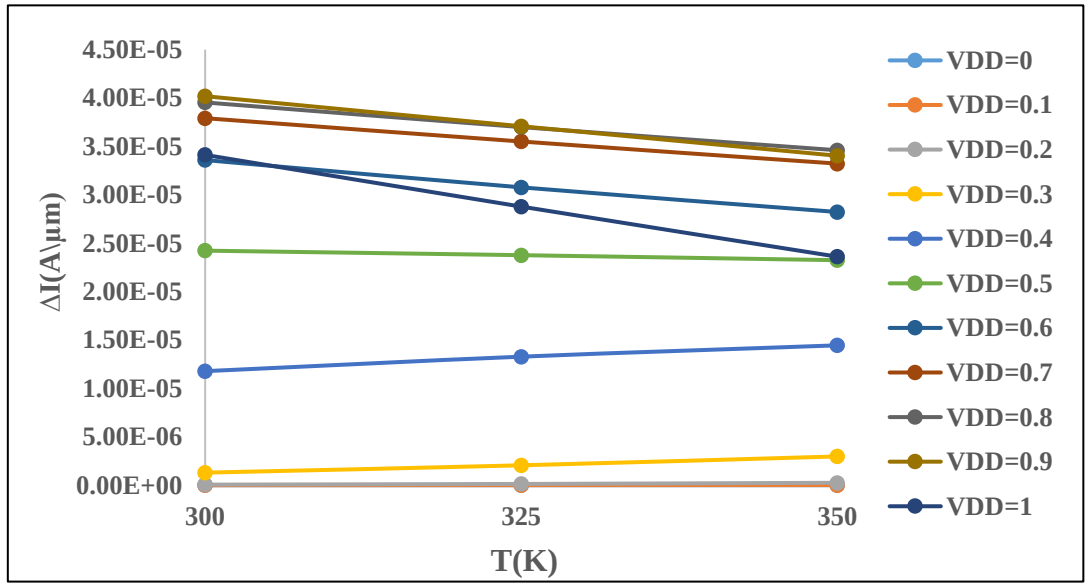


Figure 4.7 ΔI -T FinFET characteristics ($L_g = 20$ nm).

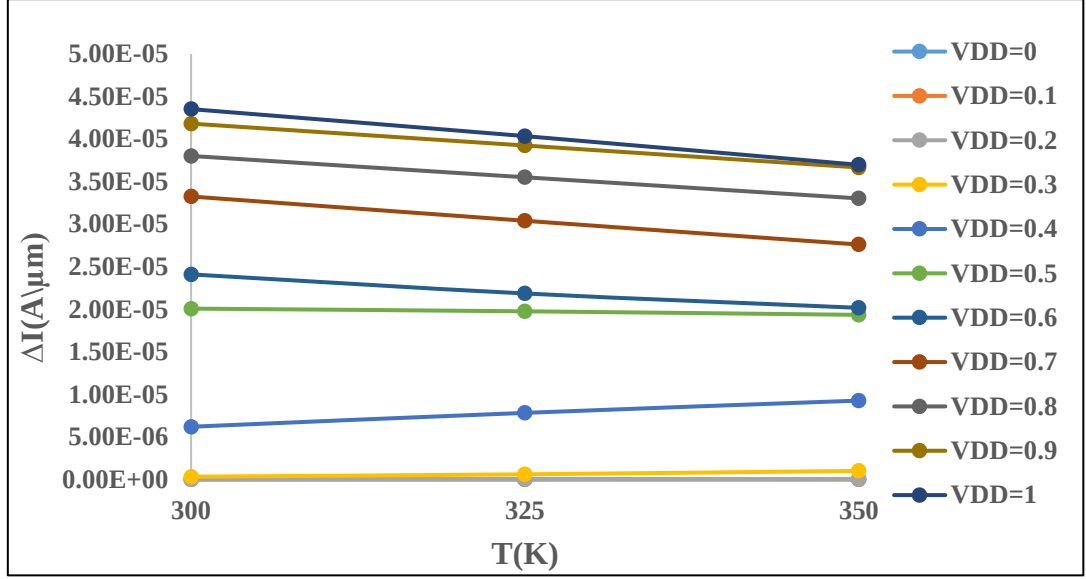


Figure 4.8 ΔI -T FinFET characteristics ($L_g = 30$ nm).

The variations in ΔI with decreasing V_{DD} at $T = 275, 300, 325$, and 350 K, and $L_g = 10, 20$, and 30 nm are presented in Figure 4.9 to 4.11. $V_{DD} = 0.1$ V ($L_g = 10$ nm), $V_{DD} = 0.3$ V ($L_g = 20$ nm), and $V_{DD} = 0.4$ V ($L_g = 30$ nm) were found to have the highest sensitivity (max ΔI). So, Figure 4.9–4.11 demonstrate that ΔI increases with increasing temperature and V_{DD} , reaching a maximum at 0.4 V for $L_g = 30$ nm and $W_g = 10$ nm.

To provide a clearer understanding of the device performance, the temperature sensitivity was assessed by examining the slope of the ΔI -T characteristics for different gate lengths. It was revealed that, with shorter gate lengths, especially at $L_g = 10$ nm, the response to temperature changes was significantly stronger and hence more sensitive. The ΔI -T curves were steeper as the gate length increased, indicating reduced thermal responsiveness. The latter observation highlights the significant role of channel length in the thermal sensitivity of FinFET devices. It justifies the use of ultra-scaled geometries to enhance the performance of FinFET devices in temperature-sensitive electronic functions.

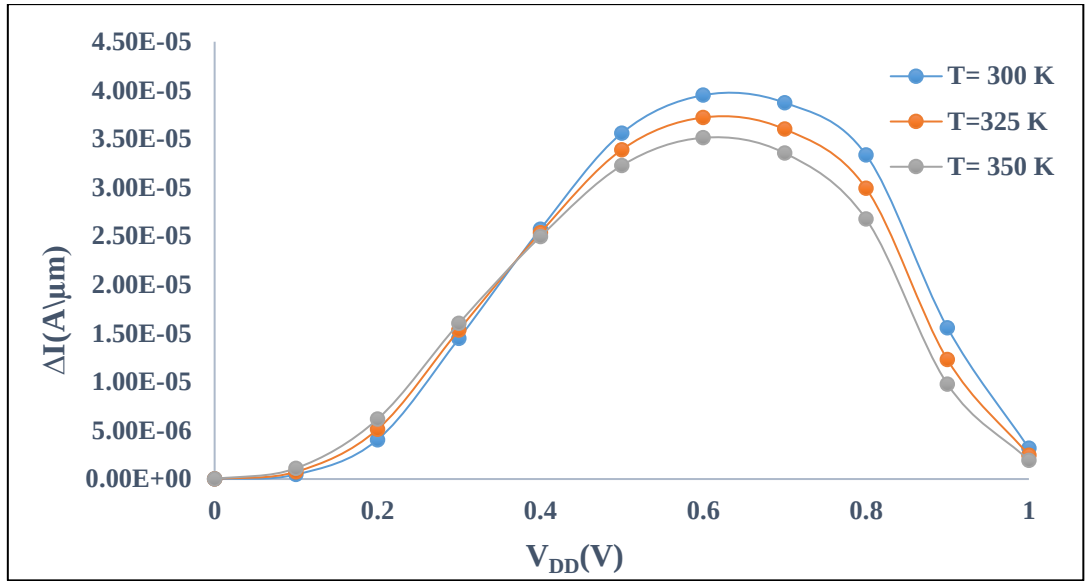


Figure 4.9 Characteristics of ΔI with V_{DD} at ($L_g = 10$ nm).

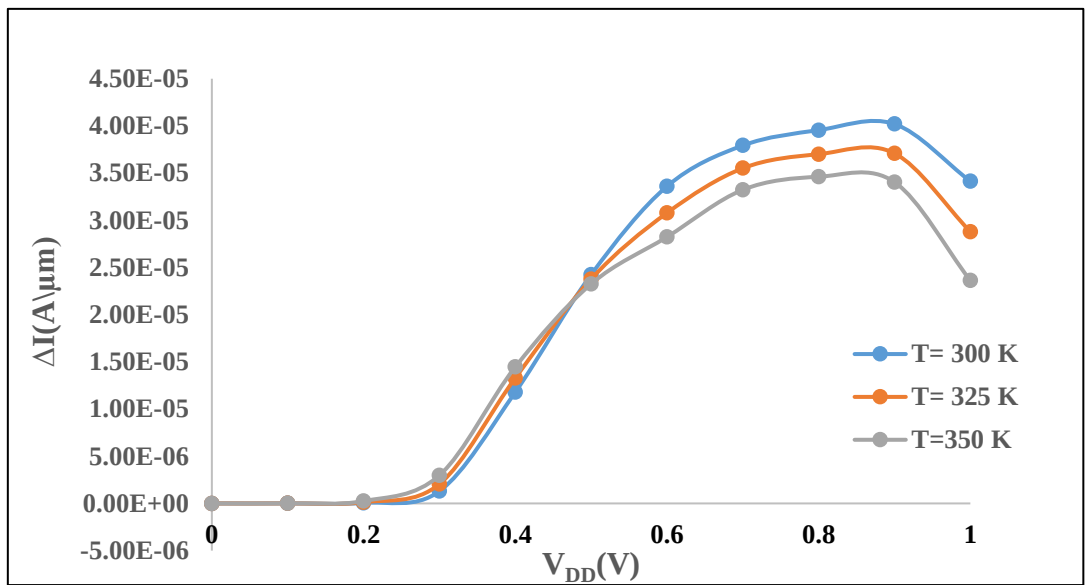


Figure 4.10 Characteristics of ΔI with V_{DD} at ($L_g = 20$ nm).

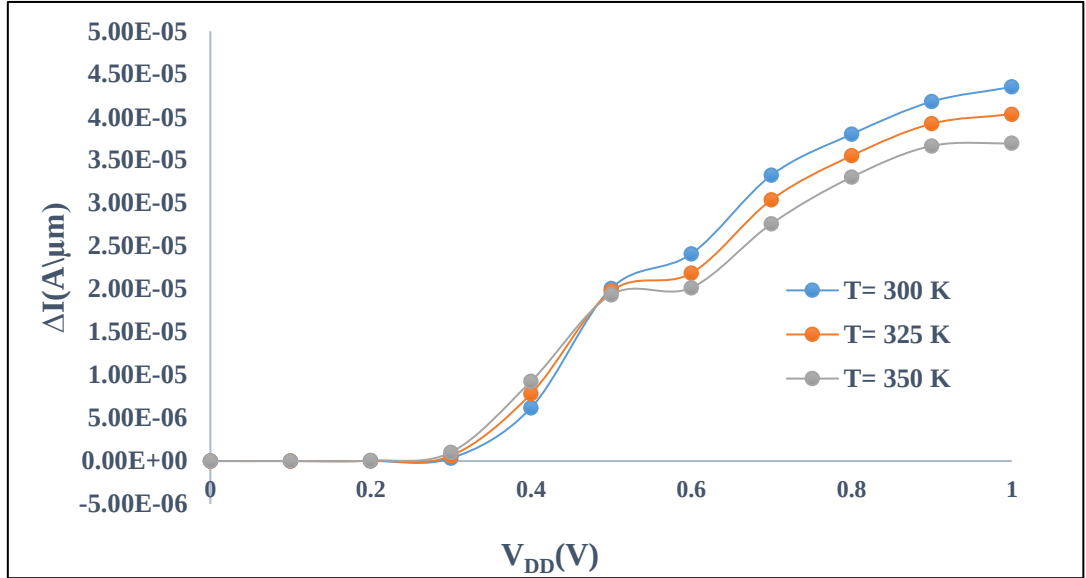


Figure 4.11 Characteristics of ΔI with V_{DD} at ($L_g = 30$ nm).

Figure 4.12 illustrates the dependence of ΔI and L_g of Si-FinFETs. The higher the L_g , the lower the ΔI , indicating a negative correlation between the two. This implies better electrical control and reduced short-channel effects as the gate length increases. The graph indicates that ΔI begins to decline sharply when L_g exceeds 20 nm, indicating that the optimal gate length for achieving optimal current performance lies between 20 and 30 nm. Beyond this range, further increases in gate length result in diminishing gains in ΔI .

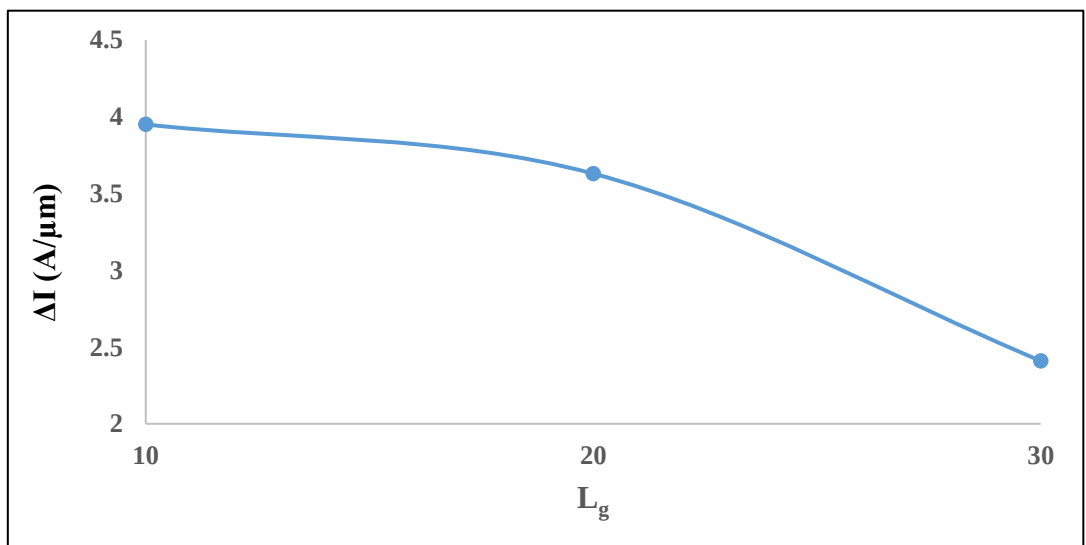


Figure 4.12 Characteristics of ΔI with L_g .

Figure 4.13 illustrates the temperature characteristics of DIBL, V_T , and SS in the FinFET, which were measured at $T = 275, 300, 325$, and 350 K with $L_g = 10$ nm. As the temperature increased, V_T declined linearly; for example, at 275 K, it was 0.28 V, and at 350 K, it was 0.22 V. At the lowest temperature, 275 K, SS began at 120.3 mV/dec. It then climbed until it reached 161.6 mV/dec (the value that deviates the furthest from the ideal SS, which is 69.5 mV/dec) at 350 K (the value that is closest to the ideal SS, which is 54.6 mV/dec). Finally, DIBL increased along with the temperature. The value of SS depends on the surrounding temperature and increases until it reaches 133.6 mV/dec (the farthest from the ideal SS at 54.6 mV/dec).

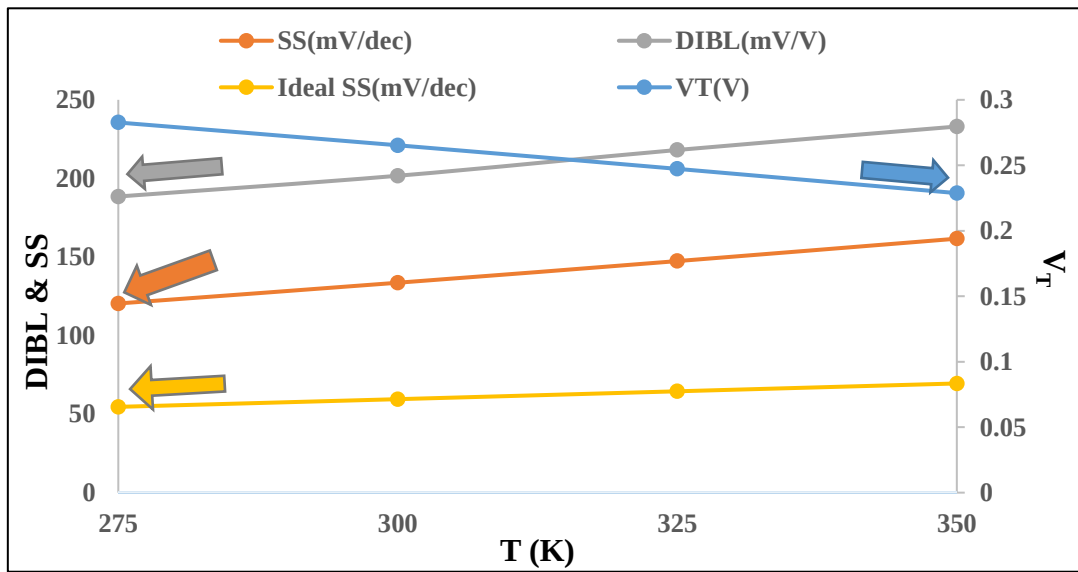


Figure 4.13 V_T , SS, and DIBL at $L_g = 10$ nm.

Figure 4.14 illustrates the FinFETs, V_T , DIBL, and SS characteristics at $275, 300, 325$, and 350 K with $L_g = 20$ nm. The figure further demonstrates a linear relationship over this temperature range, with V_T values of 0.46 V and 0.41 V, SS values of 89.67 mV/dec and 115.81 mV/dec, and DIBL values of 34.71 mV/V and 48.45 mV/V, respectively. The subthreshold slope at 275 K, measured at 89.67 mV/dec, deviates most from the ideal value of 54.6 mV/dec. At the lowest temperature of 275 K, the SS was farthest from ideal, whereas at 350 K, the SS improved to 69.5 mV/dec before increasing again to 115.81 mV/dec. Meanwhile, DIBL increased progressively with increasing temperature. FinFET has been suggested as a formidable rival to classical CMOS due to its proven scalability and potential performance advantage

(albeit at the cost of increasing the complexity of the current planar process during fabrication).

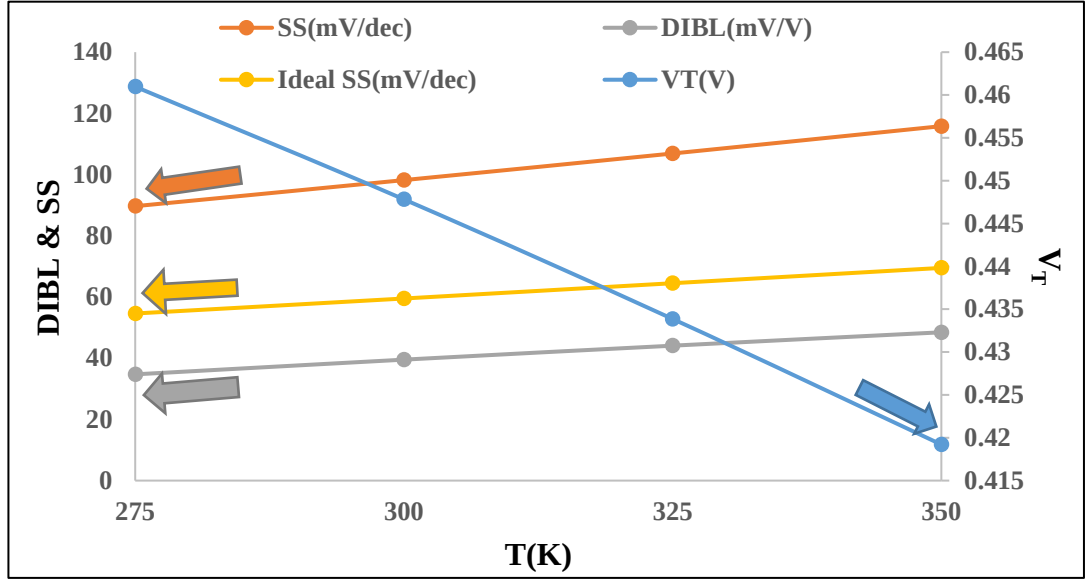


Figure 4.14 V_T , SS, and DIBL at $L_g = 20$ nm.

Figure 4.15 illustrates the relationships between variations in V_T , SS, and DIBL, and their impact on FinFET characteristics as temperature changes from 275 K to 350 K, with a L_g of 30 nm. The V_T decreased slowly with increasing temperature. $V_T = 0.48$ and 0.46 V, $SS = 74.22$ and 99.93 mV/dec, and $DIBL = 8.29$ and 13.37 mV/V, respectively, are the values obtained between 275 K and 350 K. The figure depicts that the SS value, which deviates the most from the ideal value of 54.6 mV/dec at 275 K, is 74.22 mV/dec. As the temperature rises to 350 K, this value increases further to 99.93 mV/dec. Additionally, DIBL increased with increasing temperature.

The major influence of temperature on the current in FinFETs is most likely due to the increased carrier velocity for n-type FinFETs as the fin dimensions decrease. The channel cross-section scaling has no discernible effect on the carrier velocities of n-type FinFETs. Furthermore, the drain saturation current in substantially downscaled MOSFETs is determined by the optimum V_{inj} from the point of origin to the channel. In the ballistic transport regime, the driving current is primarily governed by the carrier injection velocity, an intrinsic material property rather than by conventional mobility-based conduction mode [157].

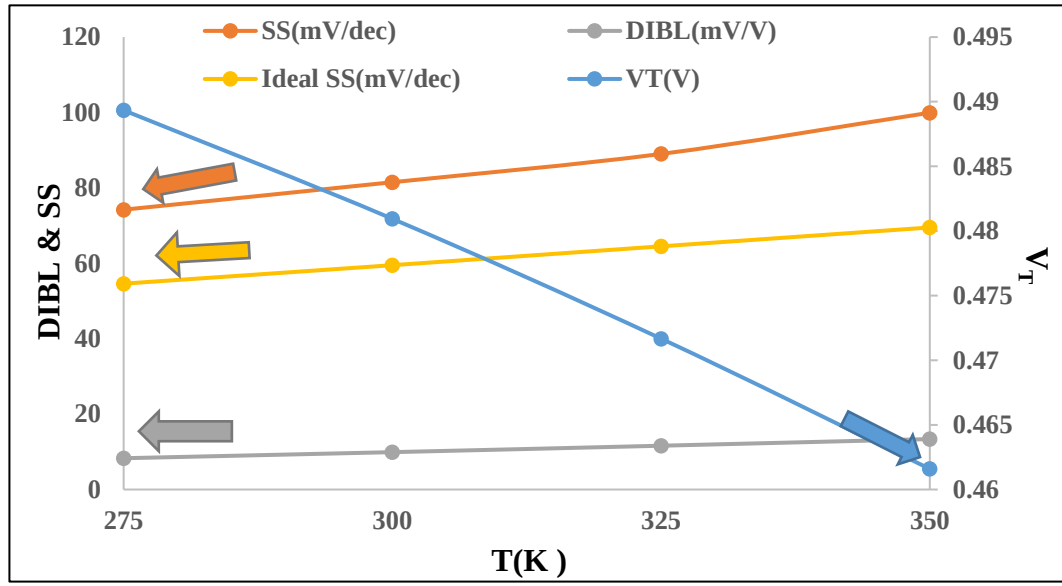


Figure 4.15 V_T , SS, and DIBL at $L_g = 30$ nm.

The characteristics of V_T , SS, and DIBL are displayed in Figure 4.16, which illustrates how these parameters change with increasing FinFET channel length at 300 K. The channel length increases in steps of 10 nm, from 10 to 30 nm. As the channel length increases beyond 10 nm, the SS decreases significantly, reaching a value of (81.5 mV/dec) close to the ideal value of (54.6 mV/dec) at L_g of 30 nm. In contrast, the V_T increases with channel length, reaching 0.48 V and nearly saturating as L_g increases. Regarding DIBL (201.6 mV/V), it demonstrates a significant increase at 10 nm before decreasing slightly with further increases in L_g (DIBL = 9.9 mV/V at $L_g = 30$ nm). These findings indicate that the optimum channel length of FinFETs is between 20 and 30 nm under the test conditions. FinFETs electrical properties at frequencies between 10 and 30 nm are directly proportional to dimension as illustrated in Figure 4.16. This observation aligns with earlier research [158].

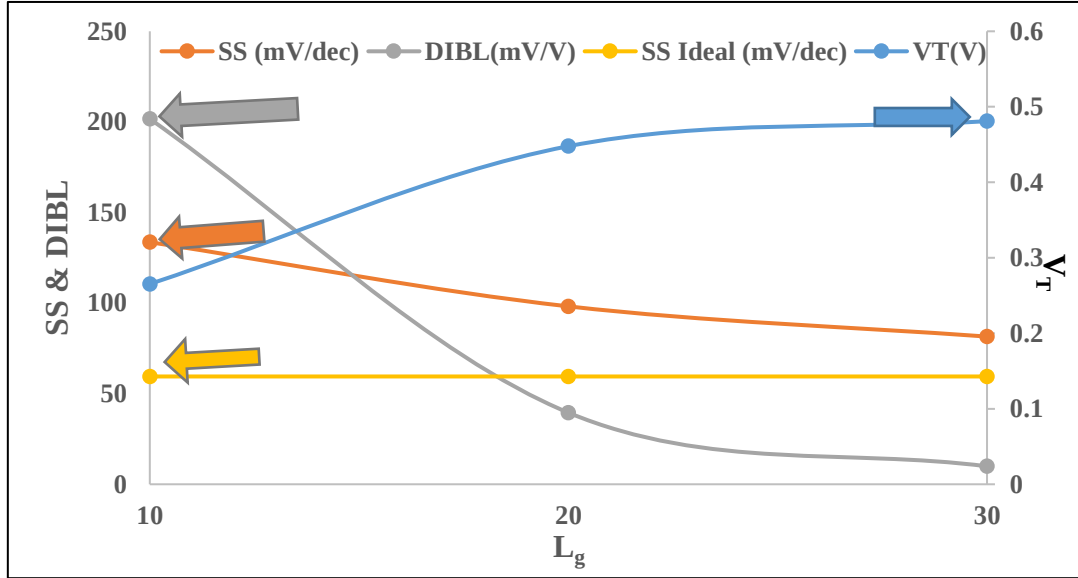
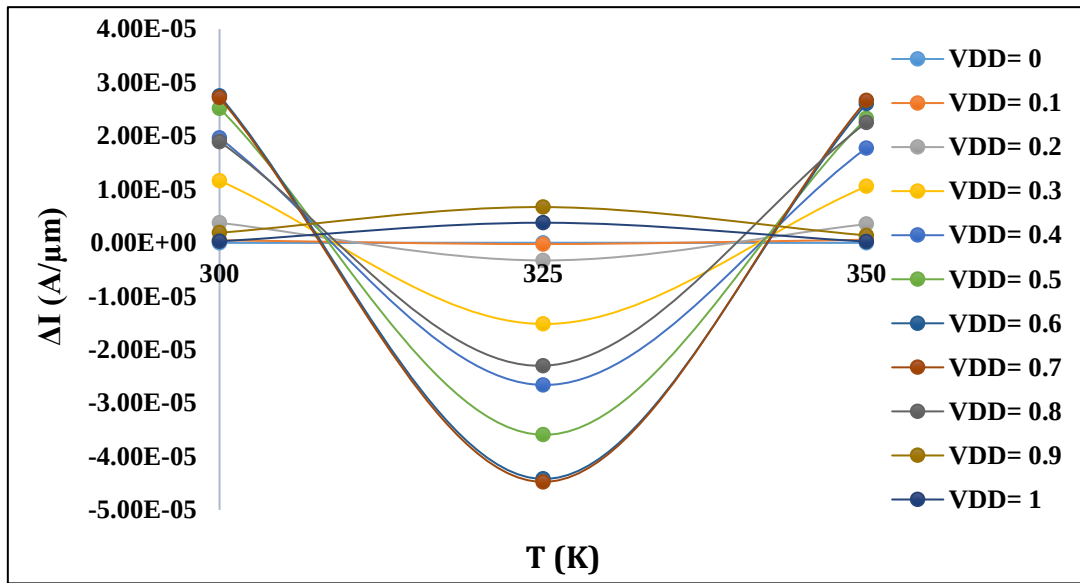


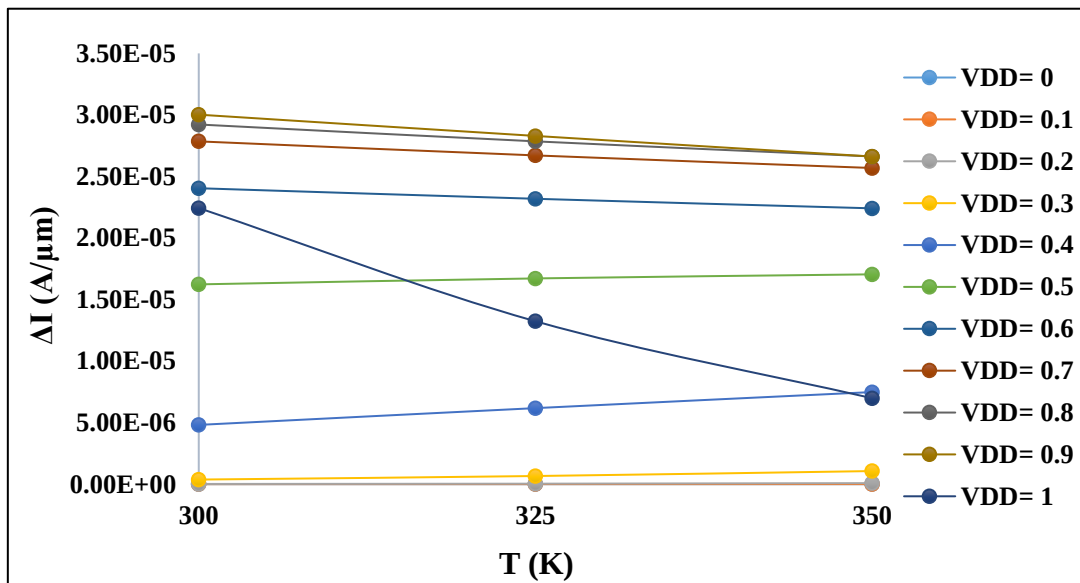
Figure 4.16 V_T , SS, and DIBL with L_g .

4.5 Effects of Temperature and Channel Length on Ge-FinFET ($x = 1$) Characteristics

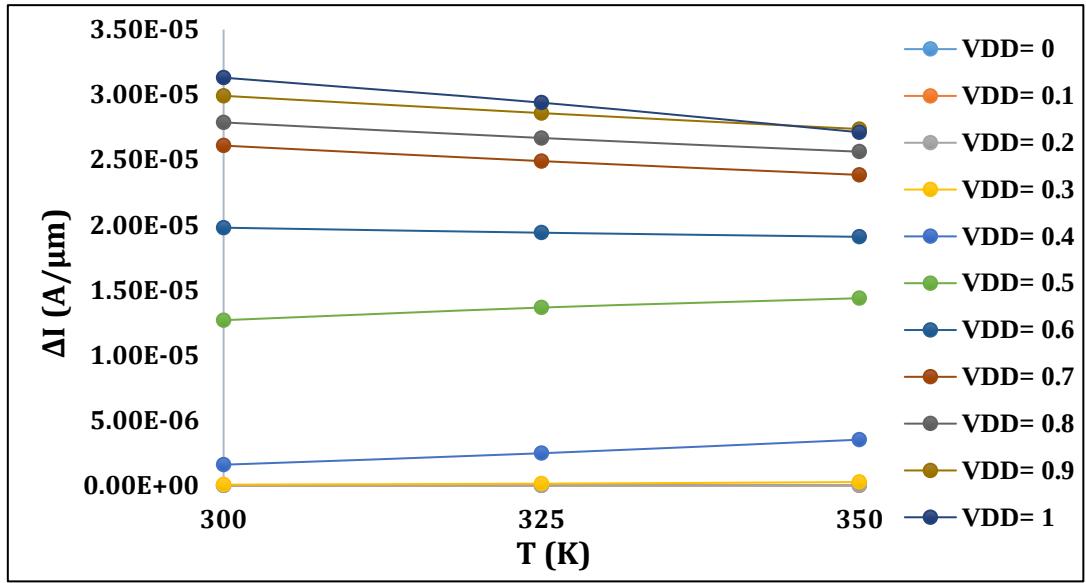
Figure 4.17(a–c) depict how current (I) changes with L_g of 10, 20, and 30 nm with a voltage increment of 0.1 V. In the V_{DD} range of 0 to 1 V, the findings indicate that ΔI increases with increasing temperature in some cases. This effect is more pronounced in conditions where the L_g is greater than 10 nm (particularly at 20 and 30 nm), and the lowest temperatures are the most sensitive, with the largest ΔI . Figure 4.17(a) and (b), respectively, illustrate the optimal temperature sensitivity coefficients at $V_{DD} = 0.9$ V, and L_g values of 10 and 20 nm, respectively. Meanwhile, Figure 4.17(c) illustrates the maximum sensitivity at $L_g = 30$ nm at $V_{DD} = 1$ V. These results indicate that, as indicated in Figure 4.17(a) to (c), the transistor works best when V_{DD} is 1 V, which is stable between 325 and 350 K.



(a)



(b)



(c)

Figure 4.17 ΔI -T characteristics of FinFET at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.18(a–c) present the changes in ΔI with V_{DD} in the presence of temperatures of 275, 300, 325, and 350 K and at L_g of 10, 20, and 30 nm. The figures illustrate the behaviour of ΔI at various temperatures and gate lengths. In this context, all subfigures exhibit different gate lengths.

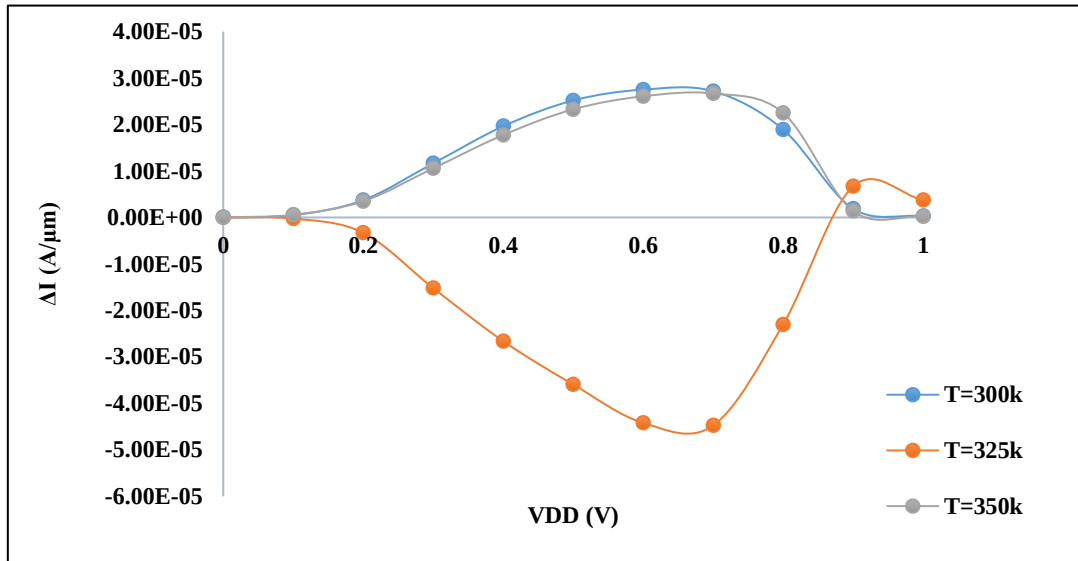
Figure 4.18(a) indicates the relation at a L_g of 10 nm. The peak ΔI occurs at a V_{DD} of 0.9 V, and at this point, the current response is most sensitive. Sensitivity increases with temperature, indicating that higher temperatures improve the device's functionality.

The maximum sensitivity is also 0.9 V at $L_g = 20$ nm, as depicted in Figure 4.18(b). The trend also indicates that higher temperatures are associated with higher ΔI and thus better device performance.

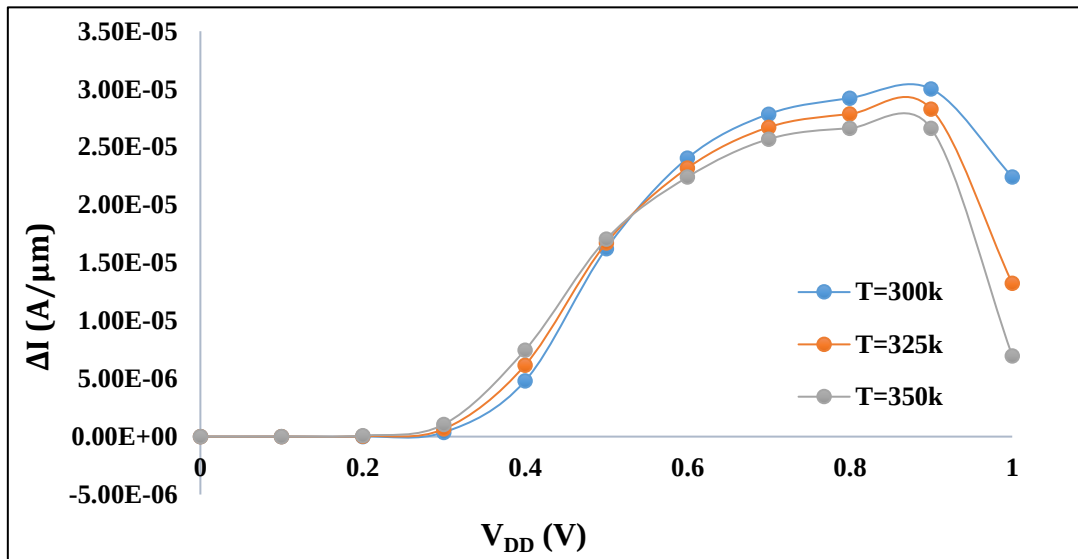
The data of 30 nm are presented in Figure 4.18(c). In this case, the highest ΔI is attained at $V_{DD} = 1$ V, which is the optimum operating voltage for this L_g . As displayed in the figures above, ΔI exhibits an upward trend with increasing temperature, indicating that the sensitivity increases with higher temperatures.

The values of the three figures reveal that ΔI tends to increase with increasing temperature and V_{DD} . In particular, results indicate optimal operating voltages of 1 V at $L_g = 30$ nm, 0.9 V at $L_g = 10$ nm, and 20 nm. According to these results, the device's performance is maximized at these voltage values for each L_g , and temperature also

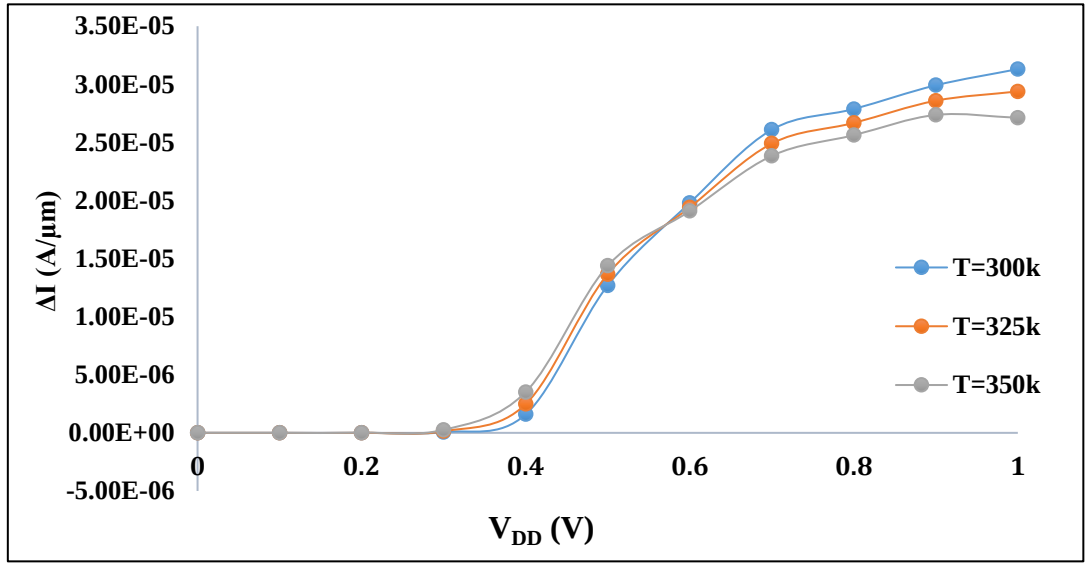
plays an important role in increasing ΔI , which is critical for device operation, especially when power demand is low.



(a)



(b)



(c)

Figure 4.18 Characteristics of ΔI with V_{DD} at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

The relationship between ΔI and L_g is portrayed in Figure 4.19, where an improvement in L_g results in a progressive increase in ΔI , indicating that the transistor has improved electrostatic integrity. Extended channels increase the channel potential under gate influence and reduce short-channel effects, as depicted in Figure 4.19, thereby enabling more reliable FinFET operation under varying biasing conditions. It is the trend that illustrates the benefit of using larger L_g values to maintain device reliability and reduce the impact of nanoscale performance degradation.

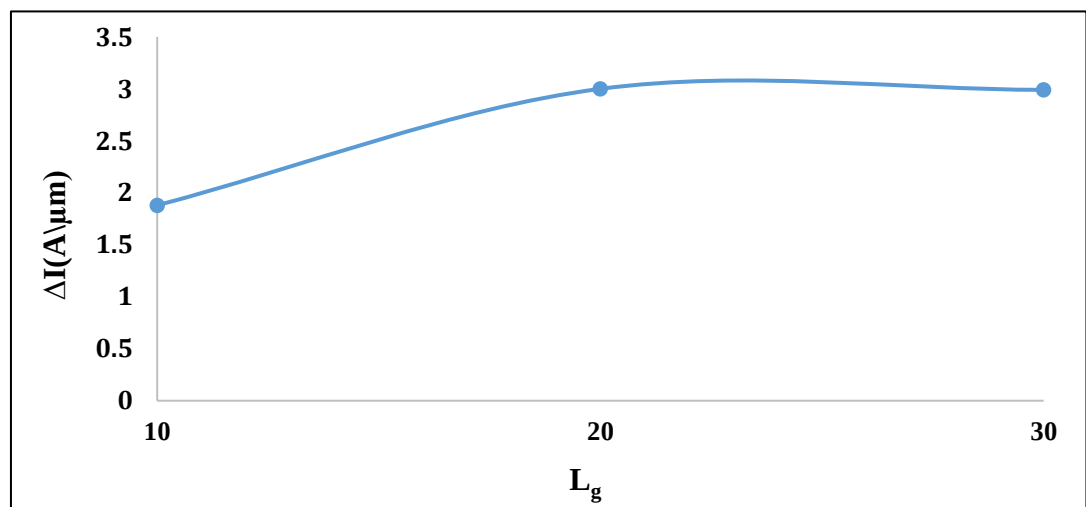


Figure 4.19 Characteristics of ΔI with L_g .

Figure 4.20(a) presents temperature curves of significant values of the FinFET, including SS, V_T , and DIBL at temperatures of 275, 300, 325, and 350 K with $L_g = 10$ nm and $W_g = 10$ nm. The temperature decreased the V_T , which decreased to 0.17 V at 350 K and 0.19 V at 275 K. This decrease in V_T is explained by a reduced channel potential barrier at the source. Consequently, DIBL increases, raising V_{DD} and the leakage current in the OFF state. The largest change in SS was observed at 275 K, with a reading of 217.49 mV/dec, which is very different from the ideal value of 54.6 mV/dec. On the other hand, at 350 K, the SS value was 187.23 mV/dec, gradually approaching the ideal value of 69.5 mV/dec. As the temperature increased, DIBL rose gradually from 260.94 to 270.8 mV/V between 275 K and 325 K, then decreased to 230.36 mV/V at 350 K.

The behaviours of V_T , SS, and DIBL for the FinFET at temperatures of 275, 300, 325, and 350 K, with L_g of 20 nm and $W_g = 10$ nm, are illustrated in Figure 4.20(b). As the temperature rises, forming a gradient of 275-350 K, it has been observed that V_T is lower at elevated temperatures, i.e., it gradually decreases in both SS and DIBL. The rate is not constant in both cases.

Specifically, the ranges of SS, DIBL, and V_T are 95.87-123.71 mV/dec, 38.57-41.75 mV/V, and 0.49-0.46 V, respectively. The maximum deviation between the ideal SS value of 54.6 mV/dec and the actual values occurs at 275 K, where SS is above 95.87 mV/dec. This was deviated by the temperature-sensitive nature of SS, which climbs to 123.71 mV/dec as the temperature rises (350 K). Similarly, DIBL exhibits an oscillatory pattern as temperature increases. Figure 4.20(c) further demonstrates the relationship between the changes in V_T , DIBL, and SS with temperature with $L_g = 30$ nm and $W_g = 10$ nm which are then associated with a decrease in V_T of 0.5 to 0.51 V, a rise in DIBL of 10.62 to 15.53 mV/V and a rise in SS of 76.11 to 100.75 mV/dec over the 275-350 K temperature. The ideal value of 54.6 mV/dec is not far from 275 K, with the SS value at 76.11 mV/dec. To determine the optimal L_g and temperature, the device's electrical characteristics are estimated. SS rises further at 350 K to 100.75 mV/dec, which contrasts with the fact that DIBL also increases with temperature, indicating a correlation between them.

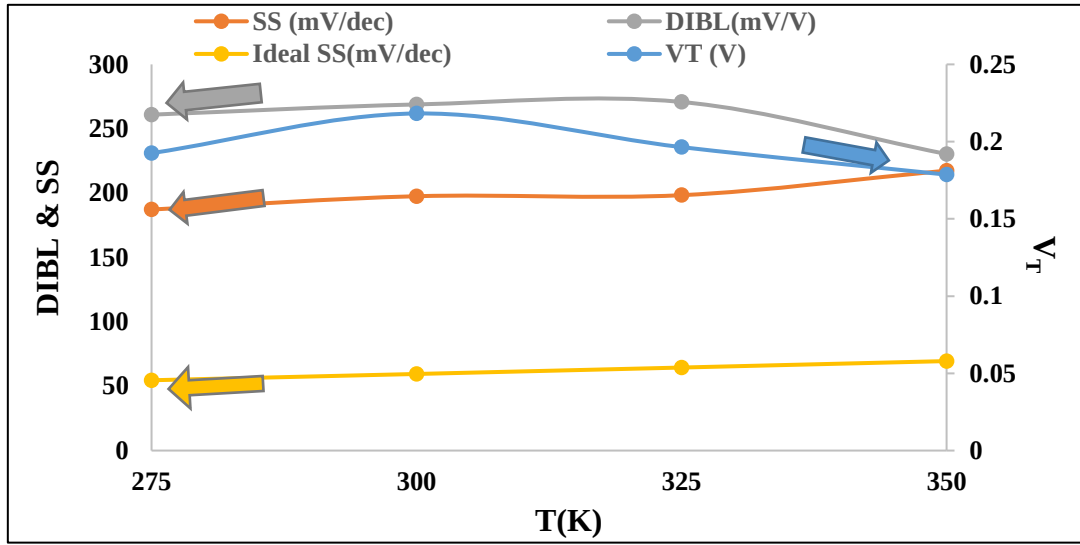
Figure 4.20(a-c) present temperature variations of the V_T , SS, and DIBL of FinFET devices having L_g of 10, 20, and 30 nm, respectively. The measured reduction in V_T at high temperature (across all channel lengths) is consistent with FinFET research, in which thermal activation reduces the source-channel potential barrier and

increases carrier injection [137-159]. Bandgap narrowing and larger intrinsic carrier concentration have been strongly suggested as the cause of similar temperature-dependent V_T roll-off in reduced-size MOS-based devices.

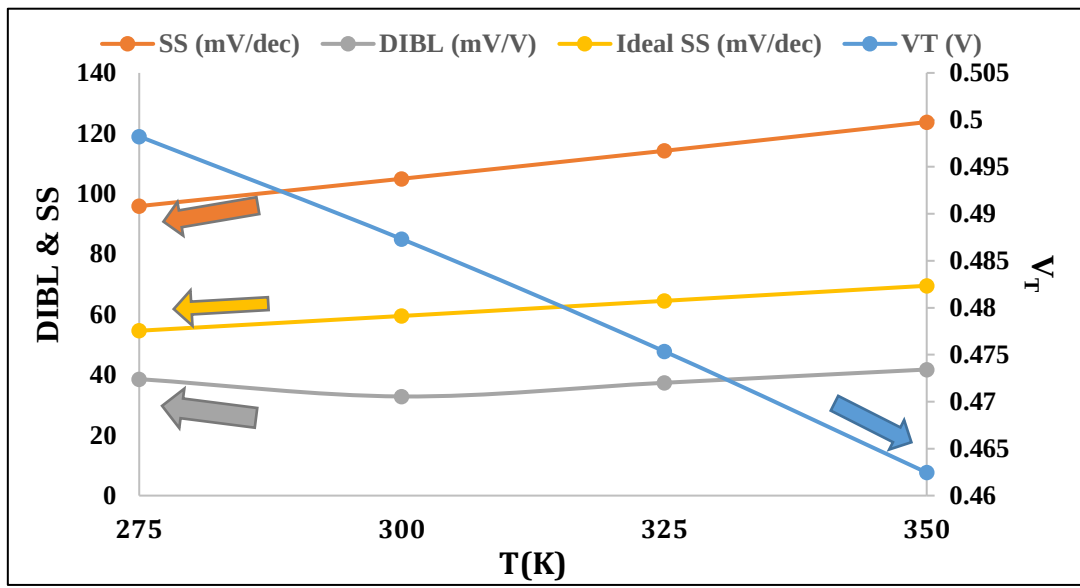
At the shortest channel length ($L_g = 10$ nm), the rapid increase in DIBL and the significantly reduced SS value demonstrate the dominance of short-channel effects in aggressively scaled dimensions. This trend is consistent with previous experimental and solution-based simulation studies, which demonstrate that sub-10 nm FinFETs exhibit a high level of electrostatic interaction between the drain and the channel, resulting in high leakage currents and PCs [36].

In comparison, devices with longer channel lengths ($L_g = 20$ and 30 nm) exhibit significantly enhanced electrostatic integrity, as indicated by reduced DIBL and SS values closer to the ideal limit. These are consistent with the reported literature, which demonstrates that channel lengths exceeding 15-20 nm offer a satisfactory trade-off between electrostatic control and thermal stability in multi-gate FinFET structures [160]. Remarkably, the findings described below also indicate the joint impact of temperature and L_g on subthreshold behaviour, finding that even longer channels can still induce some appreciable long-short-channel interaction. Higher temperatures are reported to cause appreciable degradation in SS and DIBL.

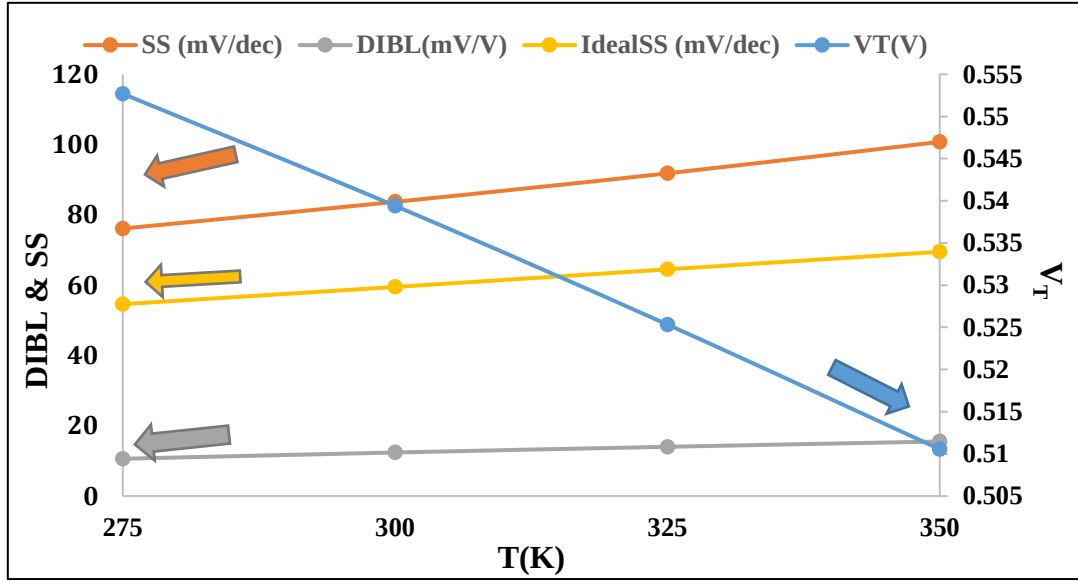
The similarity of the trends extracted to the earlier published literature indicates, overall, the physical validity of the simulation results. Furthermore, systematic comparisons and contrasts across different channel lengths and temperatures provide further insight into the combined influence of thermal effects and geometrical scaling, thus expanding the existing literature on FinFET performance analysis.



(a)



(b)



(c)

Figure 4.20 V_T , SS, and DIBL at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.21 demonstrates that in the W_g of 10 nm, the variation of L_g of FinFET in the 10-30 nm range gives a DIBL of 0.184 V/m and SS of 0.134 mA/m. When L_g is raised from 10 to 20 nm, DIBL exhibits a clear attenuation from 256.8 to 32.8 mV/V. This indicates that short-channel effects are considerably minimised due to increased electrostatic gate control. The decrease in DIBL beyond 20 nm is slighter, and at $L_g = 30$ nm to 30 nm, the DIBL has decreased to 12.4 mV/V, consistent with the established FinFET behaviour of DIBL saturation at higher channel lengths.

The given trend compares well with experimental and simulation results reported in the literature, which depict that DIBL values below 50 mV/V are generally observed at FinFET channel lengths above 20 nm [161]. Equally, the SS values extracted also monotonically decrease with increasing L_g and approach 83.7 mV/dec at 30 nm. Similar SS values ranging from 70 to 90 mV/dec at the nanoscale have been commonly reported in IEEE-indexed articles [162] for [Fin] FinFETs with L_g values of 20 nm or more.

Conversely, V_T demonstrates a gradual increase with L_g and is likely to saturate beyond 20 nm, indicating reduced drain-field penetration and enhanced channel potential stability. This is consistent with prior publications, which reflect an increase and subsequent saturation of the threshold voltage as short-channel effects are mitigated in longer FinFET channels [5]. All in all, the trends of reduced DIBL and SS, as well

as the stabilization of V_T , indicate that the most appropriate operating regime for the proposed FinFET structure under current-state-of-the-art conditions is 20-30 nm. This finding is fully consistent with the existing state-of-the-art technologies supported by FinFETs.

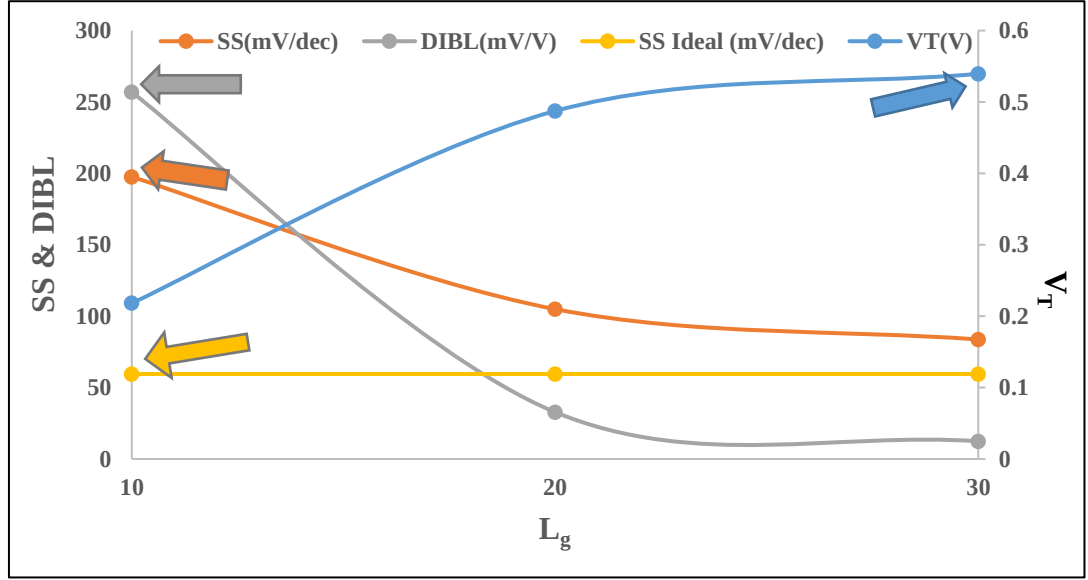


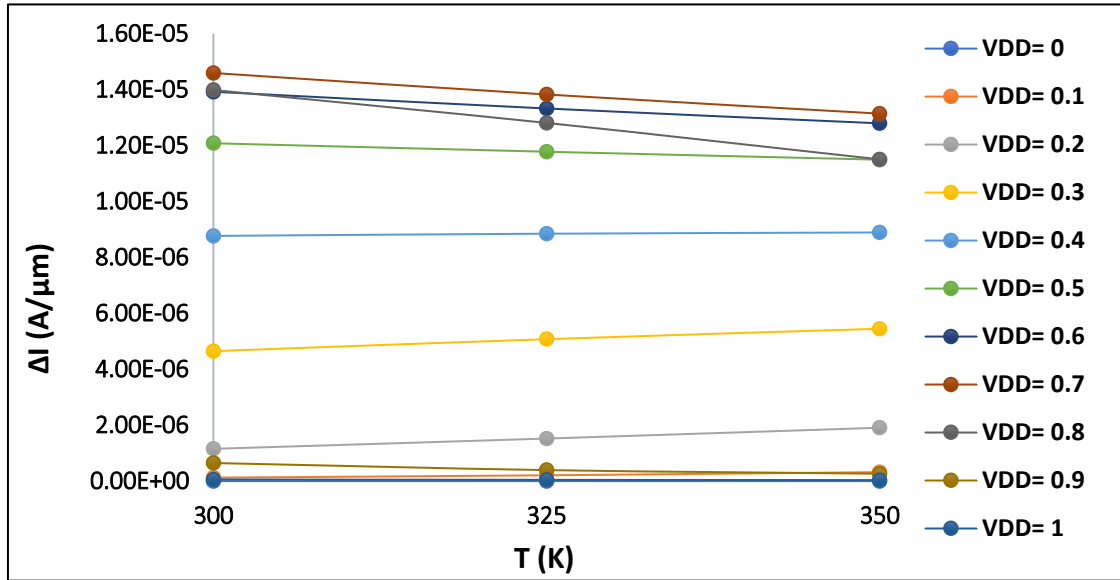
Figure 4.21 V_T , SS, and DIBL with L_g .

4.6 Effects of Temperature and Channel Length on $\text{Si}_{1-x}\text{Ge}_x$ -FinFET Characteristics

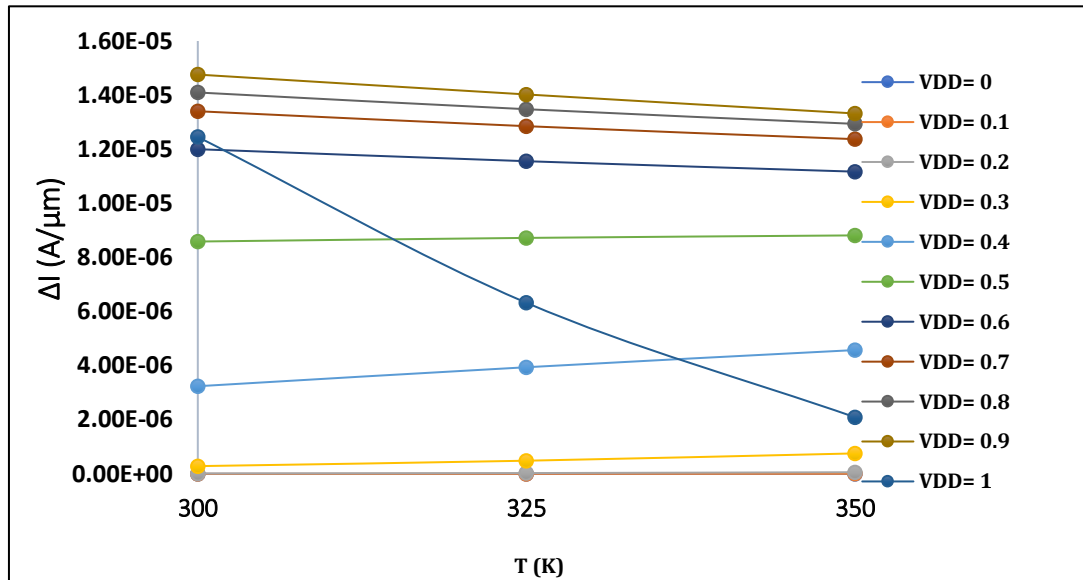
4.6.1 Effects of Temperature and Channel Length on $\text{Si}_{0.75}\text{Ge}_{0.25}$ -FinFET ($x = 0.25$) Characteristics

Figure 4.22(a–c) illustrate the variation in current as a result of L_g of 10, 20, and 30 nm, with voltage increments of 0.1 V. Within the V_{DD} range of 0 to 1 V, the results demonstrate that ΔI gradually decreases with a rare and slight increase in some cases with rising temperature. Instead, while lower temperatures exhibit the greatest sensitivity (max ΔI), the behaviour of ΔI with increasing temperature varies non-linearly across different values of V_{DD} . For L_g values of 10 and 20 nm, Figure 4.22(a–b) depict the temperature sensitivity coefficients at $V_{DD} = 0.7$ and 0.9 V, respectively. Figure 4.22(c) presents that the greatest sensitivity is $L_g = 30$ nm in the case of $V_{DD} = 1$ V. Such results indicate that the transistor is most favorable under working loads of V_{DD}

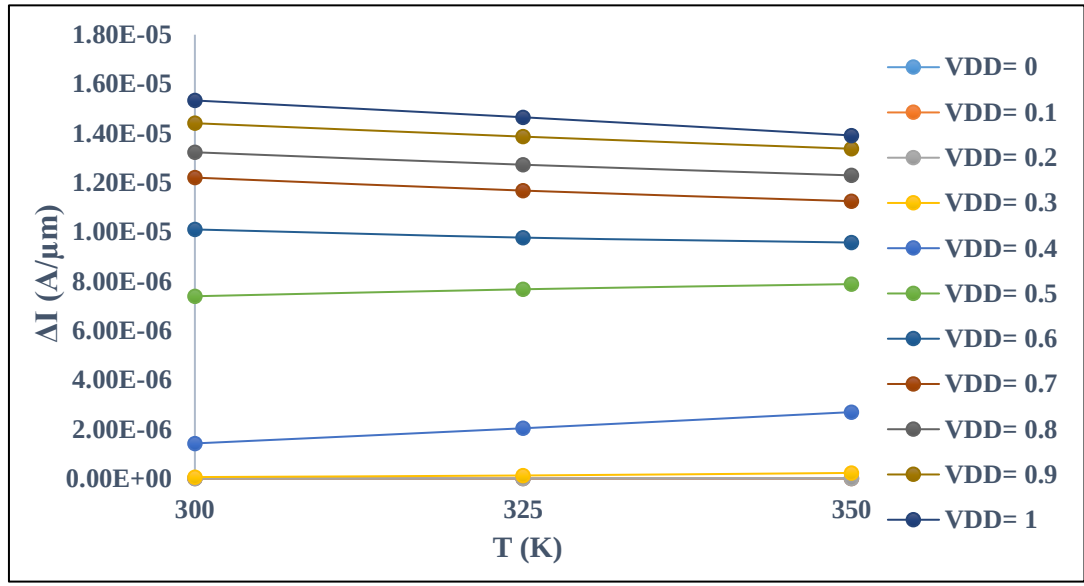
$= 1$ V when ΔI indicates the greatest sensitivity of the transistor at varying temperatures. This tendency indicates that V_{DD} and L_g significantly affect the thermal and electrical performance of FinFETs. Emphasis should be placed on maximizing these parameters to ensure device stability across different temperature conditions, as illustrated in Figure 4.22(a-c).



(a)



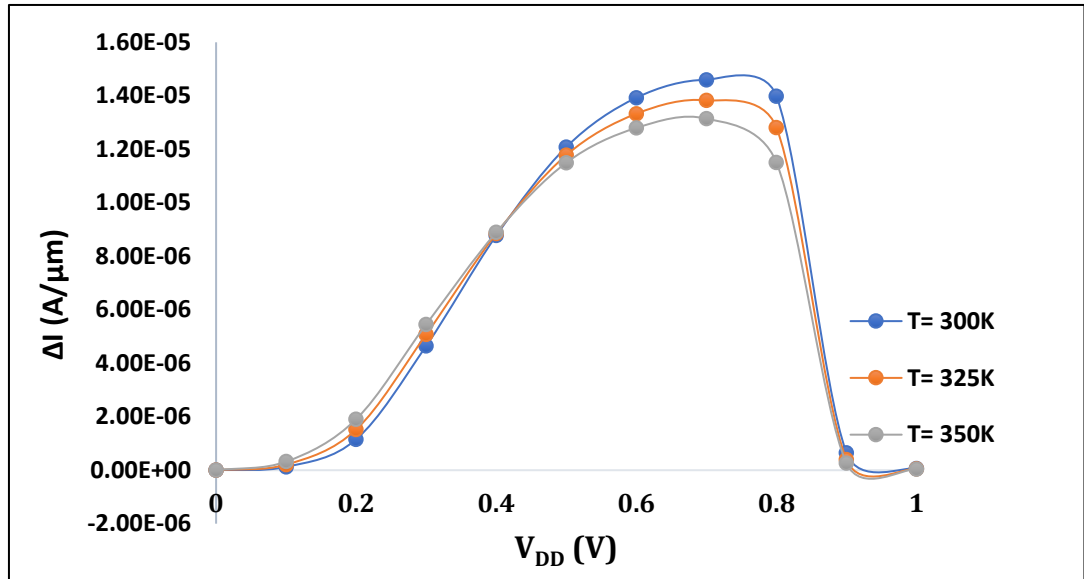
(b)



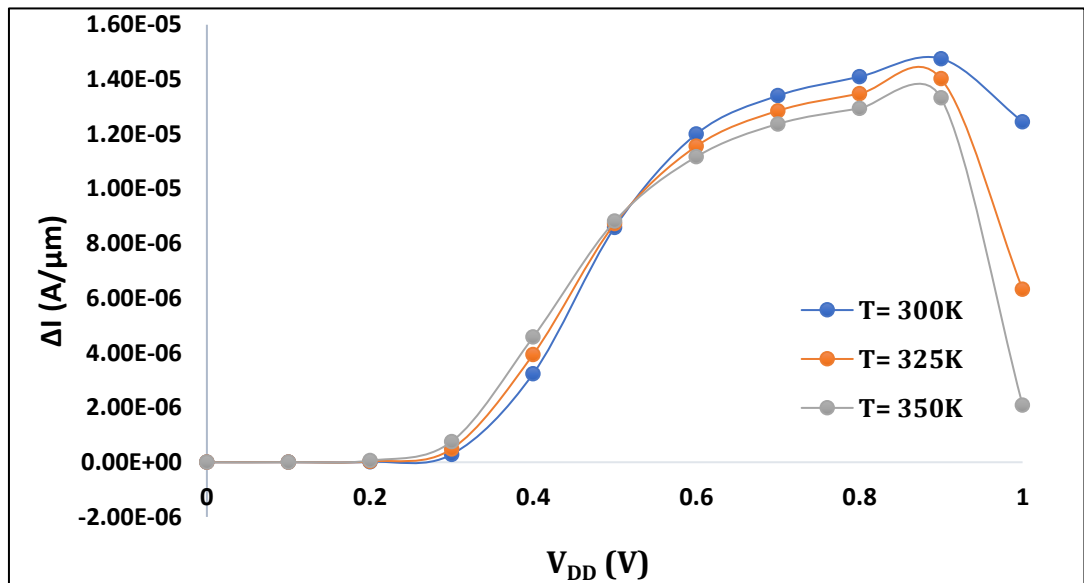
(c)

Figure 4.22 ΔI - T characteristics of FinFET (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

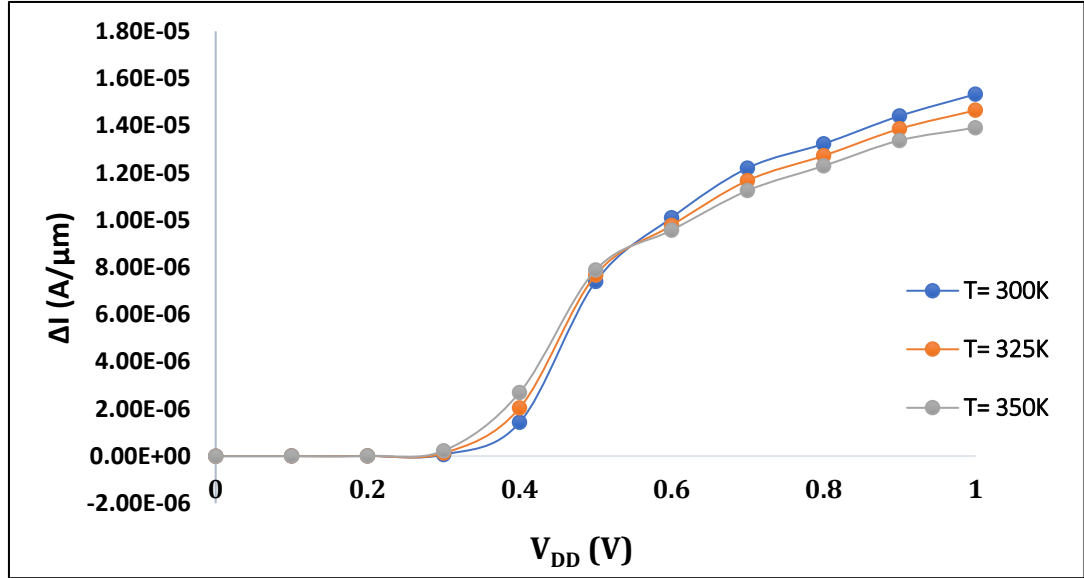
Figure 4.23 (a-c) indicate the influence of different temperatures on the 275, 300, 325, and 350 K power output clean gate (FinFET) on eight gates of different widths (10, 20, and 30 nm) and different power supply voltages. The results revealed that the maximum sensitivity (ΔI) is at $V_{DD} = 0.7$ V for 10 nm, $V_{DD} = 0.9$ V for 20 nm, and $V_{DD} = 1$ V for 30 nm. In the research, a significant relationship was observed between fluctuations at the moment, temperature, and voltage conditions, with the magnitude of ΔI decreasing as temperature increased and V_{DD} increased. The findings demonstrated that a working voltage of 1 V yields the highest sensitivity across various gate lengths (10, 20, and 30 nm). The transistor is most likely to work under $V_{DD} = 1$ V, especially at $L_g = 30$ nm, which will increase stability and sensitivity. Although $V_{DD} = 0.9$ V is also a good configuration with good performance, $V_{DD} = 1$ V has a much higher sensitivity and better electrical performance due to its temperature response. Such conclusions highlight the need to design gates to maximize the thermal and electrical characteristics of FinFETs, including L_g , W_g , and V_{DD} . This ensures better performance in high-sensitivity and thermal stability over a large temperature range.



(a)



(b)



(c)

Figure 4.23 Characteristics of ΔI with V_{DD} at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

The change in ΔI versus L_g is demonstrated in Figure 4.24. As the channel length increases from 10 nm to 30 nm, the current difference between the two increases gradually, indicating that longer channels provide a more constant current. This implies that the current management is determined by the dimension L_g . Short channels exhibit lower ΔI since intense short-channel effects can confuse matters. The longer channels minimise those effects, making the current more stable.

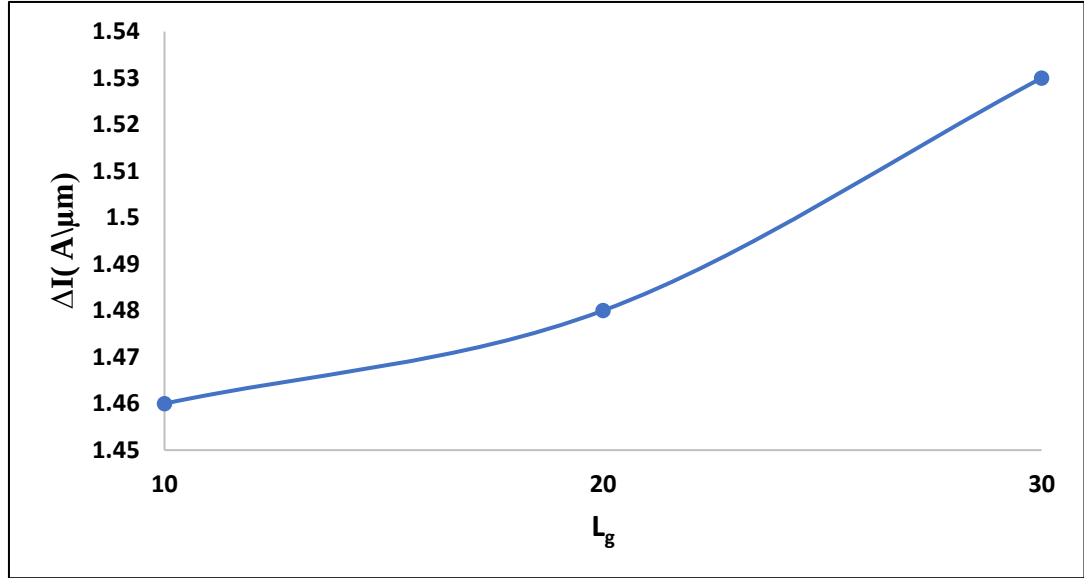


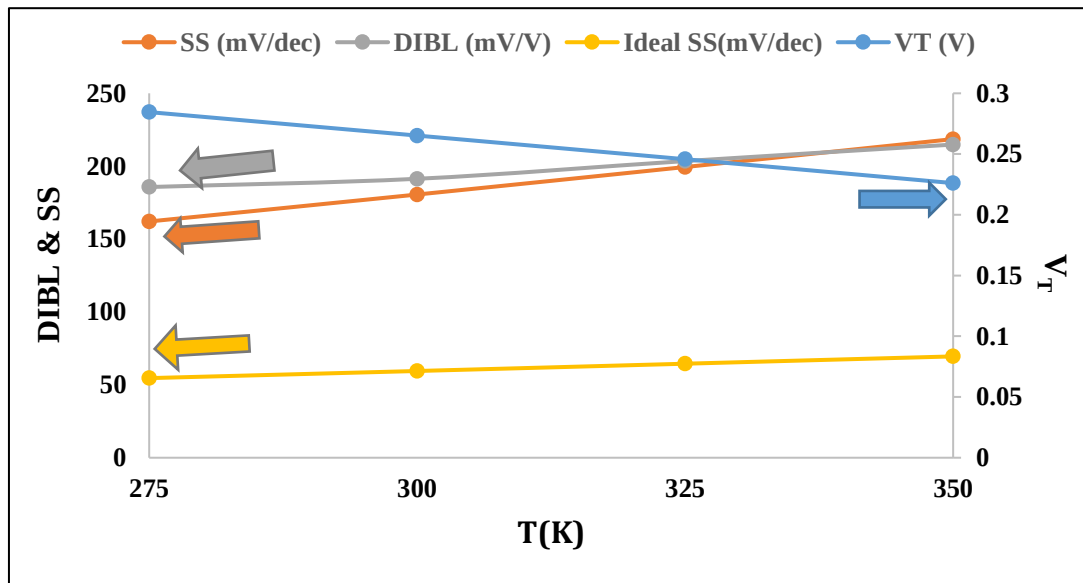
Figure 4.24 Characteristics of ΔI with L_g .

Figure 4.25(a) reveals the temperature-dependent characteristics of critical FinFET parameters of V_T , SS, and DIBL at operating temperatures 275 K, 300 K, 325 K, and 350 K, and $L_g = 10$ nm and $W_g = 10$ nm. These findings indicate that V_T changes gradually with increasing temperature (reducing from 0.28 V at 275 K to 0.22 V at 350 K). This decrease is primarily due to the DIBL effect, which lowers the channel potential barrier at the source and increases the OFF-state leakage current. In the case of SS, the values increase at 275 K (162 mV/dec) and 350 K (218.59 mV/dec), with the greatest deviation observed at 54.6 mV/dec, which is the optimum value. Interestingly, the SS tends to converge on the ideal reference value of 69.5 mV/dec at high temperatures, suggesting that its switching efficiency improves under high thermal conditions. In DIBL, a linear temperature dependence is observed, with leakage at 185.7 mV/V at 275 K, lower than at 350 K (214.83 mV/V). Temperature has a drastic impact on the OFF-state leakage properties of FinFETs.

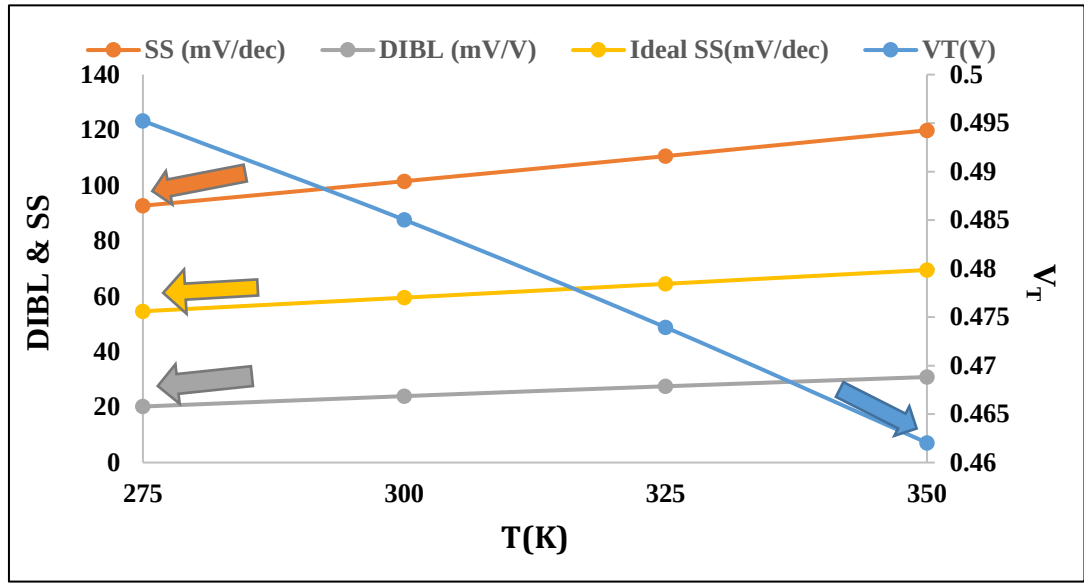
Figure 4.25(b) demonstrates how V_T , SS, and DIBL vary with temperature of a FinFET with $L_g = 20$ nm and $W_g = 10$ nm over the temperature range of 275, 300-350 K. V_T depicts a gradual decrease with increasing temperature (275-350 K), while SS and DIBL increase slowly. In particular, SS varies between 92.68 and 119.9 mV/dec, DIBL between 20.22 and 30.86 mV/V, and V_T between 0.49 and 0.46 V. The most negative departure of the ideal SS value of 54.6 mV/dec is observed at a temperature of 275 K, in which the SS is larger than 93.65 mV/dec. The rising temperature results in

the greatest increase in SS, with a maximum of 120.92 mV/dec. On the same note, DIBL will increase with temperature.

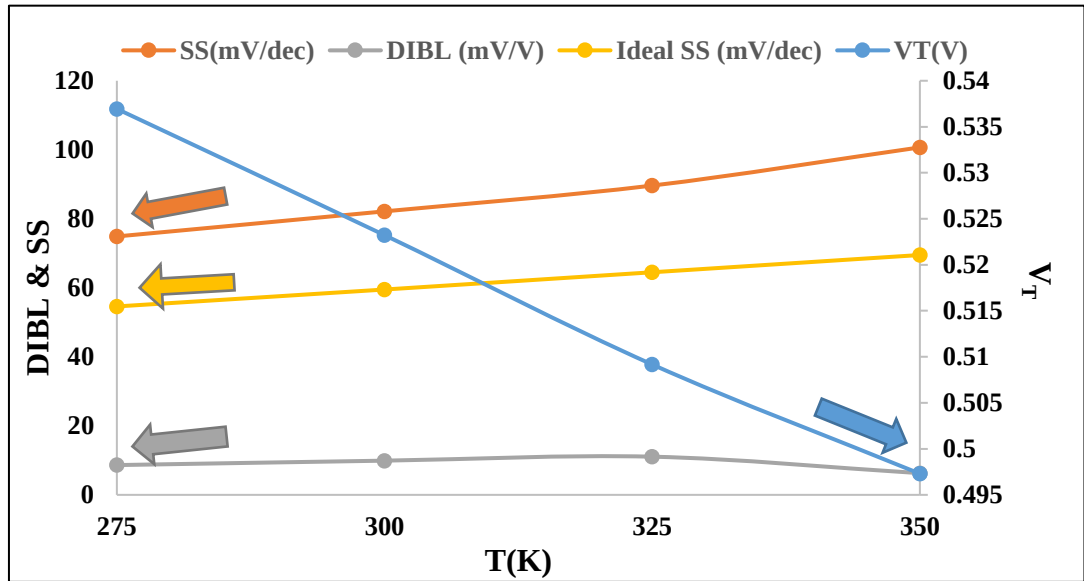
Figure 4.25(c) illustrates the interaction between V_T , DIBL, and SS when L_g and W_g are 30 nm and 10 nm, respectively, and how these factors affect FinFET performance at the same temperature. V_T starts dropping at 275 K, with a value of 0.53 V, and continues dropping to 350 K, with a value of 0.49 V. DIBL rises with temperature, from 8.62 mV/V to 20.04 mV/V, and SS rises by 74.88 mV/dec to 120 mV/dec. The SS value at 350 K is similar to 120 mV/dec, which is much greater than the desirable value of 69.5 mV/dec. SS is also closer to the ideal of 54.6 mV/dec, particularly at $L_g = 30$ nm and 275 K. These results demonstrate that L_g and the operating temperature must be optimized to achieve an optimal balance between device performance and stability. As temperature increases, DIBL continues to rise, emphasizing the impact of temperature on the device's electrical behaviour.



(a)



(b)



(c)

Figure 4.25 V_T , SS, and DIBL at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.26 reveals a correlation between the Min FinFET transistor channel lengths and electrical properties. It demonstrates that the optimal channel length is 20-30 nm, with the V_T value as large as possible (0.58 V), and that DIBL (5.57 mV/V) and

SS (82.2 mV/dec) tend to reach optimal values (54.6 mV/dec). The optimum SS is the subthreshold swing that provides the best trade-off between low current leakage and efficient switching in the transistor, balancing power consumption and device stability. These findings validate earlier researchers' [155] findings, which establish a linear correlation between the electrical properties of FinFET transistors and channel length. The figure depicts that increasing the channel length improves the device's subthreshold characteristics. At a gate length of 30 nm, the device characteristics approach long-channel behaviour, with SS = 82.2 mV/dec. However, as the gate length decreases to 10 nm, conventional SCEs become increasingly severe. This happens since a reduction in L_g leads to a lower V_T (0.35 V) and a degradation in the SS (185.78 mV/dec) due to charge sharing. As a result, the device exhibits higher DIBL (199.76 mV/V), further affecting its performance. To further support the identified tendencies, it will be necessary to critically compare previously published experimental and simulation-based studies. These findings in Figure 4.26 are highly consistent with the theory of electrostatic scaling of multi-gate devices proposed by Hisamoto and colleagues [145]. The theory implied that FinFET structures provide better control of short-channel effects than planar MOSFETs, especially at gate lengths greater than 20 nm. The SS values measured in their experimental apparatus at L_g values of about 25 nm were 70.85 mV/dec, and the DIBL was less than 50 mV/V, confirming the improved gate electrostatic integrity in this region.

Similarly, [146] have documented that in tri-gate FinFETs under a 22 nm technology node, the subthreshold swing measured was only 75.90 mV/dec, and the DIBL was about 60 mV/V when the fin dimensions were optimized. These values are closely consistent with the current measurements at $L_g = 30$ nm, where SS = 82.2 mV/dec and DIBL = 5.57 mV/V, and it is possible to state that, in the chosen device design, electrostatic control can be achieved competitively. Even the DIBL is lower due to the unique structural optimization adopted in this publication.

Conversely, excessive SS degradation (185.78 mV/dec) and DIBL (199.76 mV/V) occur when the channel length is reduced to less than 10 nm. This finding is consistent with the observation of [147], who reported that aggressive scaling below 14 nm leads to significant charge sharing, barrier thinning, and enhanced penetration of the drain field, thereby yielding DIBL values of over 150 mV/V in sub-15 nm Fin. This makes it clear that electrostatic scaling limitations have manifested as a physically

consistent performance degradation in the current investigation, rather than as an anomaly.

However, in some cases, advanced FinFET designs have been reported in the literature that demonstrate better subthreshold performance at ultra-scaled nodes using high-k dielectrics, metal-gate design, and strain enhancement [148]. The current device structure is focused more on geometric scaling analysis than on material engineering optimization, compared to such optimized industrial implementations. Thus, the deviation observed at 10 nm reflects the inherent electrostatic constraints of the traditional FinFET architecture under severe scaling, not a modelling effect.

In general, the consistency of the numerical results with available experimental data confirms the adopted simulation framework. It indicates that the parameters extracted reflect the physical effects underlying short-channel behaviour in scaled FinFET devices.

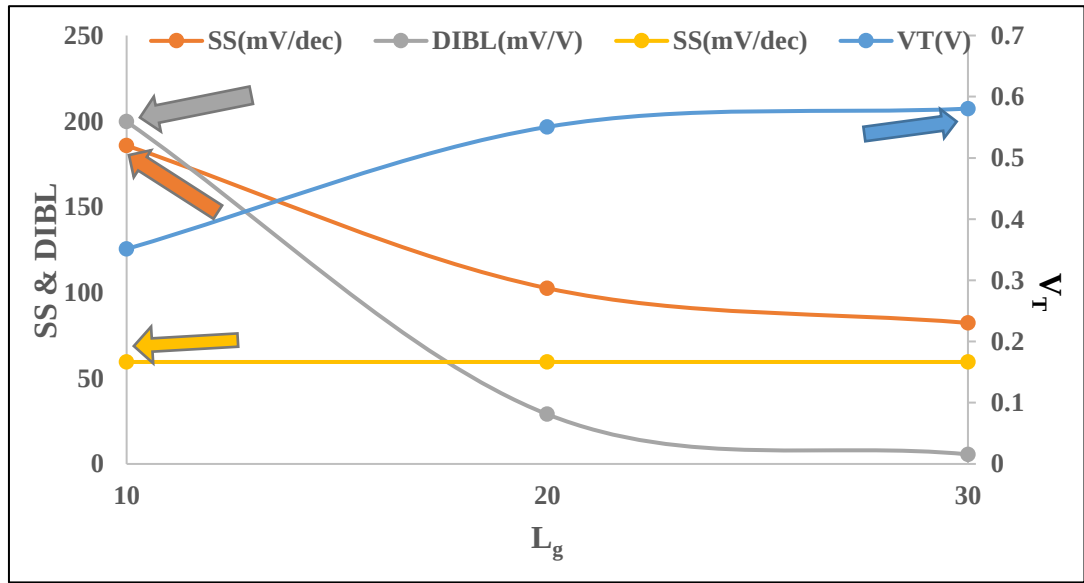
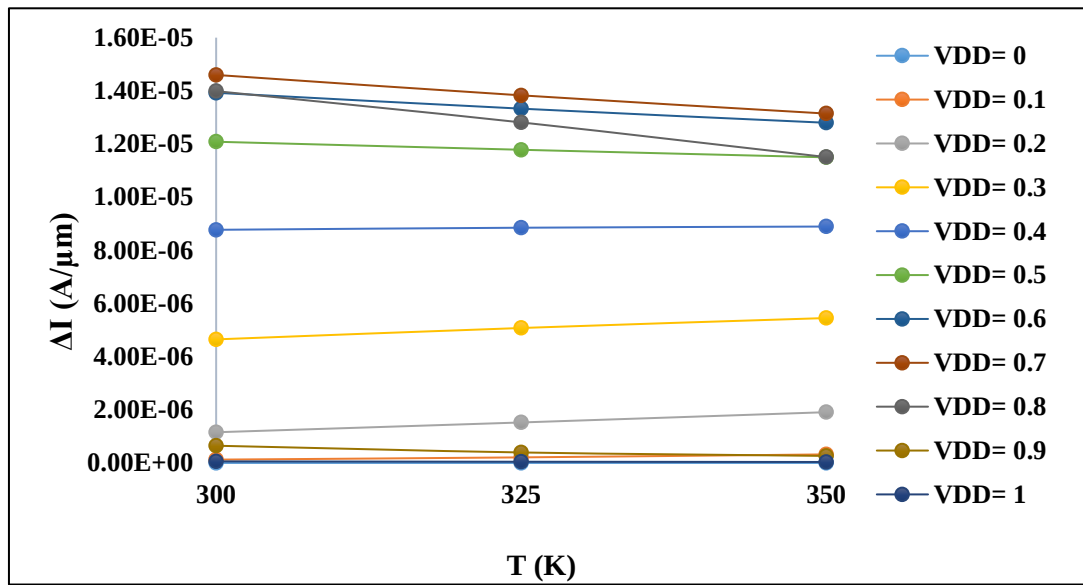


Figure 4.26 V_T , SS, and DIBL with L_g .

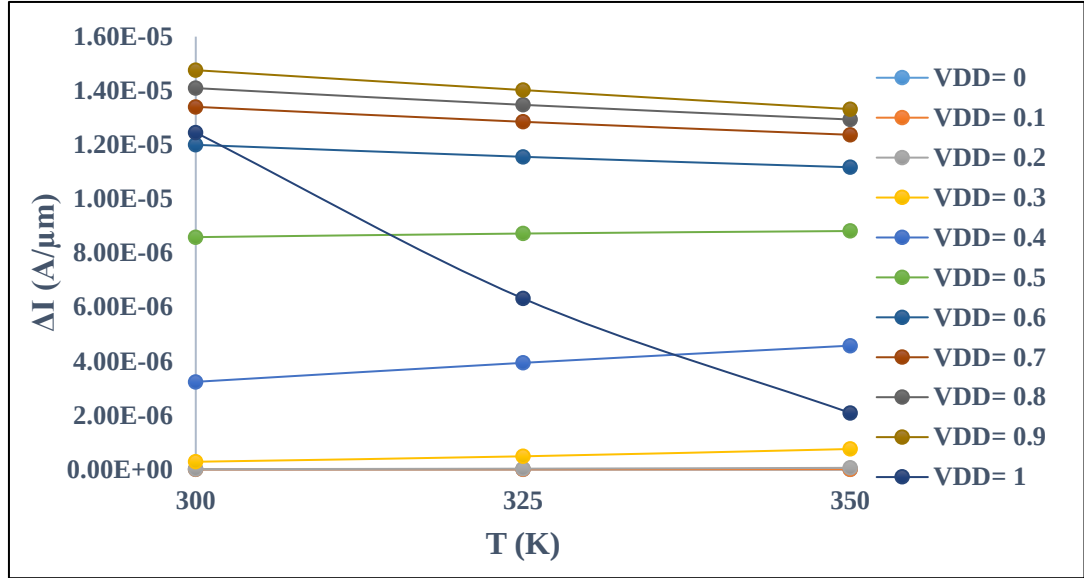
4.6.2 Effects of Temperature and Channel Length on $\text{Si}_{0.5}\text{Ge}_{0.5}$ -FinFET ($x = 0.5$) Characteristics

Figure 4.27(a–c) depict the variation in current for L_g of 10, 20, and 30 nm, with voltage increments of 0.1 V. The data indicate that as V_{DD} increases from 0 to 1 V, the current response increases, but the current exhibits both increases and decreases

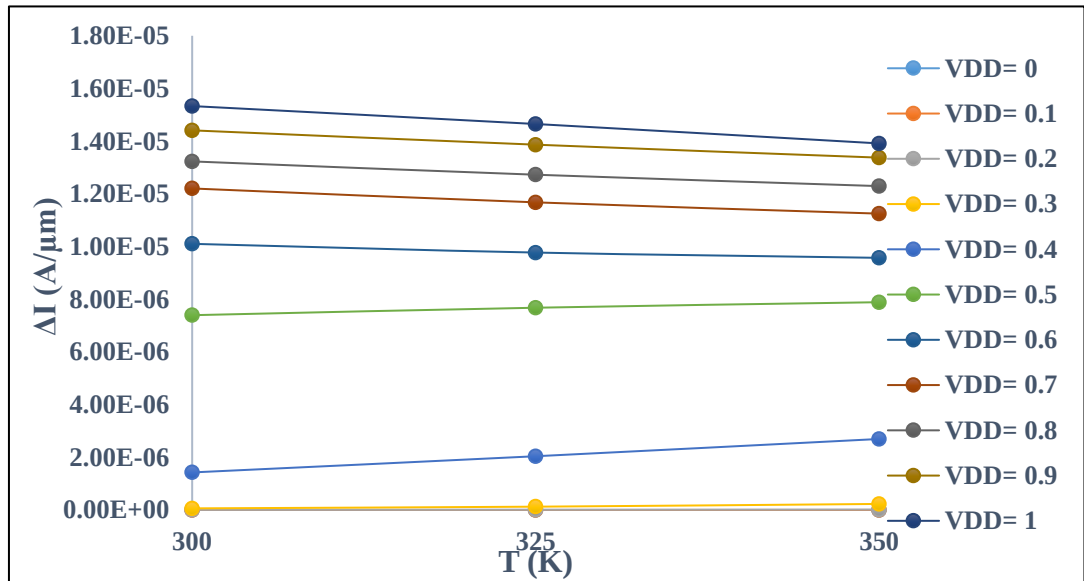
with temperature changes. The maximum sensitivity (max ΔI) in the V_{DD} tested range, however, is attained at higher temperatures (not lower), as expected. This is explained by the joint action of L_g , temperature, and the Ge mixing ratio ($x = 0.5$), which is particularly noticeable in this case. Figure 4.27(a) and (b) depict the optimal values of the coefficients of temperature sensitivity to $V_{DD} = 0.7$ and 0.9 V, respectively, for the L_g values of 10 and 20 nm. On the contrary, Figure 4.27(c) illustrates the least sensitivity at $L_g = 30$ nm for $V_{DD} = 1$ V. This indicates that the transistor performs best with $V_{DD} = 1$ V, where the greatest sensitivity (ΔI) is observed over the temperature range 325-350 K.



(a)



(b)

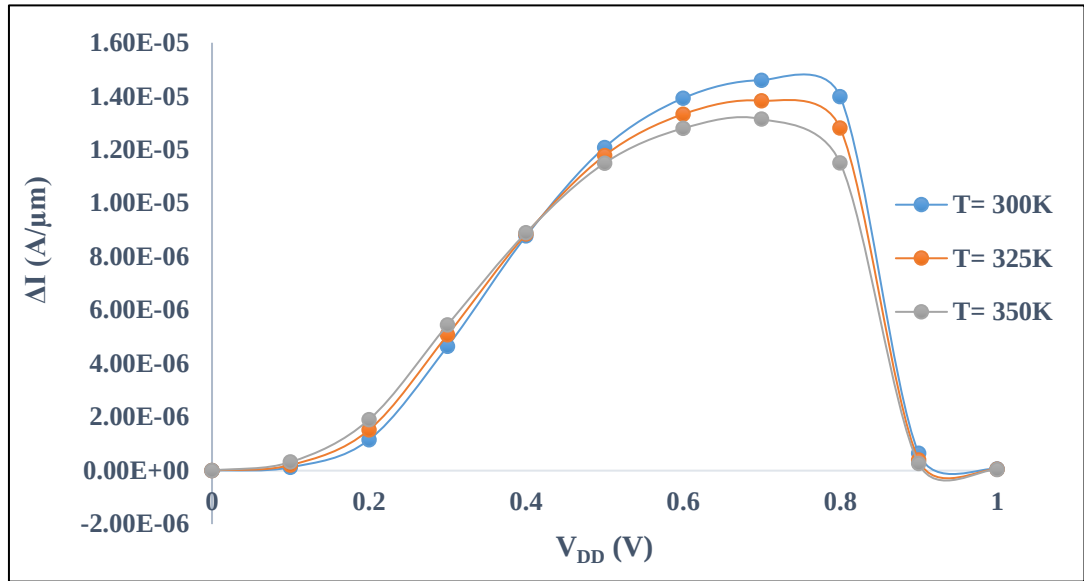


(c)

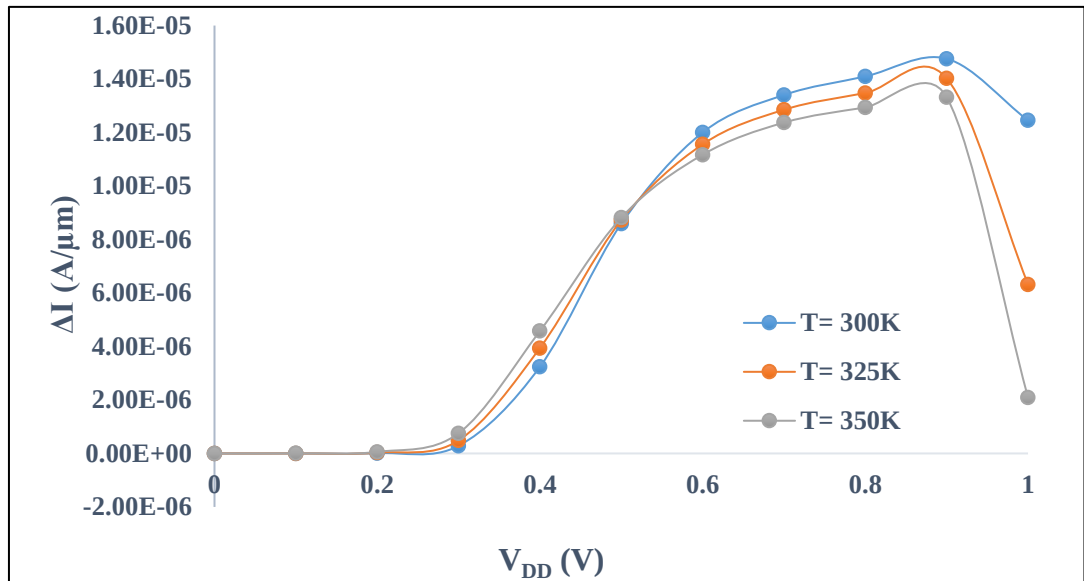
Figure 4.27 ΔI - T characteristics of FinFET (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.28 (a-c) present the variations in ΔI with declining V_{DD} at $T = 275, 300, 325$, and 350 K for L_g of 10, 20, and 30 nm. V_{DD} values of 0.7 V ($L_g = 10$ nm), 0.9 V ($L_g = 20$ nm), and 1 V ($L_g = 30$ nm) yielded maximum sensitivity, or max

ΔI . The highest sensitivity is 1 V for $L_g = 30$ nm, with $W_g = 10$ nm. The results indicate that ΔI increases with rising temperature and V_{DD} .



(a)



(b)

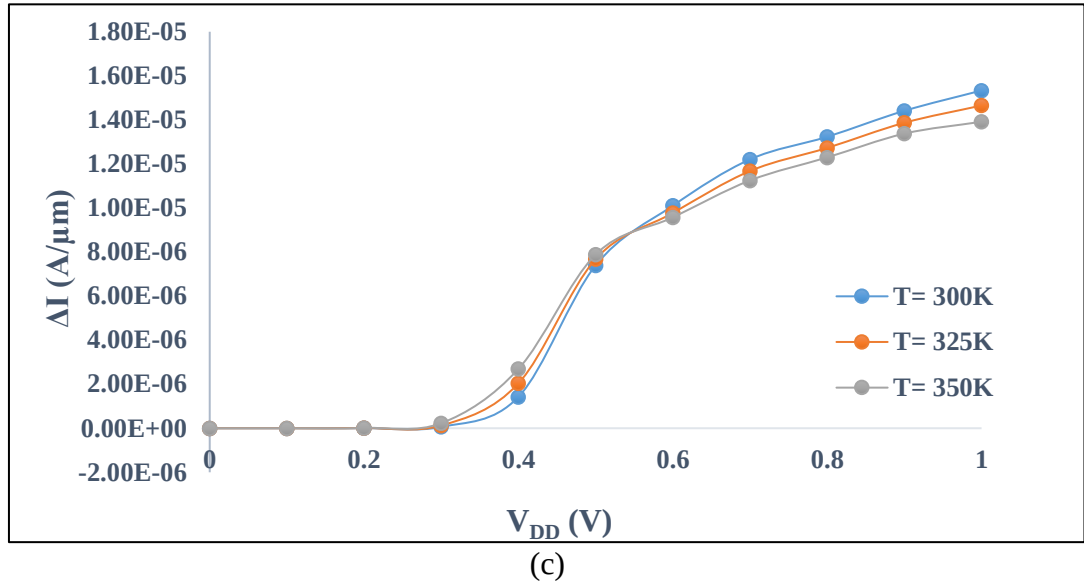


Figure 4.28 Characteristics of ΔI with V_{DD} at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.29 demonstrates the relationship between ΔI and L_g . The experiment reveals that ΔI increases with longer L_g , indicating better electrostatic control and lower short-channel effects. This tendency indicates greater stability and reliability of FinFET devices as L_g increases.

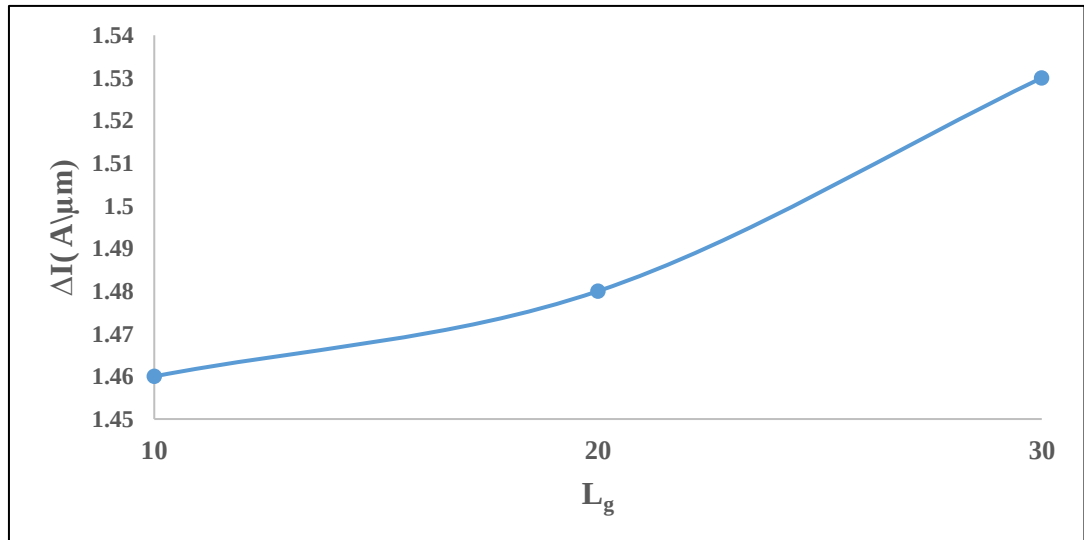


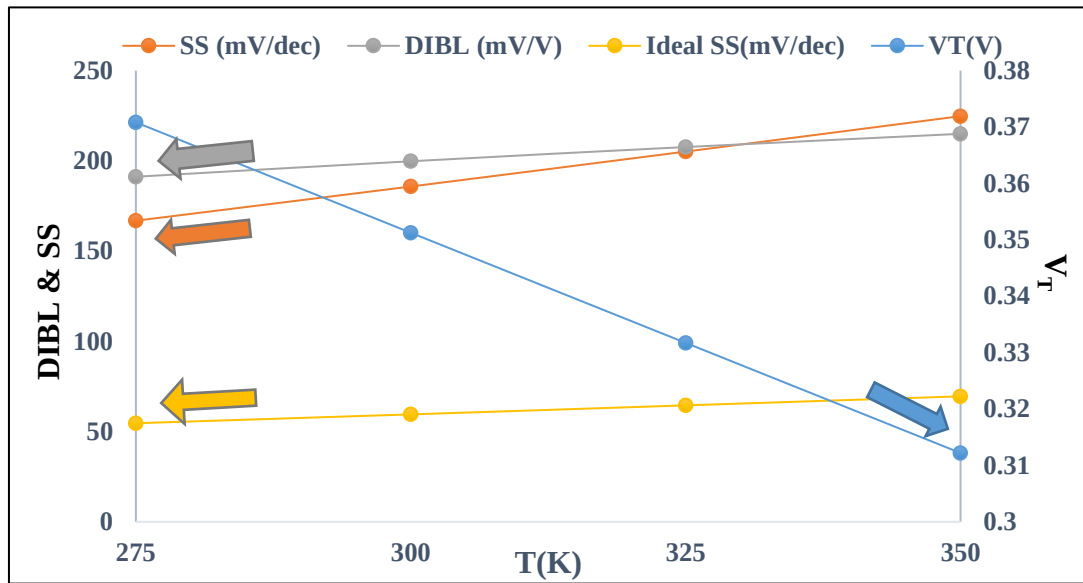
Figure 4.29 Characteristics of ΔI with L_g .

The temperature profiles for key FinFET characteristics are displayed in Figure 4.30(a). These characteristics include the SS, V_T , and DIBL. These were quantified at 275, 300, 325, and 350 K with $L_g = 10$ nm and $W_g = 10$ nm. V_T demonstrated a calculated decrease in voltage with increasing temperature from 0.37 V at 275 K to 0.31 V at 350 K. The higher the temperature, the greater the upsurge in V_{DD} and leakage current due to DIBL in the OFF state, and the greater the reduction in V_T from mitigating the source-increase channel potential barrier. With the temperature rising to 350 K, SS rose to 224.75 mV/dec, against 166.82 mV/dec at 275 K, the greatest departure from the ideal value of 69.5 mV/dec. At 350 K, SS, on the other hand, is closer to the ideal value of 54.6 mV/dec at 350 K. DIBL is found to continuously increase with rising temperature, with a value of 191.19 mV/V at 275 K, rising to 214.96 mV/V at 350 K. According to the study, the best transistor sizes are $L_g = 20$ and 30 nm at 350 K. V_T increases slowly with increasing oxide thickness, DIBL varies significantly, and SS varies significantly.

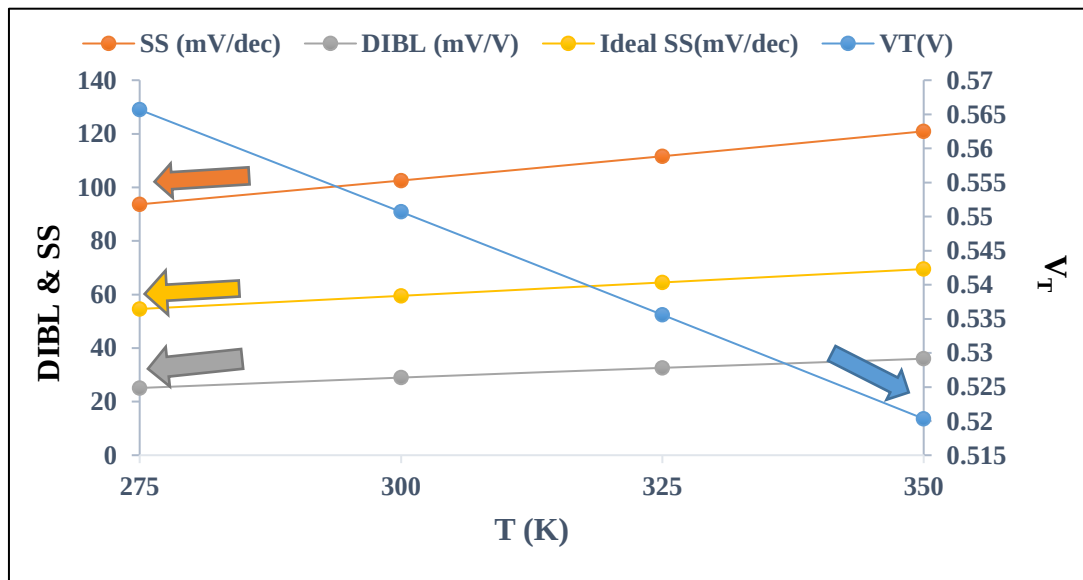
Figure 4.30(b) illustrates the behaviour of V_T , SS, and DIBL of FinFETs at the temperatures of 275, 300, 325, and 350 K with $L_g = 20$ nm and $W_g = 10$ nm. This figure depicts that V_T declines with temperature between 275 and 350 K, whereas SS and DIBL exhibit no decline, only a significant increase. In particular, the values of SS, DIBL, and V_T fall within the ranges of 93.6 to 120.92 mV/dec, 25.1 to 36.01 mV/V, and 0.56 to 0.51 V, respectively. The SS value at 350 K is the least deviant from the ideal SS reading of 54.6 mV/dec, as SS increases to 93.6 mV/dec. The SS with temperature dependence increases and peaks at 120.92 mV/dec as the temperature rises. Similarly, DIBL demonstrates a strong temperature dependence, making it sensitive to temperature fluctuations.

Figure 4.30(c) represents the interaction between V_T , DIBL, and SS and their interactive impact on the performance of the FinFET in the temperature scale of 275-350 K, $L_g = 30$ nm, and $W_g = 10$ nm. The value of V_T drops from 0.57 V at 275 K to 0.56 V at 350 K, a slight negative change that increases with temperature. DIBL slowly increases from 4.11 to 7.98 mV/V, while SS gradually increases from 75 to 97.25 mV/dec as temperature rises. The SS value at 350 K is 97.25 mV/dec, which is further from the ideal value of 69.5 mV/dec. The SS value at 275 K is also evidently close to the ideal value of 54.6 mV/dec that was observed in this range. These findings substantiate the strong temperature sensitivity of V_T , DIBL, and SS, and highlight the

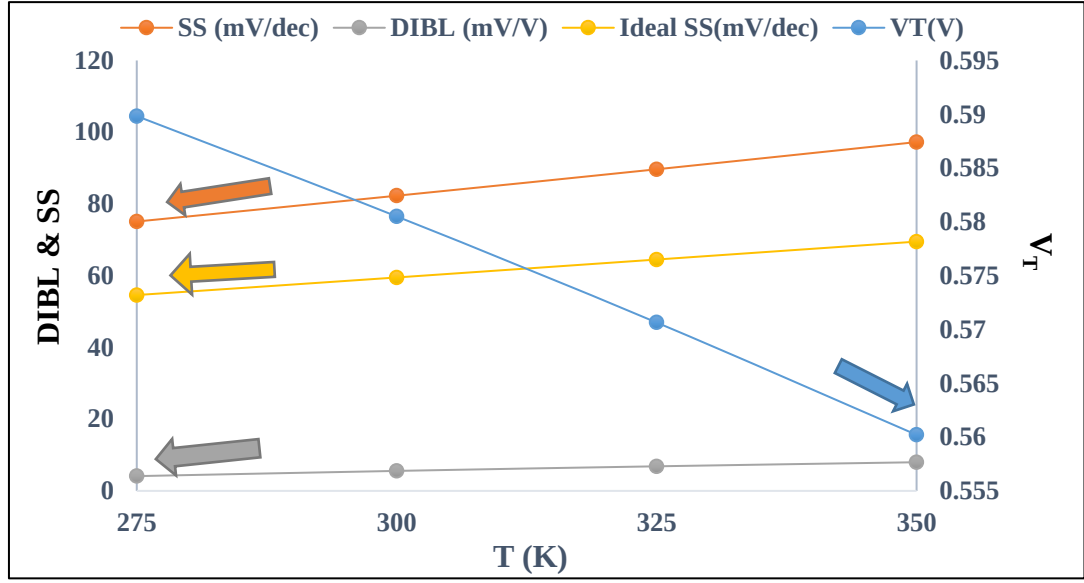
importance of optimizing these parameters to ensure the high reliability of FinFET device functionality.



(a)



(b)



(c)

Figure 4.30 V_T , SS, and DIBL at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.31 displays the characteristics of V_T , DIBL, and SS in cases of different FinFET channel lengths (10-30 nm) with $W_g = 10$ nm. V_T value beginning at 0.50 V ($L_g = 10$ nm), gradually increases to 0.55 V ($L_g = 20$ nm), and goes on increasing slowly with rise in L_g to 0.58 V ($L_g = 30$ nm). The DIBL value starts at 199.7 mV/V at $L_g = 10$ nm and decreases to 5.57 mV/V at $L_g = 30$ nm. Meanwhile, the SS value is initially at $L_g = 10$ nm, 185.7 mV/dec, and progressively decreases to 82.2 mV/dec at $L_g = 30$ nm, indicating that the subthreshold characteristics improve with increasing channel length. These findings indicate that V_T rises slowly along the channel length, whereas DIBL falls sharply at short channel lengths, particularly around $L_g = 20$ nm. SS diminishes and approaches the optimum value (54.6 mV/dec) at $L_g = 20$ nm, indicating that this length offers the best performance with minimum power consumption as applied in the test. Such results are consistent with prior work [163], which indicates that the electrical characteristics of FinFETs depend on L_g . Simulations of the PADRE device demonstrate that the DIBL and SS grow dramatically as the gate length decreases. This phenomenon occurs since a shorter gate length allows the drain electric field to encroach further into the channel, giving the gates greater control over the channel and a larger role in device conduction through the drain potential.

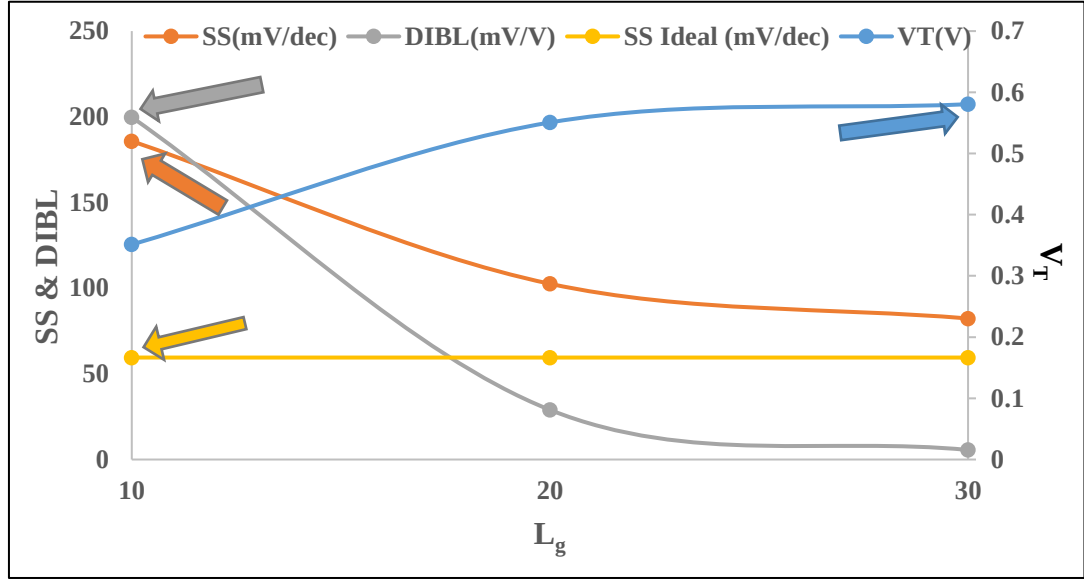


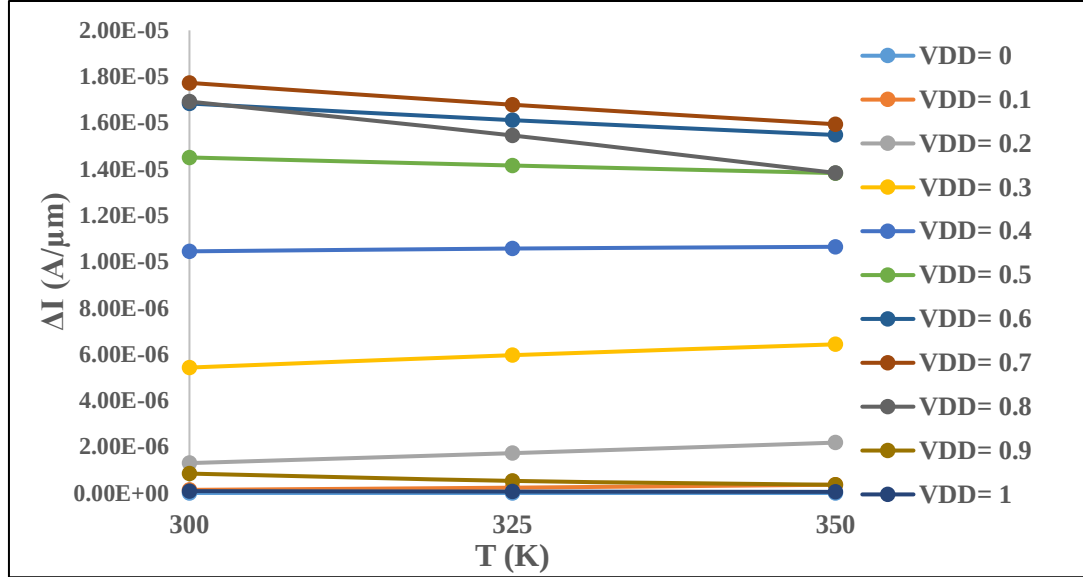
Figure 4.31 V_T , SS, and DIBL with L_g .

Si-Ge FinFETs are better than Si FinFETs, especially with respect to higher saturation current and voltage. Si is modified with Ge atoms, which diminish atomic forces and increase electron movement. The increase in electrical conductivity results in higher output current in Si-Ge FinFETs. Furthermore, it is found that the current leakage of the Si-Ge FinFETs is minimal, particularly at shorter channel lengths (10, 20, and 30 nm), due to stronger electric fields in the source and drain regions. Si-Ge FinFETs are therefore the best choice for electronic devices that require high switching speed and low current leakage [164].

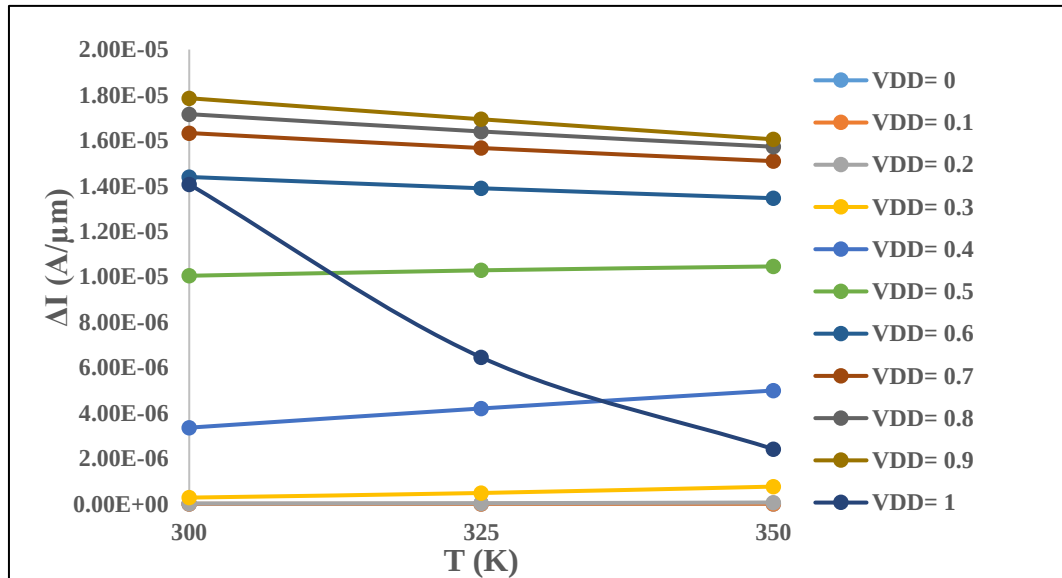
4.6.3 Effects of Temperature and Channel Length on $\text{Si}_{0.25}\text{Ge}_{0.75}$ -FinFET ($x = 0.75$) Characteristics

Figure 4.32(a–c) illustrate the variation of current (I) L_g at 10, 20, and 30 nm increments of voltage by 0.1 V. These findings indicate that current sensitivity (ΔI) has a non-linear dependence on V_{DD} with increasing temperature. In particular, the peak sensitivity is observed at $V_{DD} = 0.7$ V with $L_g = 10$ nm, $V_{DD} = 0.9$ V with $L_g = 20$ nm, and $V_{DD} = 1$ V with $L_g = 30$ nm. Figure 4.32(a-b) display the temperature sensitivity coefficients for $L_g = 10$ and 20 nm at $V_{DD} = 0.7$ V and 0.9 V, respectively. Figure 4.32(c) presents the peak sensitivity at $L_g = 30$ nm for $V_{DD} = 1$ V. These results indicate that

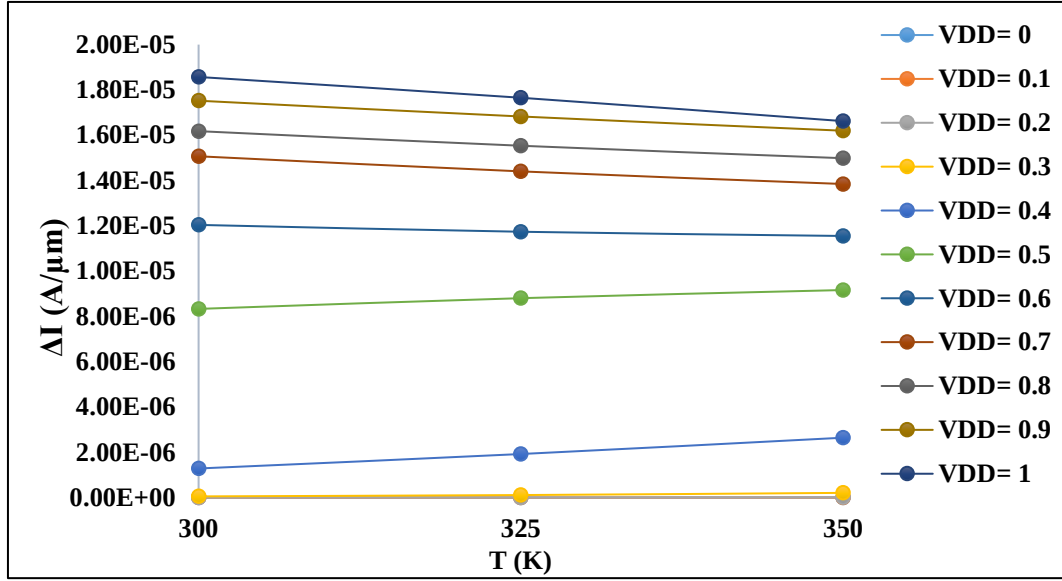
the transistor achieves optimal performance at $V_{DD} = 1$ V, where it provides the highest sensitivity and stability across the 325–350 K temperature range.



(a)



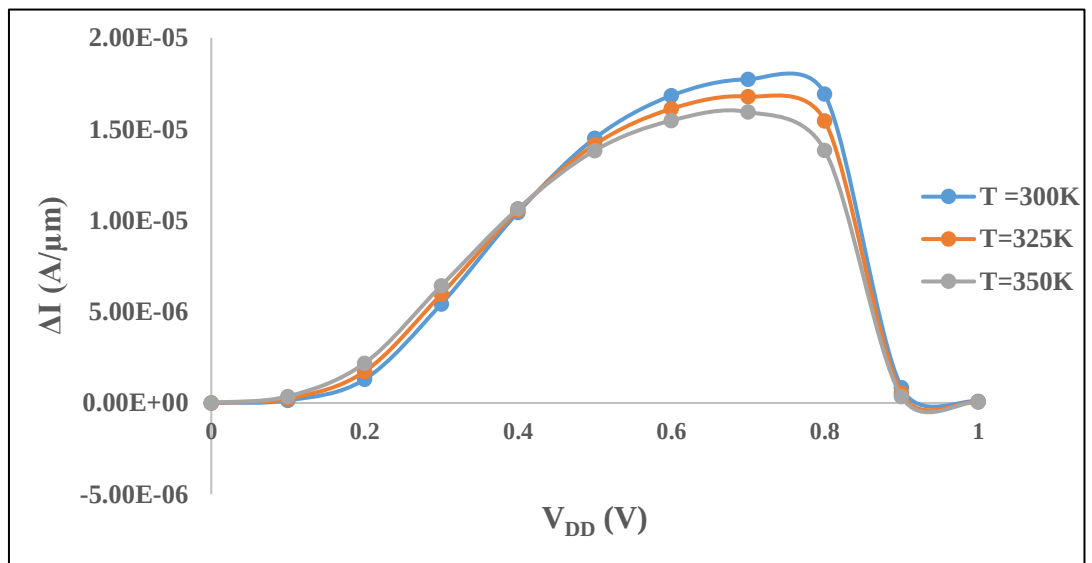
(b)



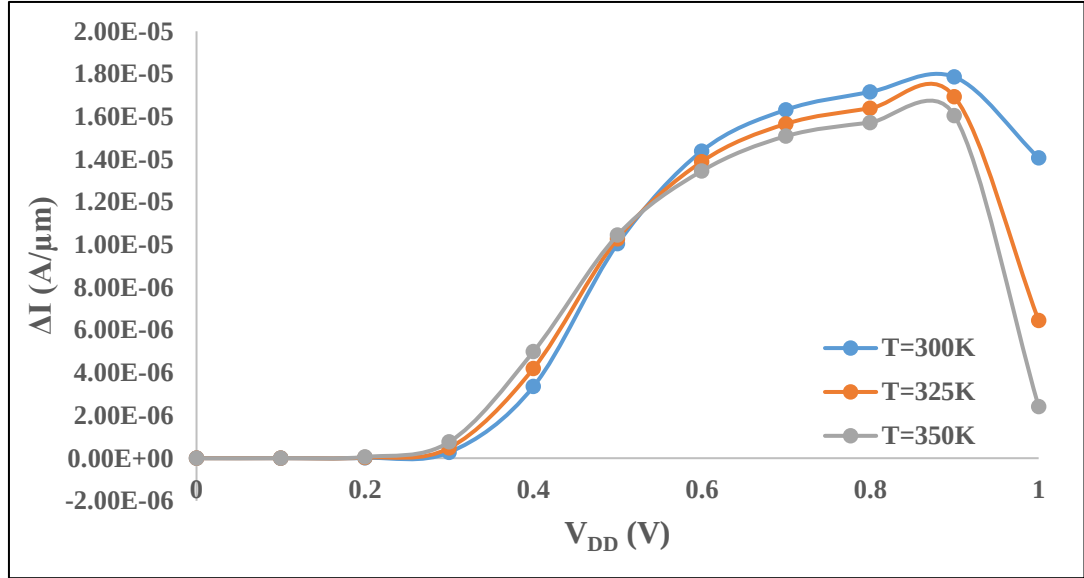
(c)

Figure 4.32 ΔI - T characteristics of FinFET at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

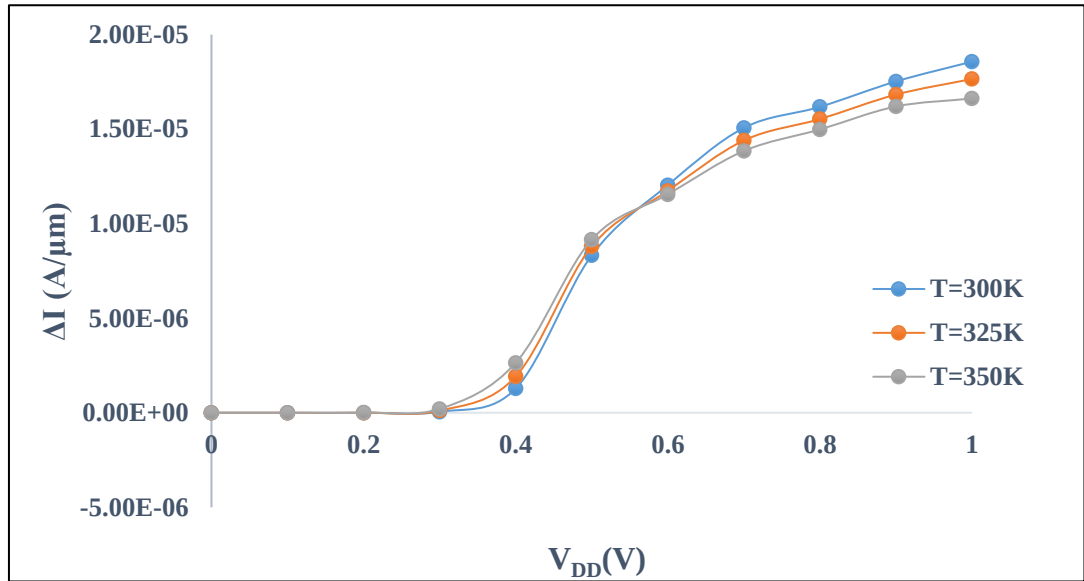
At temperatures of 275, 300, 325, and 350 K, the variations in ΔI due to increasing V_{DD} are depicted in Figure 4.33 (a through c). These variations are observed for gate lengths of $L_g = 10$, 20, and 30 nm. The maximum sensitivity, or max ΔI , is achieved at $V_{DD} = 0.7$ V for $L_g = 10$ nm, $V_{DD} = 0.9$ V for $L_g = 20$ nm, and $V_{DD} = 1$ V for $L_g = 30$ nm. As temperature and V_{DD} increase, ΔI rises accordingly, indicating that the transistor demonstrates the highest sensitivity to both.



(a)



(b)



(c)

Figure 4.33 Characteristics of ΔI with V_{DD} at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.34 demonstrates the results for 10, 20, and 30 nm, respectively. The curve reveals a slow increase in ΔI with increasing L_g . This indicates that the shorter the channels used in the devices ($L_g = 10$ nm), the higher the ΔI value. The longer the

channels used ($L_g = 20$ and 30 nm), the smaller the current difference shall be, since the SCEs are suppressed.

The channel electrostatic control can explain the observed behaviour. The shorter L_g (10 nm), the greater the influence the drain voltage has on the potential barrier at the source, and the greater is the leakage, the less is the electrostatic control, which translates to a higher ΔI . On the other hand, with longer channel lengths ($L_g = 20$ 30 nm), the electrostatic integrity is enhanced and effectively prevents SCEs, thus resulting in a decrease in ΔI .

These results agree with previous studies on SS, DIBL, and V_T , which reported steadier, more desirable values at $L_g = 20$ and 30 nm. Consequently, while shorter channel lengths are better at enhancing ΔI , longer channel lengths are better at suppressing SCEs. Therefore, they should be chosen to achieve better SCE suppression in $\text{Si}_{1-x}\text{Ge}_x$ FinFETs for increasingly advanced nanoscale FinFET applications.

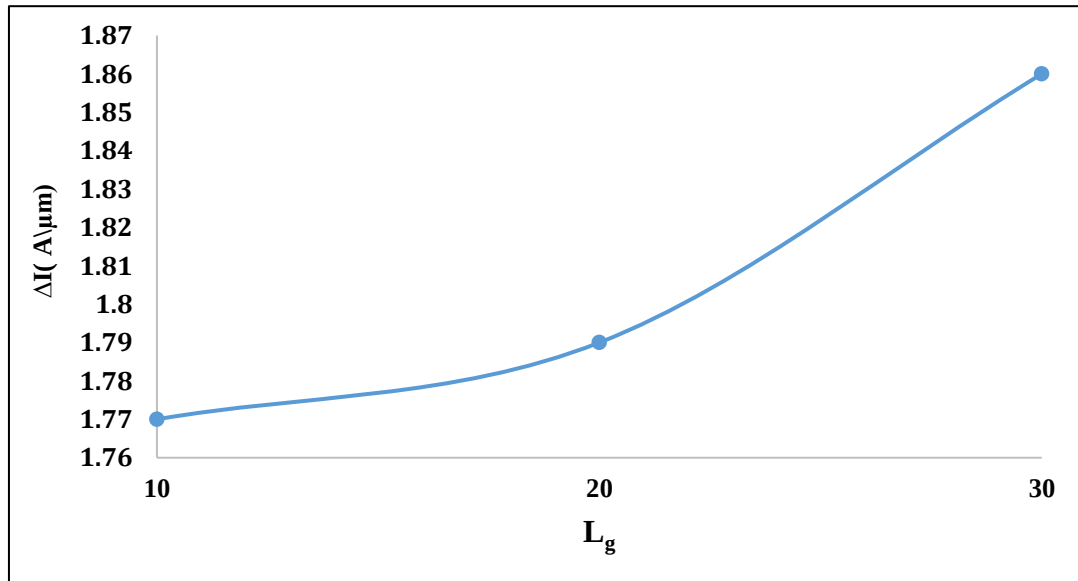


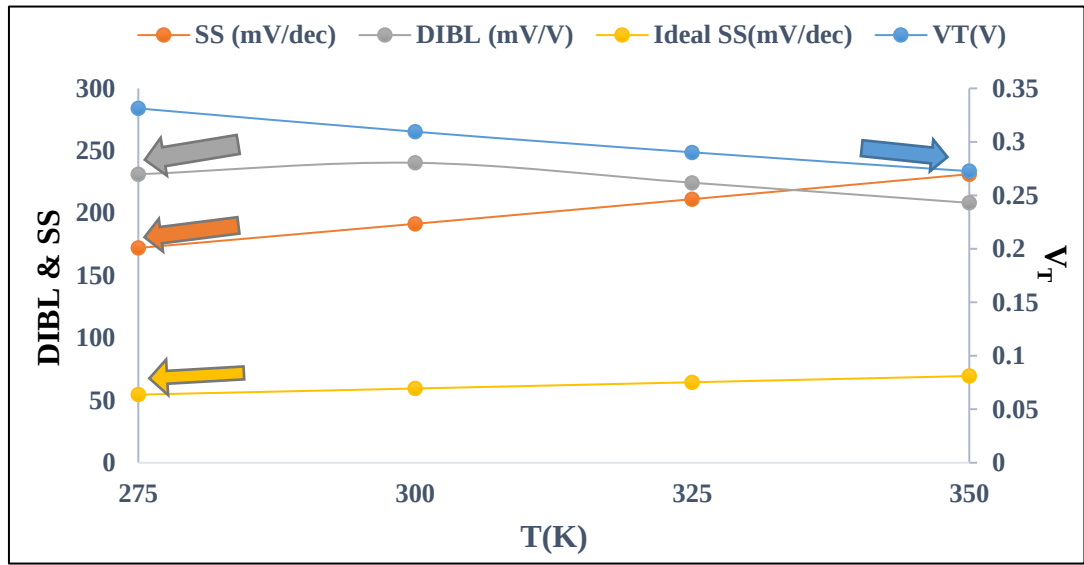
Figure 4.34 Characteristics of ΔI with L_g .

Figure 4.35(a) illustrates the temperature curves of key FinFET parameters. SS, V_T , DIBL, estimated at 275, 300, 325, and 350 K, using $L_g = 10$ nm and $W_g = 10$ nm. V_T decreases gradually with increasing temperature, from 0.33 V at 275 K to 0.27 V at 350 K. This is due to a reduced potential barrier at the source, which intensifies DIBL and increases leakage current in the OFF state. The value of SS at 350 K is also taken as 172.1 mV/dec, which is higher than at 275 K (231.2 mV/dec). This increment

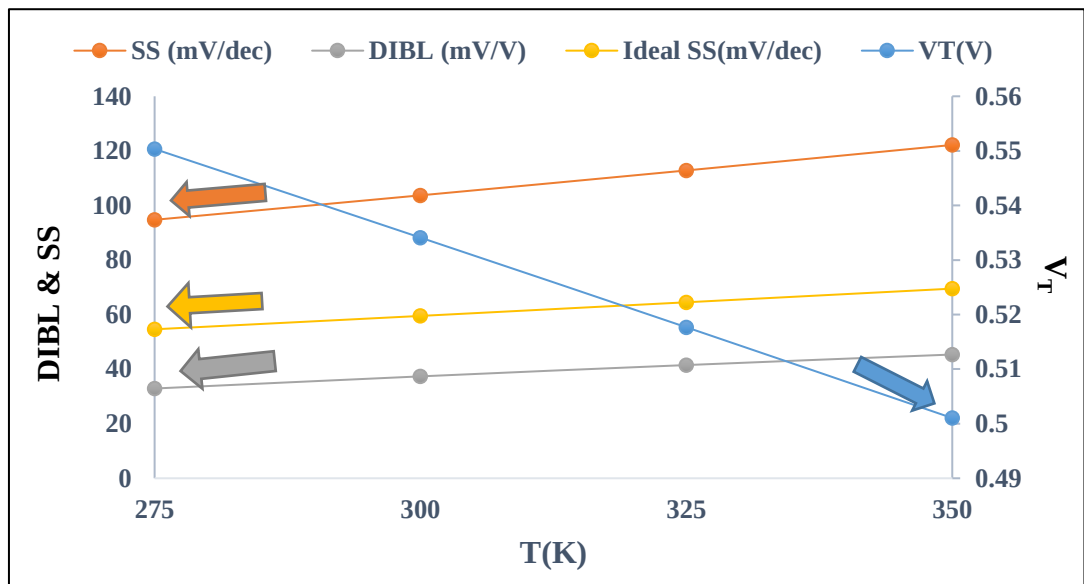
indicates that SS increases with temperature, contradicting the conceptual ideal of 69.5 mV/dec. The SS value is about 350 K, which seems much higher than the ideal value of 54.6 mV/dec. DIBL increases gradually with temperature up to 300 K, rising from 231.17 mV/V at 275 K to 240.4 mV/V at 300 K. However, beyond 300 K, DIBL begins to decrease, slowly dropping to 208.29 mV/V at 350 K. The trend depicts an initial increase in DIBL at the onset of the temperature increase, followed by a subsequent decrease as the temperature rises. The influence of the Ge ratio ($x = 0.75$) is indeed felt. The above behaviour confirms that DIBL is also thermally sensitive, particularly at low temperatures. The findings indicate that the transistor sizes at an optimum size are $L_g = 20, 30$ nm at 350 K, which give maximum performance when the test is conducted. In addition, V_T increases gradually with increasing oxide thickness, whereas DIBL and SS vary very slowly with temperature.

Figure 4.35(b) illustrates the V_T , SS, and DIBL behaviour of a FinFET with L_g and W_g 20 nm and 10 nm at 275, 300, 325, and 350 K. The graph indicates that V_T slowly declines with increasing temperature, from 0.56 V at 275 K to 0.50 V at 350 K. In the meantime, SS also rises slowly, with 94.73 mV/dec being recorded at 275 K, and 122.16 mV/dec at 350 K. This indicates a slow rise in SS, which is not an ideal value of 54.6 mV/dec (275 K), but yet a constant rise in increase with temperature rise. The consistent increase in DIBL with increasing temperature ranges from 32.89 mV/V at 275 K to 45.35 mV/V at 350 K. The results indicate that both DIBL and SS are highly influenced by temperature, with one illustrating a steadily increasing trend and the other demonstrating an increase in deviation from the optimal value as temperature increases.

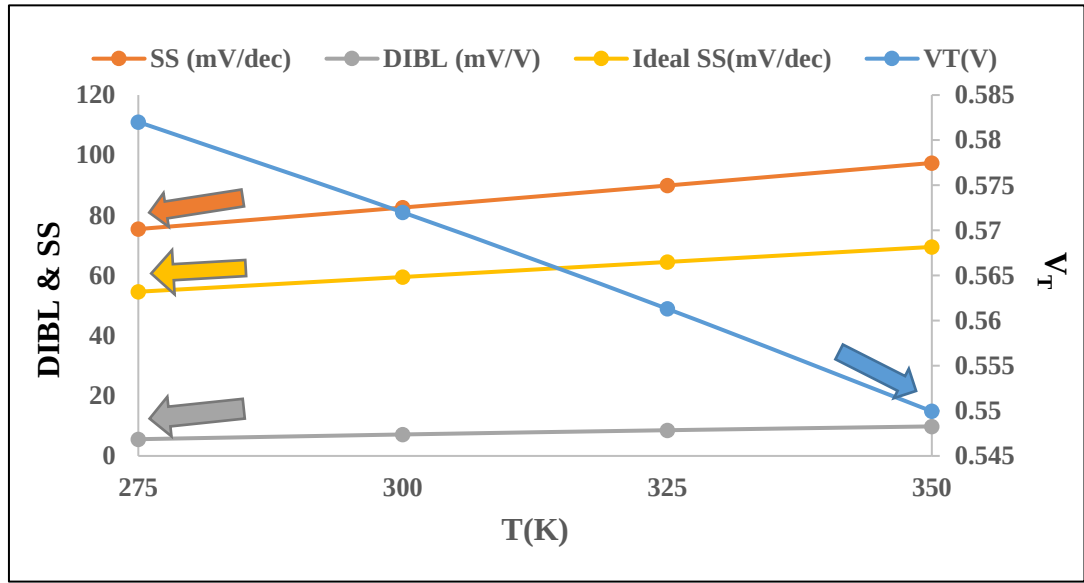
Figure 4.35(c) reveals that V_T , DIBL, and SS have a relationship with each other and their effects on the performance of the FinFET at temperatures between 275 and 350 K with $L_g = 30$ nm and $W_g = 10$ nm. With increasing temperature, V_T decreases slowly and nonlinearly: 0.56 V at 275 K and 0.51 V at 350 K. DIBL increases up to 9.82 mV/V and SS up to 122.16 mV/dec at 350 and 375 K, respectively, and continues to rise. The SS value of 350 K is observed to be 122.16 mV/dec, which is not equal to the ideal SS value (69.5 mV/dec) at 350 K. This reflects that subthreshold characteristic are aggravated with an increase in temperature. On the contrary, DIBL increases with temperature, making it sensitive to temperature changes. All these findings demonstrate that both SS and DIBL exhibit steadily increasing trends with temperature, indicating their critical impact on device performance.



(a)



(b)



(c)

Figure 4.35 V_T , SS, and DIBL at (a) $L_g = 10$ nm; (b) $L_g = 20$ nm; (c) $L_g = 30$ nm.

Figure 4.36 illustrates the character of V_T , DIBL, and SS at various lengths of channel ($L_g = 10, 30$ nm), and $W_g = 10$ nm. It has been reported that V_T increases from 0.30 V ($L_g = 10$ nm) to 0.57 V ($L_g = 30$ nm), indicating a gradual increase with increasing channel length. At $L_g = 10$ nm, DIBL is 240.4 mV/V at V, and at $L_g = 30$ nm, it is 7.14 mV/V at V, with a persistent downward trend as channel length increases. Conversely, SS has a starting point of 191.5 mV/dec at $L_g = 10$ nm, and this value falls to 82.6 mV/dec at $L_g = 30$ nm, with the value decreasing gradually with increasing channel length. The optimal SS value is obtained at $L_g = 20$ nm, indicating that 20 nm is the optimal channel length for the FinFETs under the conditions tested. The findings suggest that $L_g = 20$ -30 nm is the best channel length range, as illustrated in the figure, since V_T is rising and SS and DIBL are declining. The results are consistent with previous works [23], indicating that the electrical characteristics of FinFETs are directly proportional to the length of channels, 10-30 nm long. FinFETs can be affected by L_g , Ge content in $\text{Si}_{1-x}\text{Ge}_x$ alloys, and temperature. The Ge density ratio increases electrical properties (carrier mobility) while increasing temperature sensitivity. With increasing temperature, SS increases and V_T shifts, worsening device performance, particularly at low power. The channel length influences electrostatic control: shorter lengths enhance short-channel effects, while longer channels enhance stability. It is important to

optimize the Ge ratio, L_g , and thermal management to gain high performance and low power consumption in FinFETs [155]. The electrostatic behaviour, as summarized in Table 4.1, is typical of the overall scaling behaviour reported in the earlier literature. The degradation at $L_g = 10$ nm is worse than that of purely silicon-based FinFETs. In particular, the obtained SS (191.5 mV/dec) and DIBL (240.4 mV/V) are higher than the upper limits reported in recent articles with an area below 15 nm. This non-conformance is explained by the synergistic effects of Ge-induced reductions in band gap and increases in intrinsic carrier concentration, as well as temperature-dependent transport processes, which together disrupt gate electrostatic control at aggressively scaled dimensions. On the other extreme, the device tends towards long-channel behaviour at $L_g = 30$ nm, and the SS and DIBL values are similar to those observed in the early multi-gate FinFET demonstrations. This alignment suggests that electrostatic stabilization occurs at L_g that is much longer than the natural scaling length.

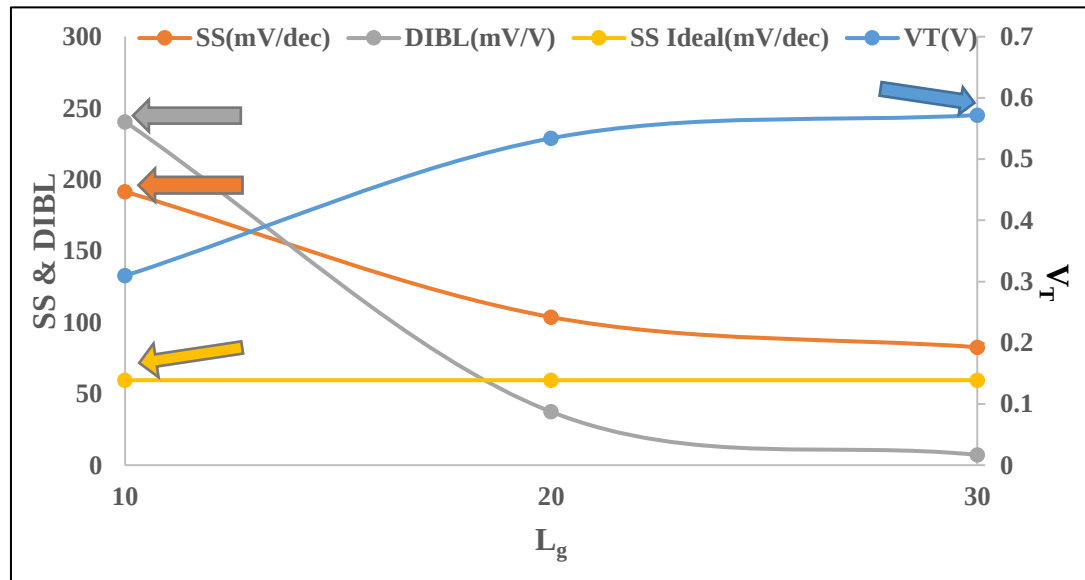


Figure 4.36 V_T , SS, and DIBL with L_g .

Table 4.1

Comparative Benchmark Table for FinFET Electrostatic Parameters

Study	Channel Material	L_g (nm)	V_T (V)	SS (mV/dec)	DIBL (mV/V)	Key Observation
[5]	Si	~30	~0.55	70–90	< 50	Strong electrostatic control in a double-gate structure
[165]	Si	14	0.40–0.45	110–130	120–160	Pronounced SCE below 20 nm
[139]	Si-Ge	10 – 15	0.32–0.38	150–180	170–220	Ge improves mobility but increases DIBL sensitivity
[166]	Si	<20	0.35–0.42	120–160	130–190	Electrostatic degradation is governed by the scaling length
This Work ($L_g = 10$ nm)	$Si_{1-x}Ge_x$	10	0.30	191.5	240.4	Strong SCE due to Ge coupling + thermal effects
This Work ($L_g = 30$ nm)	$Si_{1-x}Ge_x$	30	0.57	82.6	7.14	Near long-channel behaviour and electrostatic recovery

Overall, the study concludes that a channel length of 20 nm is an effective choice for enhancing the electrical characteristics of $Si_{0.25}/Ge_{0.75}$ -FinFETs by maximizing the most important device characteristics, including V_T , SS, and DIBL. This optimization is especially affected by the Si-Ge alloy composition. The higher the Ge content, the higher the carrier mobility and, hence, the better the device performance. The findings indicate that an increased Ge composition in the form of $Si_{0.25}/Ge_{0.75}$ has reduced resistance and enhanced current flow through the FinFET devices, particularly at higher temperatures. Furthermore, sensitivity also varies with operating temperature between 275 and 350 K, with an optimum bias of 1.0 V for 20 nm and 0.9 V for 30 nm channel lengths. The larger Ge proportion tends to lower V_T , enhancing transistor performance at lower operating voltages. The high Ge content also alters the crystal structure, reducing the lattice mismatch and stabilizing the devices' thermal and electrical properties. The devices' behaviour changes with increasing temperature, as V_T and

DIBL become less sensitive, while SS becomes more sensitive. The present study, in addition to confirming previous literature, reveals that careful attention to temperature control and channel-length adjustment is critical for advancing semiconductor device technology. Optimization of the Si-Ge alloy composition is further employed to enhance temperature-dependent properties, with high Ge percentages preferred to improve electrostatic integrity and device stability. These findings confirm that Si-Ge composition and channel length play important roles in improving FinFET performance, particularly under high-temperature conditions for next-generation applications.

4.7 Effects of x ratio on the Temperature of Si_{1-x}Ge_x-FinFET Characteristics

Si_{1-x}Ge_x alloys, with varying Si and Ge compositions, play a major role in the efficiency of FinFET transistors. With increasing Ge content, significant changes occur in the device's thermal and electrical characteristics, and several important parameters, such as SS, DIBL, and V_T, can be observed. These effects increase with temperature between 275 K and 350 K, indicating the importance of both temperature regulation and the Ge ratio in optimizing device performance.

The Ge concentration in Si_{1-x}Ge_x FinFET transistors is a significant factor in the dependence of L_g on the key parameters SS, DIBL, and V_T. L_g and temperature are the major factors that affect SS, as presented in Table 4.2, whereas the Si and Ge ratios have a lesser effect. In particular, the SS values for pure Si (x = 0) and pure Ge (x = 1) are 74.22 mV/decade and 76.11 mV/decade, respectively, at an L_g of 30 nm. This trend suggests that an increase in the Ge ratio has no negative effect on SS. Instead, it emphasizes that SS relies heavily on L_g, in which longer channel lengths improve transistor performance without compromising the threshold required for low-power switching.

Equally, DIBL reduces with the L_g. DIBL is maximum at L_g = 30 nm 8.29 mV/V, Si (x = 0), and 10.62 mV/V, Ge (x = 1) at L_g = 30 nm. This gain in DIBL is a sign of improved electrical control and counteracts the influence of SCEs at longer channel lengths and higher Ge content.

The V_T also demonstrates a dependence on channel length and the Ge ratio. V_{TS} of Si (x = 0) and Ge (x = 1) are 0.48 V and 0.55 V, respectively, at L_g = 10 nm and 30

nm. The increase in V_T indicates that, for a given Ge fraction, the transistor becomes more stable at higher temperatures.

The carrier mobility is also sensitive to Ge content: higher Ge content leads to a lower effective carrier mass, thereby increasing mobility and electrostatic control. Nevertheless, the further increase in Ge levels makes it more susceptible to temperature changes. High drain biases can also reduce subthreshold performance due to IGIDL fluctuations. SS and DIBL are also sensitive to temperature variations in gadgets containing more Ge. The thermal effects are also complicated by the fact that epitaxial growth of $\text{Si}_{1-x}\text{Ge}_x$ layers requires precise control of temperature between 450°C and 700°C to prevent thermal-stress-related defects [167].

Therefore, the findings indicate that maximizing the Ge ratio and the channel length is necessary to achieve optimal performance in $\text{Si}_{1-x}\text{Ge}_x$ FinFETs. These aspects are crucial for optimizing performance, thermal stability, and electrostatic control, which are critical to high efficiency and stable operation at high temperatures. Table 4.2 demonstrates the influence of the Ge ratio on these key parameters across different channel lengths. It is observed that increasing the Ge content increases mobility and switching speed but, conversely, reduces SS and DIBL under thermal stress. Hence, it is paramount to choose the appropriate x ratio to achieve a thermally stable, electrically efficient FinFET design.

Table 4.2
Comparison of the research results.

$W_g = 10$	Si, $x = 0$			Si-Ge, $x = 0.25$			Si-Ge, $x = 0.50$			Si-Ge, $x = 0.75$			Ge, $x = 1$		
	SS	DIBL	V_T	SS	DIBL	V_T	SS	DIBL	V_T	SS	DIBL	V_T	SS	DIBL	V_T
$L_g = 10$	120.39	188.47	0.28	162.06	185.7	0.28	166.82	191.19	0.37	172.1	231.17	0.33	187.23	260.94	0.19
$L_g = 20$	89.67	34.71	0.46	92.68	20.22	0.49	93.65	25.1	0.56	94.73	32.89	0.55	95.87	38.57	0.49
$L_g = 30$	74.22	8.29	0.48	74.88	8.62	0.53	75.09	4.11	0.58	75.44	5.56	0.58	76.11	10.62	0.55

Note: Temperature range during simulations: 275 K to 350 K.

Figure 4.37 illustrates the dependence of SS on L_g of various fractions of Ge in $\text{Si}_{1-x}\text{Ge}_x$ alloys. The graph depicts the change in SS as L_g increases from 10 to 30 nm and the variation in x on the performance of FinFETs.

The data indicate that SS improves progressively with increasing Ge(x) ratio. The SS value of a channel with length $L_g = 20$ nm has an initial value of 89.67 mV/dec, and the recorder value of 74.22 mV/dec with $L_g = 30$ nm. At $x = 0.25$, the SS value at $L_g = 20$ nm = 92.68 mV/dec, but the SS value still decreases with increasing content of Ge as far as 74.88 mV/dec at $L_g = 30$ nm. At $x = 0.50$, the SS value is further enhanced to 75.09 mV/dec at $L_g = 30$ nm. The SS values of 75.44 mV/dec at $L_g = 30$ nm at $x = 0.75$ and 76.11 mV/dec at $L_g = 20$ nm at $x = 1$ (pure Ge).

This trend suggests that increasing Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ alloy improves FinFET subthreshold efficiency, particularly by reducing SS. The reduction of SS due to increased Ge content results in higher switching efficiency, which is very important for low-power applications. As the SS approaches the desired value of 60 mV/dec, the device becomes more effective in terms of switching speed and low-power performance.

Furthermore, the effect of Ge content on SS is not purely positive. It also depends on L_g . The impact of L_g on SS is more intense than that of Ge content. The SS also increases with L_g , underscoring the importance of channel length in FinFET performance. It has been scientifically proven that longer channel lengths offer better electrostatic control and minimise short-channel effects, resulting in a more stable SS. Thus, the trade-off between Ge content and channel length is critical for enhancing FinFET performance, especially in low-power operation.

Regarding thermal effects, elevated temperatures (275 to 350 K) increase SS's sensitivity dramatically with increasing Ge ratios ($x = 1$). This Ge effect on the thermal behaviour of the devices is captured in the increase in SS, with higher Ge content reducing the effective mass of the charge carriers, making them more mobile and thus increasing their electrostatic control. Nevertheless, the increased Ge concentration also increases the device's sensitivity to thermal variations, thereby increasing IGIDL. This thermal sensitivity leads to performance degradation in the subthreshold regime, particularly at high drain biases.

Therefore, the findings affirm that augmenting the Ge quantity enhances SS and overall electrical performance. This, however, comes with a trade-off, since an increase in Ge concentration increases the devices' susceptibility to thermal stress. Ensuring that

the Ge ratio and channel length are tightly controlled is essential to achieve optimal performance in FinFETs, especially in high-temperature environments. These results align with previous work that emphasized the need to adjust the Ge ratio to balance thermal stability and electrical efficiency in FinFET designs.

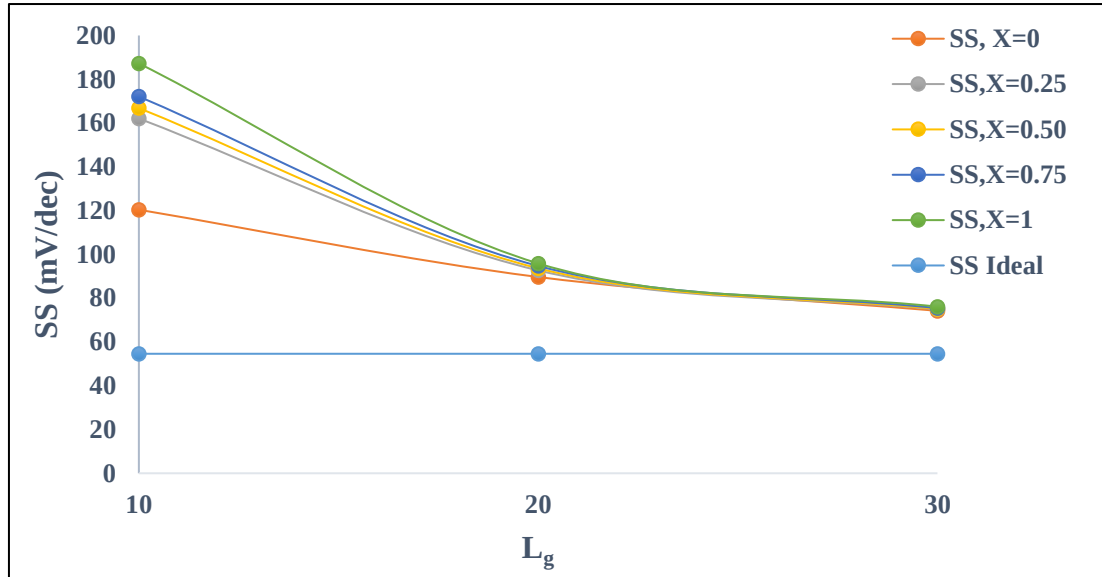


Figure 4.37 Effect of (x) on SS versus Gate and Length (L_g).

The influence of the Ge fraction (x) in the $\text{Si}_{1-x}\text{Ge}_x$ element on DIBL at various L_g is illustrated in Figure 4.38, comparing the x value ($x = 0, 1$) of the element as a factor of L_g . The graph indicates a clear trend in DIBL with changes in Ge content and channel length.

The evidence indicates that a higher Ge ratio is associated with higher DIBL values. Nevertheless, as the Ge ratio increases with channel length, DIBL decreases. This trend is well depicted in the figure. At $x = 0$ and $L_g = 10$ nm, the DIBL is 188.47 mV/V, and at $L_g = 20$ nm, it is 34.71 mV/V, indicating greater electrostatic control with longer channel length. This trend is also observed, and the DIBL at $x = 0.25$ decreases from 185.7 mV/V at $L_g = 10$ nm to 20.22 mV/V at $L_g = 20$ nm.

In the case of $x = 0.5$, DIBL = 191.19 mV/V at $L_g = 10$ nm and = 25.1 mV/V at $L_g = 10$ nm. At even higher contents of Ge at $x = 0.75$, DIBL begins at 231.17 mV/V when $L_g = 10$ nm and at 32.89 mV/V when $L_g = 20$ nm. Lastly, DIBL has a net starting value of 260.94 mV/V at $x = 1$ with $L_g = 10$ nm, and a maximum decrease in DIBL of

38.57 mV/V at $L_g = 20$ nm. This trend demonstrates that the greater the Ge content, the better the electrostatic control and the lower the SCEs.

The channel length plays a significant role in DIBL behaviour. The DIBL value also decreases with L_g . Thus, longer channels allow the gate to maintain greater control over the device's electrostatics, thereby reducing the DIBL effect. This reflects enhanced channel control and reduced short-channel effects with increased channel length.

Temperature is also very important in DIBL values. All Ge fractions demonstrate an increase in DIBL with increasing temperature from 275 to 350 K. This increase is most pronounced in devices with higher Ge content, as Ge enhances carrier mobility while increasing sensitivity to temperature variations, thereby raising DIBL. This has been ascribed to Ge having even greater carrier mobility, accompanied by increased sensitivity to thermal changes, leading to higher IGIDL and additional SCEs, particularly at elevated drain biases.

In summary, the graph depicts that a higher Ge fraction in $\text{Si}_{1-x}\text{Ge}_x$ alloys leads to better DIBL performance at longer channel lengths, though it is also more sensitive to temperature changes. These results reflect that the trade-off between mobility and thermal stability is important, and it is essential to optimize the Ge content and channel length to achieve optimal performance in FinFET devices, particularly at high temperatures.

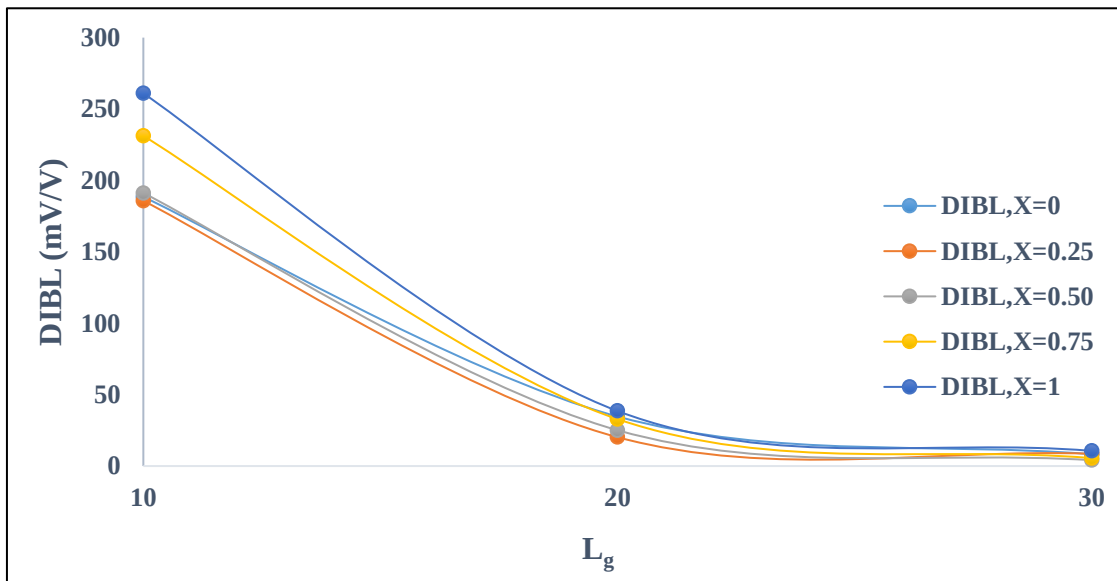


Figure 4.38 Effect of (x) on (DIBL) and (L_g).

Figure 4.39 presents how, with different concentrations of Ge (y) in $\text{Si}_{1-x}\text{Ge}_x$ alloys (where x is the concentration of Ge), the V_T varies with the concentrations of the L_g , and vice versa. The graph displays how V_T varies with increasing L_g (10-30 nm) and the variations in each Ge ratio.

Based on Figure 4.39, the Ge ratio increases with increasing V_T . Moreover, V_T varies with channel length. Additionally, V_T is 0.28 V at $L_g = 10$ nm and 0.48 V at $L_g = 30$ nm. V_T begins at 0.28 V at $x = 0.25$ and rises to 0.53 V at $L_g = 10$ nm, which then rises to 0.53 V at $L_g = 30$ nm. V_T exhibits a slight rise at $x = 0.50$ with starting values of 0.37 V at $L_g = 10$ nm and 0.58 V at $L_g = 30$ nm. For $x = 0.75$, V_T is 0.33 V at $L_g = 10$ nm and increases to 0.58 V at $L_g = 30$ nm. Lastly, at $x = 1$, V_T started at $V = 0.19$ V at $L_g = 10$ nm, and increased tremendously to $V = 0.55$ V at $L_g = 30$ nm.

These trends reveal that the higher the Ge content, the earlier the first drop, followed by an upward trend in V_T . At large values of L_g , these variations are more pronounced. The behaviour is explained by Ge's lower carrier effective mass, which increases carrier mobility and reduces the potential barrier, thereby changing V_T . This reduction and subsequent rise in V_T can improve the device's switching speed, despite this feature perhaps increasing leakage currents and SCEs, since higher Ge ratios also enhance sensitivity to temperature variations.

Figure 4.39 also suggests that, for $\text{Si}_{1-x}\text{Ge}_x$ FinFET devices in use, L_g is extremely sensitive to V_T with increasing Ge content (x). The influence is even more drastic with a higher Ge ratio. This is where the significance of optimizing both Ge ratio and channel length lies: to trade off switching speed and power consumption, while minimizing leakage currents and short-channel interactions.

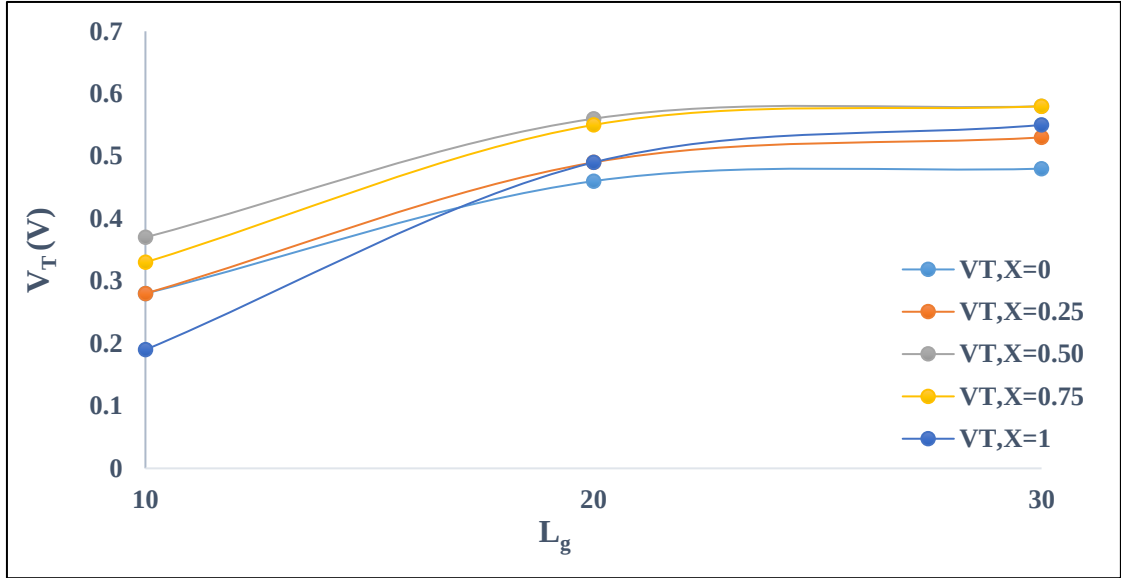


Figure 4.39 Effect of (x) on (V_T) and (L_g).

The observed V_T behaviour across different Ge mole fractions can be compared with recent experimental and modelling studies of Si-Ge-channel FinFETs, with a view to making a more in-depth comparison with past published work. For example, [168] demonstrated that the narrowing of the bandgap and the lowering of the effective mass were caused by increasing Ge content in $\text{Si}_{1-x}\text{Ge}_x$ channels and, consequently, decreased V_T first due to improved carrier transport. However, at higher Ge concentrations ($x \geq 0.4$ – 0.6), quantum confinement and strain-induced band-structure modification were observed to stabilize V_T or slightly increase it. Their values of V_T were measured at 0.30 to 0.55 V in the case of $L_g = 20$ – 30 nm, as compared to the V_T window (0.28–0.58 V) used in the present work.

Other researchers also confirmed that sub-20 nm Si-Ge FinFETs have superior mobility and greater electrostatic susceptibility, with V_T roll-off increasing more at $x = 0.7$ and above due to lower gate control efficiency [169]. Their findings indicated that V_T degradation is nonlinear at $L_g = 10$ and 15 nm as the Ge fraction was increased, which agrees with the fluctuation pattern observed in the current results.

Considering more recent studies, [170] have claimed that near $x = 0.5$, when the trade-offs between performance and mobility gain are maximized, and the electrostatic degradation is still manageable. They offered to underscore that adding too much Ge ($x > 0.7$) dramatically increases DIBL and temperature sensitivity due to increased intrinsic carrier concentration and dielectric screening loss. This is very much in line

with the current results, where $\text{Si}_{0.5}\text{Ge}_{0.5}$ has the least fluctuating V_T due to L_g fluctuations, and higher Ge ratios exhibit greater electrostatic instability.

Importantly, channel length, Ge fraction, and temperature-dependent behaviour are accounted for and combined in a single analysis, whereas past research typically considers one variable at a time, either geometry scaling or material composition. This coupling of two variables indicates that, at medium Ge ratios ($x = 0.5$), voltage stabilization is a balance point at which the mobility enhancement does not yet dominate electrostatic confinement. Thus, the value of this work lies in quantitatively determining the stability range within which material-based performance gains do not compromise the integrity of short-channel devices.

When Table 4.2 and, 4.38, and 4.39 are thoroughly examined, it is clearly revealed that the $\text{Si}_{0.5}\text{Ge}_{0.5}$ composition ($x = 0.50$) provides the most even performance within the entire range of the experimented gate lengths. This ratio consistently yields good results, with good values at $L_g = 20$ and 30 nm, where DIBL is also low. The SS values have been observed to fall within an acceptable range, and the V_T values do not change with temperature. For example, the DIBL value at $x = 0.50$ and $L_g = 20$ nm is 32.89 mV/V, and 25.1 mV/V at $L_g = 30$ nm, indicating good control of short-channel effects.

Although pure Si ($x = 0$) is somewhat better at a minimum channel length ($L_g = 20$ nm) with a DIBL of 34.71 mV/V, supreme lack of electrostatic control is evident at higher levels of Ge content, particularly at $x = 0.75$ and $x = 1$, where the DIBL values are 231.17 and 260.94 mV/V, respectively, as illustrated in Figure 4.38. This underscores the fact that an increase in the Ge ratio increases mobility and increases the device's vulnerability to thermal and short-channel effects, as seen in the SS and DIBL behaviour in Figure 4.37 and 4.38.

There is a clear correlation between V_T and the Ge ratio, with $\text{Si}_{0.5}\text{Ge}_{0.5}$ as the most stable V_T value. V_T of $\text{Si}_{0.5}\text{Ge}_{0.5}$ at $L_g = 10$ nm is 0.56 V, and 0.52 V at $L_g = 30$ nm provides more stable device operation across differing temperature conditions than pure Si or Ge. As Figure 4.39 also reveals, V_T rises slightly with increasing Ge content, e.g., at $x = 0$, $V_T = 0.48$ V, and at $x = 1$, $V_T = 0.55$ V when $L_g = 30$ nm, which offers superior switching properties at low voltages.

Past research mostly explored either geometry scaling or material engineering alone [166]. Recent announcements attest to improvements in carrier transport through the addition of Si-Ge, nevertheless raising electrostatic sensitivity at scaled nodes [165].

Such investigations, however, are usually conducted under constant thermal or compositional conditions when measuring performance. Conversely, the current study combines channel length scaling, Ge mole fraction, and temperature-dependent behaviour using a single overriding model, which allows the quantitative determination of a stability window ($x = 0.50$, $L_g = 20, 30$ nm).

In addition, V_T roll-off and DIBL amplification at levels below 20 nm have been extensively reported [166-165]. However, the current study explicitly maps the multi-parameter trade-off boundary between mobility enhancement and electrostatic degradation. With this combination view, the detailed contribution to the strain-modified fin-structure variability and scaling-length-controlled electrostatics of FinFETs in Si-Ge is developed in addition to the existing parameters analysis.

These results demonstrate that achieving the best FinFET performance is not possible with high-mobility materials alone. Ge-rich channels enhance carrier transport, but at the expense of increased thermal sensitivity and sensitivity to short-channel effects. Hence, a balanced trend in design that considers both machine design and material structure is necessary. The $\text{Si}_{0.5}\text{Ge}_{0.5}$ structure is a viable option, with superior carrier mobility, thermal stability, and short-channel controllability. This underscores the need to align material properties with physical measurements to improve FinFET operation at the nanoscale.

These findings clarify the significance of optimizing the Ge ratio and channel length to achieve maximum thermal and electrostatic control, particularly at high operating temperatures. This optimization approach aligns with the objectives of state-of-the-art semiconductor design.

CHAPTER 5

CONCLUSION

5.1 Introduction

This chapter concludes with the key findings and a description of possible future research paths. This research aimed to examine how L_g at three different values (10, 20, and 30 nm) affects the electrical properties of FinFET devices. Analysis was performed with a constant W_g of 10 nm and T_{ox} of 1 nm. The impact of temperature change was also considered, and an investigation of alternative ($Si_{1-x}Ge_x$) alloy compositions as the active channel material was conducted. The MuGFET simulator was used to run simulations, revealing that channel length, material composition, and operating temperature play significant roles in determining device performance, particularly drive current, leakage behaviour, and threshold control. The results can be useful in the design of FinFETs, where it is essential to carefully balance the physical sizes, material choices, and thermal conditions of next-generation semiconductor devices to achieve optimal performance.

5.2 Conclusion

This study has thoroughly discussed the characterization and modelling of $Si_{1-x}Ge_x$ FinFET structures. It emphasizes the influence of the compositional ratio (x), geometric dimensions, and operating temperature on the electrical and thermal behaviour of the nanoscale devices. The research study was designed to fulfill three main purposes, two of which were appropriately addressed.

Objective 1 was to examine the impact of working temperature on the FinFET channel in terms of V_T , SS, and DIBL with Si, Ge, and $Si_{1-x}Ge_x$ as semiconductors. This has been conducted by simulations in the temperature range of 275 K to 350 K. The findings verified that elevated temperature tended to reduce SS and DIBL values, with Ge-rich devices being more susceptible to temperature changes due to their lower thermal conductivity. Notably, the $Si_{0.5}Ge_{0.5}$ composition had a stable SS (approximately 75 mV/dec) and low DIBL (approximately 25 mV/V) even at high

temperatures, confirming its better thermal stability (as per Table 4.2). This is explained by the fact that carrier mobility increases with Ge incorporation, while electrostatic control is maintained by the Si fraction.

Objective 2 aimed to optimize and minimise FinFET channel dimensions, with V_T , SS, and DIBL as limiting factors. Three L_g values (10, 20, and 30 nm) were investigated, with the channel width held constant at 10 nm and the oxide thickness held constant at 1 nm. The results indicated that the 20 and 30 nm channel lengths provided optimal performance for the $\text{Si}_{0.5}\text{Ge}_{0.5}$ ($x = 0.5$) setup, with a SS of less than 75 mV/dec, a DIBL of less than 25 mV/V, and V_T kept within the target range (0.37 V to 0.58 V). The findings indicate that moderate channel lengths are effective in suppressing short channel effects and also in providing high switching performance. As an alternative, $\text{Si}_{0.25}\text{Ge}_{0.75}$ ($x = 0.75$) also offered competitive performance especially a stable threshold voltage (0.55, 0.58 V) and low DIBL (5.56, 32.89 mV/V), respectively at $L_g = 20, 30$ nm which makes it a viable option when slightly higher Ge content is required to enhance mobility. Its marginally larger SS values, however, highlight a trade-off in switching sharpness with the $x = 0.50$ composition.

Objective 3 was to develop a FinFET using Si, Ge, or $\text{Si}_{1-x}\text{Ge}_x$ as the semiconductor material to achieve the best electrical and thermal properties. The findings made $\text{Si}_{0.5}\text{Ge}_{0.5}$ the most relevant composition, which, especially at L_g of 20 and 30 nm, exhibited the best thermal stability, low leakage, and good electrostatic control. Although pure Si revealed good performance in short channels at 10 nm, it had poorer thermal stability. The selected composition leverages the benefits of Ge carrier mobility while retaining the strength of Si, making it an attractive choice for high-performance, thermostable nanoscale applications.

In general, this work establishes that, by optimizing the compositional ratio (x) and the device geometry, without considering the 1 nm channel thickness and the 1 nm oxide thickness. FinFETs using $\text{Si}_{1-x}\text{Ge}_x$ can achieve higher performance and reliability.

The streamlined $\text{Si}_{0.5}\text{Ge}_{0.5}$ FinFET architecture identified in the present study has significant implications for advanced CMOS nodes. The established compromise, guided by thermal stability and electrostatic control, between $L_g = 20\text{-}30$ nm aligns with current sub-30 nm industry fabrication interests. Leakage suppression and power efficiency are the key uniformity requirements.

The enhanced SS and lower DIBL in a high-temperature environment indicate strong applicability to low-power logic controllers, high-density integrated systems, and

chip architectures with thermal constraints. Furthermore, the temperature-sensitivity trends, specifically the predictability of V_T shift and SS variation with temperature changes, indicate the possible use of $\text{Si}_{1-x}\text{Ge}_x$ FinFET designs in nanoscale temperature sensors and on-chip thermal devices. These features are highly valued in current-day thermal control for high-end processors and 3D integrated circuits, where localized hotspots can be observed to ensure reliability and extended lifespan.

The results provide valuable insights for the design of next-generation FinFET devices, enabling improved electrostatic control, reduced short-channel effects, and enhanced thermal management in advanced semiconductor technologies.

5.3 Recommendations for Future Work

This work demonstrated how the length of the channel and the material used to fabricate it could influence the performance of $\text{Si}_{1-x}\text{Ge}_x$ FinFETs, though much remains to be uncovered and to be continually gnarled:

- 1- Ge Content optimization: Future experiments can consider larger intervals of germanium content (x) to adjust the equilibrium between carrier mobility, leakage reduction, and thermal resistance, particularly in more demanding scaling situations.
- 2- Adoption of High-k Dielectrics: The adoption of high-k dielectrics in the gate is expected to improve electrostatic control and reduce gate leakage, especially in ultra-short-channel devices.
- 3- Strain - Engineering Investigations: Systematic investigations of the strain effects induced by different Si-Ge alloy compositions may reveal further improvements in carrier transport and sub-threshold performance.
- 4- Process Variability and Reliability Analysis: Modelling the effects of fabrication-induced variability, aging, and thermal cycling would help create a more robust and manufacturable FinFET design.
- 5- Exploration of 3D Architectures: Future research should consider more recent 3D device architectures, such as Gate-All-Around (GAA) and nanosheet FETs with Si-Ge channels. Studying these can provide ideas for scaling devices in the future.
- 6- Circuit-Level Implementation: The integration of optimized Si-Ge-FinFET designs into circuit-level frameworks, coupled with a systematic analysis of key metrics, i.e., power consumption, Propagation Delay, and Area (PDA), is implemented as a

way to narrow the gap between device-level modelling and real practical applications at the system level.

These future directions may help further understand the Si-Ge-based FinFET design and make a meaningful contribution to the development of next-generation low-power, high-performance semiconductor technologies.

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APPENDICES

APPENDIX 1

Design 2 (X = 0)

		300	325	350
	0	4.23E-11	6.73E-11	9.62E-11
	0.1	4.63E-07	7.47E-07	1.11E-06
	0.2	4.04E-06	5.11E-06	6.16E-06
	0.3	1.45E-05	1.53E-05	1.60E-05
delta I	0.4	2.57E-05	2.53E-05	2.49E-05
	0.5	3.56E-05	3.39E-05	3.23E-05
	0.6	3.95E-05	3.72E-05	3.51E-05
	0.7	3.87E-05	3.60E-05	3.35E-05
	0.8	3.34E-05	2.99E-05	2.67E-05
	0.9	1.56E-05	1.23E-05	9.76E-06
	1	3.16E-06	2.46E-06	1.93E-06

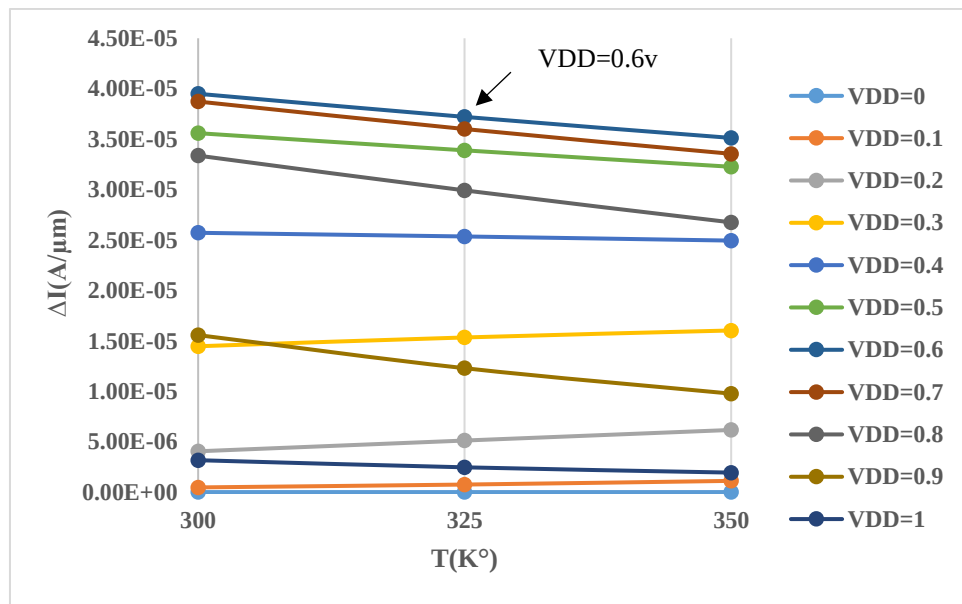


Figure 1: ΔI -T FINFET characteristics ($L_g = 10$ nm).

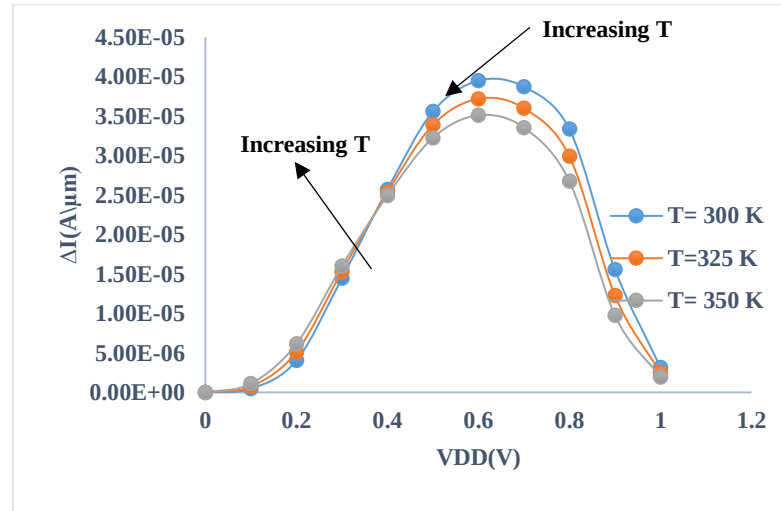


Figure 2: Characteristics of ΔI with V_{DD} at ($L_g = 10$ nm).

	L_g	300
	10	3.95
0.6	20	3.63
	30	2.41

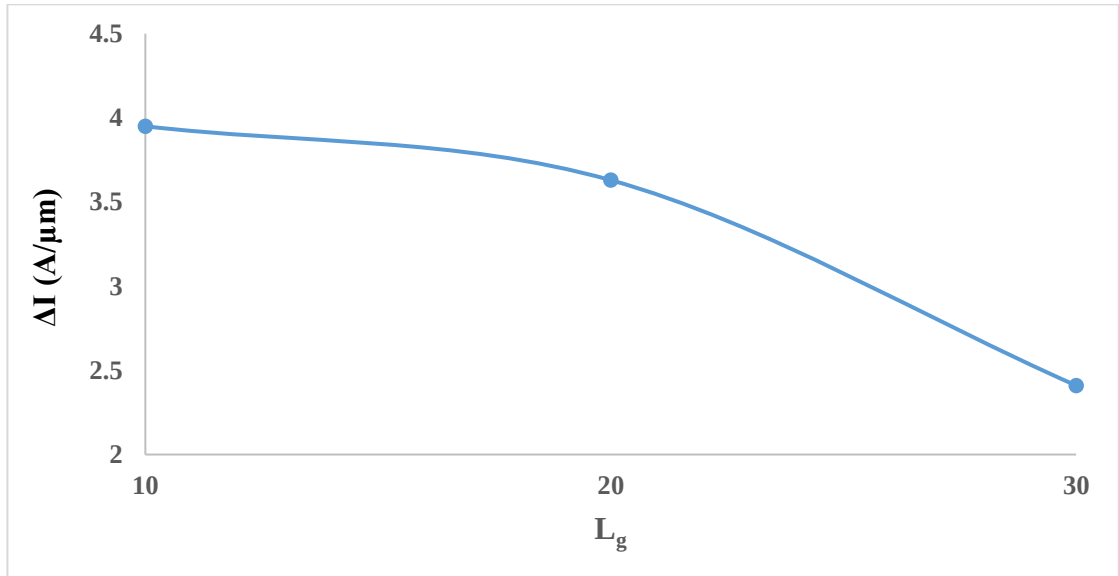


Figure 3: Characteristics of ΔI with L_g .

Design 2 (X = 1)

	Ge	Lg	300
		10	1.88
When	$V_{DD}=0.9\text{ v}$	20	3
		30	2.99

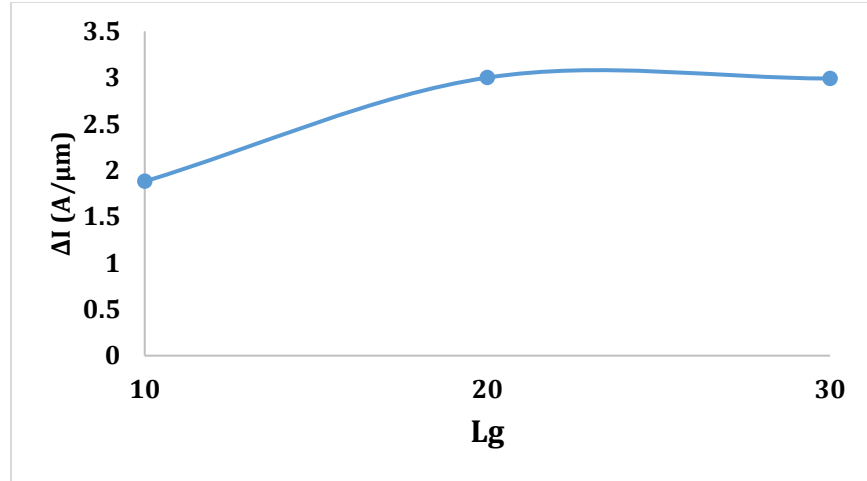


Figure 4: Characteristics of ΔI with L_g .

					W=10 L=10				
				V_{DD}		275	300	325	350
			V_T	1		0.192552	0.218221	0.196456	0.178619
L=10nm			SS	1		187.2359	197.5877	198.3957	217.4937
			DIBL	1		260.9469	268.8781	270.807	230.3632
			PFT SS	1		54.6	59.5	64.5	69.5

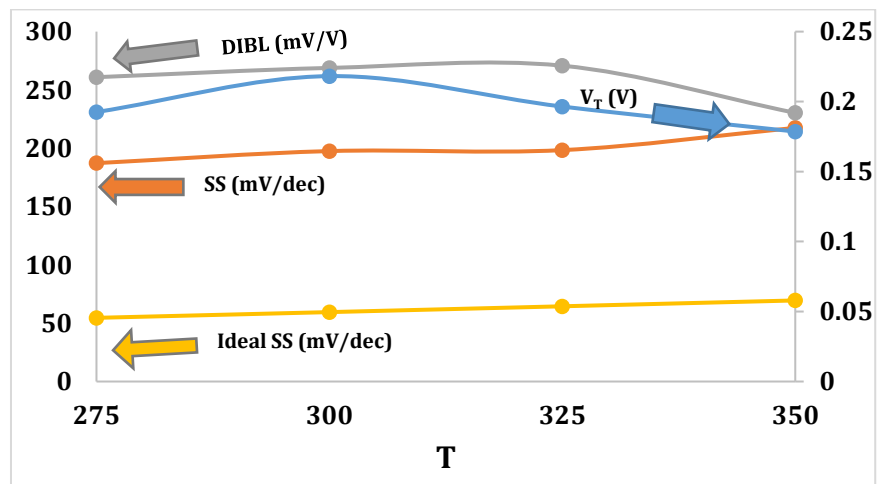


Figure 5: V_T , SS, and DIBL at $L_g = 10\text{ nm}$

		V_{DD}	10	20	30
	V_T	1	0.218221	0.487315	0.539401
$T=300$	SS	1	197.5877	104.942	83.70425
	DIBL	1	256.8564	32.84188	12.40159

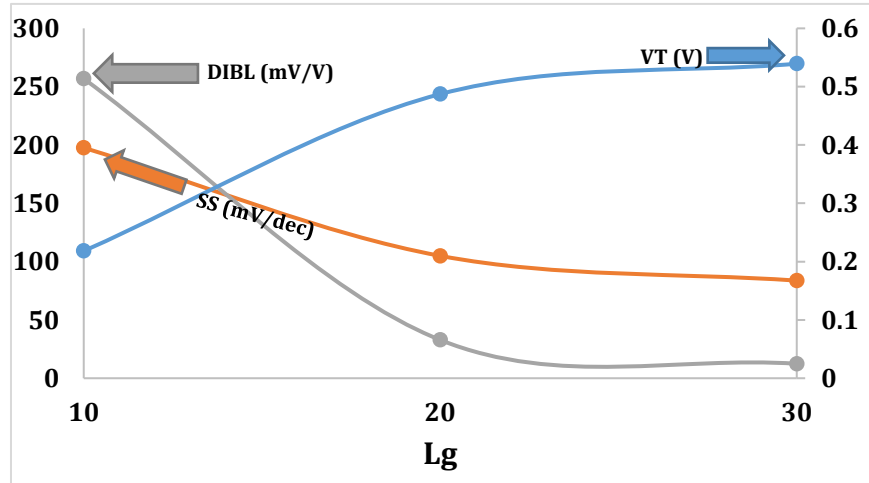


Figure 6: V_T , SS, and DIBL with L_g .

Design 2 ($X = 0.25$)

		300
	10	1.46
$x=0.25$	20	1.48
	30	1.53

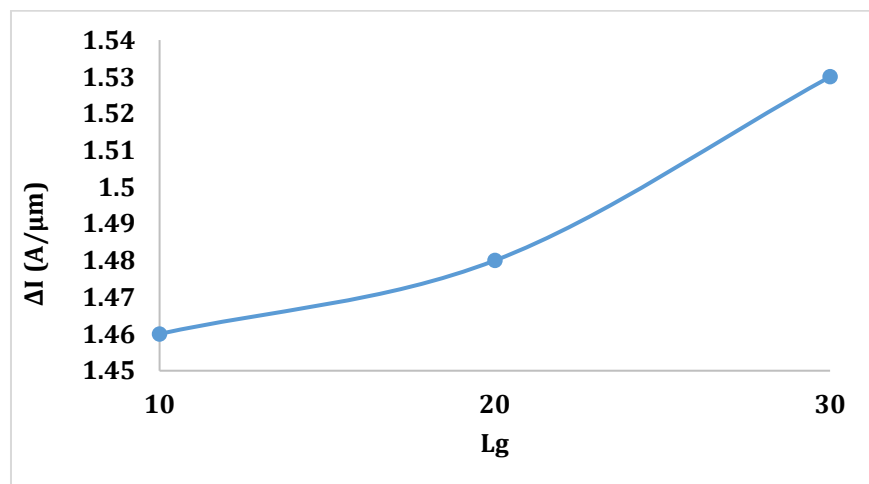


Figure 7: Characteristics of ΔI with L_g .

				W10 L10			
				275	300	325	350
L10		VT	1	0.370829	0.351253	0.331725	0.312197
X=0.5		SS	1	166.8284	185.7828	205.1211	224.7552
		DIBL	1	191.1949	199.7636	207.6391	214.9692
		PFT SS	1	54.6	59.5	64.5	69.5

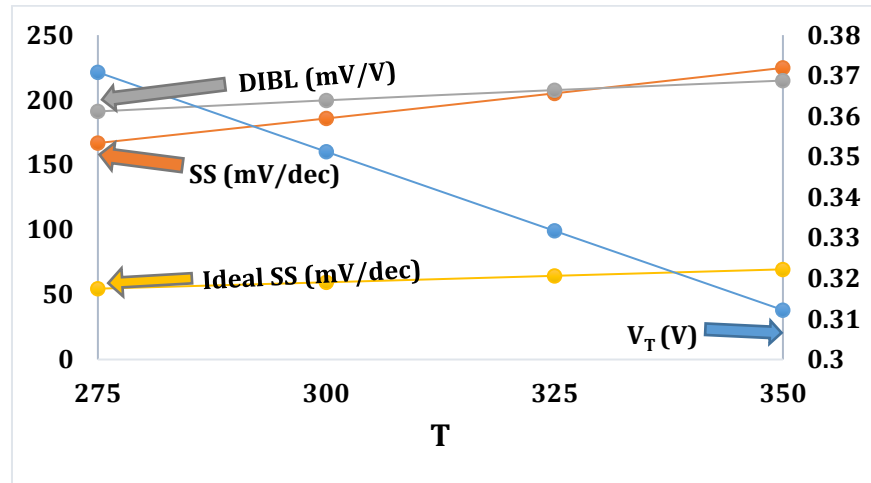


Figure 8: VT, SS, and DIBL at Lg = 10 nm

			10	20	30
		VT	0.351253	0.550691	0.580508
T=300		SS	185.7828	102.5459	82.28981
		DIBL	199.7636	28.98446	5.570801

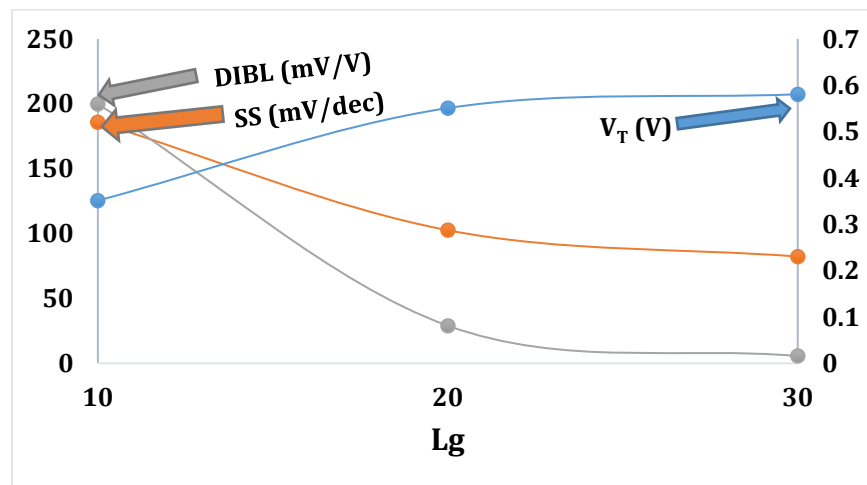


Figure 9: VT, SS, and DIBL with Lg.

Design 2 (X = 0.5)

		300
x=0.5	10	1.46
	20	1.48
	30	1.53

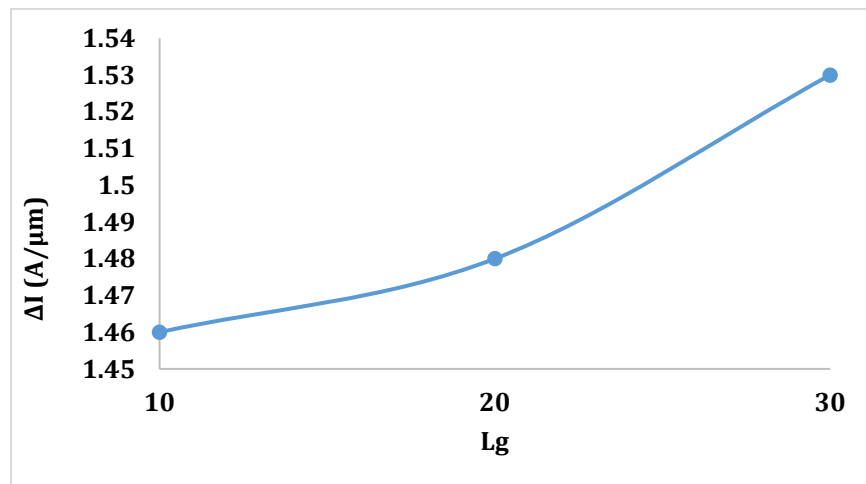


Figure 10: Characteristics of ΔI with L_g .

			10	20	30
		VT	0.351253	0.550691	0.580508
T=300		SS	185.7828	102.5459	82.28981
		DIBL	199.7636	28.98446	5.570801

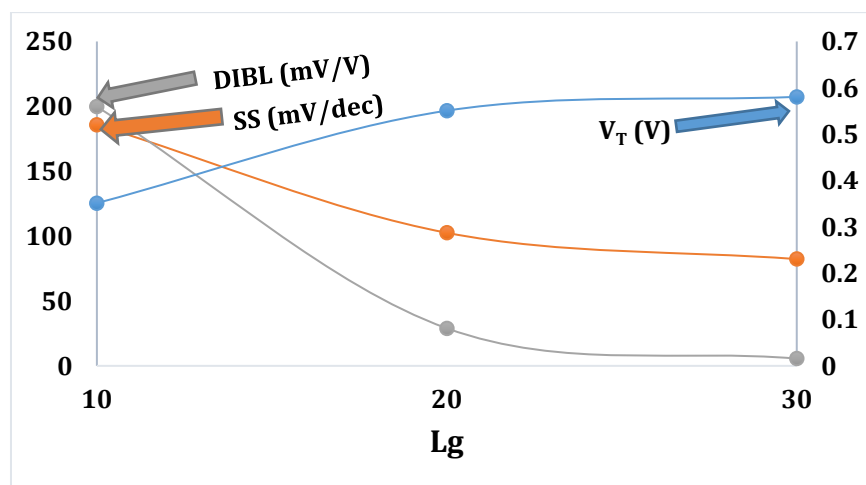


Figure 11: V_T , SS, and DIBL with L_g .

Design 5 (X = 0.75)

		300
	10	1.77
x=0.75	20	1.79
	30	1.86

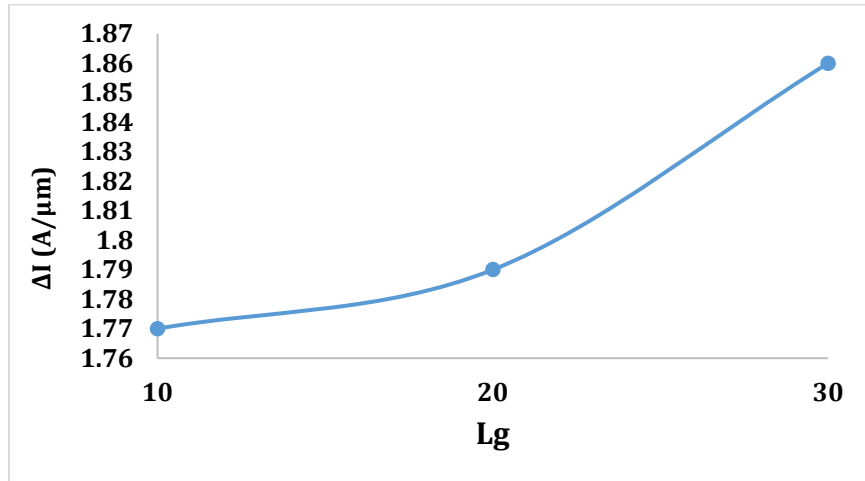


Figure 12: Characteristics of ΔI with L_g .

		10	20	30
T=300	VT(V)	0.309509	0.534097	0.571995
	SS(mV/dec)	191.5074	103.6905	82.60009
	DIBL(mV/V)	240.4086	37.34707	7.146033
	SS Ideal(mV/dec)	59.5	59.5	59.5

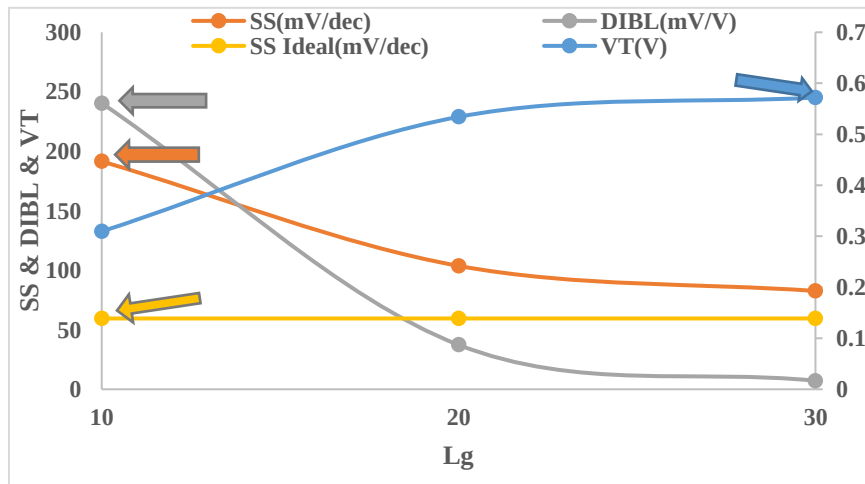


Figure 13: VT, SS, and DIBL with L_g .

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LIST OF PUBLICATIONS:

- Atalla, Y., Mamat, M. H., & Hasyim, Y. (2025). Characterization of Si_{0.25}Ge_{0.75}-FinFET as a Temperature Nano Sensor. *Journal of Electronics, Electromedical Engineering, and Medical Informatics*, 7(2), 422-430, DOI: <https://doi.org/10.35882/jeeemi.v7i2.695>
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