A Single Phase Matrix Converter Operating as a Rectifier Driving Constant Power Load.

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Abstract :- This paper presents the study of a Single Phase Matrix Converter (SPMC) operated as an AC-DC controlled rectifier driving the linear and non-linear load (Constant Power Load). The multiple Pulse Width Modulation (PWM) technique are used as its switching operation for synthesizing the output modeling. The analysis of constant power load were conducted in detailed before being compliment in the SPMC system. In this work a simple commutation strategy for implementation in single phase matrix converter provides the required free-wheeling operation similar to those available in other converter topologies is proposed. The commutation strategy used in this work has also shown reduction in spikes, a common phenomenon in matrix converter topologies. The commutation scheme establish a current path for energy to flow during dead-time, the avoiding the generation of voltage spikes. The simulations has been done by using MATLab/Simulink software to validate the design approach of SPMC. Results from the simulation are presented to express the concept.

Keywords : Single Phase Matrix Converter (SPMC), Insulated Gate Bipolar Transistor (IGBT), Constant Power Load (CPL), MATLAB Simulink (MLS).

1. Introduction

Power electronic devices are playing an important role in order to convert electrical energy from one form to another form. Power electronics circuit containing semiconductor devices as switches, thereby controlling the current or voltage. Power electronics circuit is able to convert electrical energy from milliwatts to hundreds of megawatts. The latest invention by using the power electronics devices is an advanced topology named Matrix Converter (MC). The MC circuit topology was first proposed by Gyugyi [1] in 1976 and offers many advantages such as the ability to regenerate energy back to the utility, sinusoidal input and output current and controllable input current displacement factor [2]. Besides, it has the potential of affording an "all silicon" solution for AC-AC conversion, removing the need for reactive energy storage components used in conventional rectifier-inverter based system. Obviously published studies mainly dealt with three-phase circuit topologies [3-5]. The Single-phase matrix converter (SPMC) was first realized by Zuckerberger [6]. Switching strategy for the four quadrant switches is the most important things of matrix

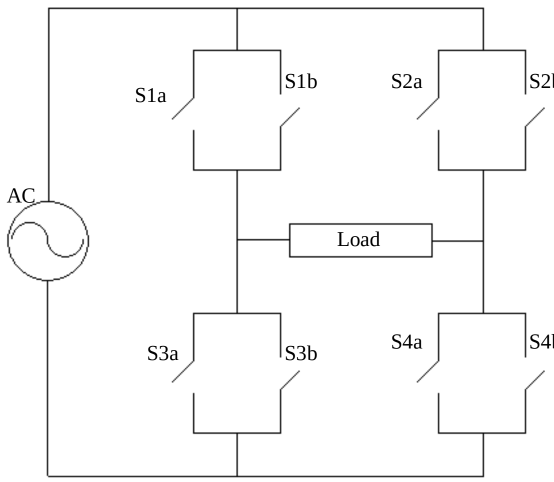

Figure 1: Single Phase Matrix Converter Topology.

converter since it will result in the input source being converted to the desired output through matrix convertion. PWM was used as the switching technique for the four-quadrant switches. Applying the switching strategy and switching technique will produce the desired output that is synthesized from the input source of the matrix converter. There are four types of matrix converter, which relates to the type of power conversion; DC-AC, AC-DC, DC-DC and AC-AC. Since matrix converter was originally introduced, it has received considerable attention because it offers many advantages as described above. The size of the converter is also reduced since there are no large reactive components for energy storage [7].

2. Single Phase Matrix Converter (SPMC)

Basically, SPMC requires 4 bi-directional switches as shown in Figure 1 which capable of blocking voltage and conducting current in both directions. The input source of a SPMC circuit can be either a DC or single-phase AC. The output also can be either AC or DC. It's depends on the switching strategy and control strategy that will be implemented.

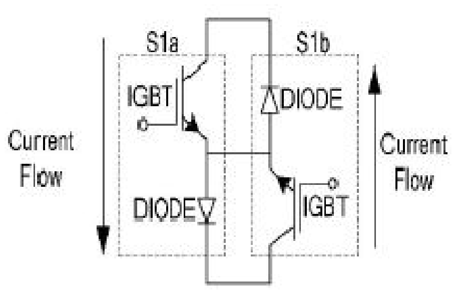

Figure 2: Bi-directional switch.

All the four switching strategies of an SPMC are shown in Figure 3 to Figure 6.

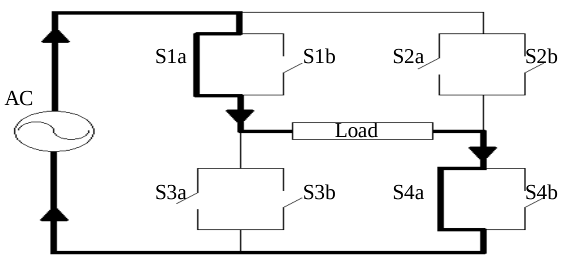

Figure 3: State 1 -Positive Cycle.

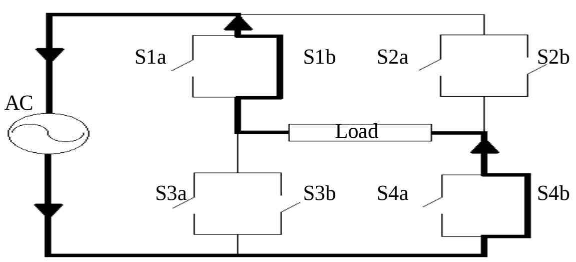

Figure 4: State 2 - Negative Cycle.

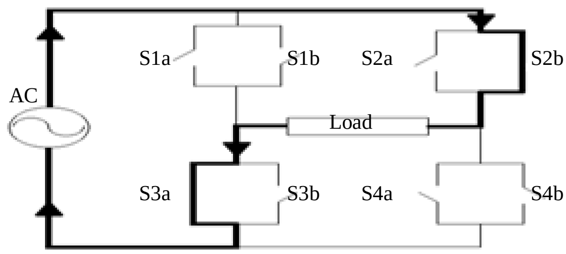

Figure 5: State 3 – Positive Cycle.

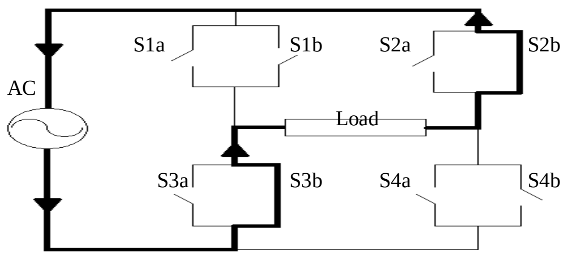

Figure 6: State 4 - Negative Cycle.

3. Controlled Rectifier

A rectifier is an electrical device which is used to convert AC input to DC ouput. The normal design of a rectifier uses a diode bridge and also known as uncontrolled rectifier. The SPMC topology can be used to design controlled rectifier. To design the controlled rectifier, the switching strategy must be identified for positive cycle and also negative cycle. To use the SPMC as a rectifier, the combination of State 1 and State 4 or State 2 and State 3 (in the previous topic) are used.

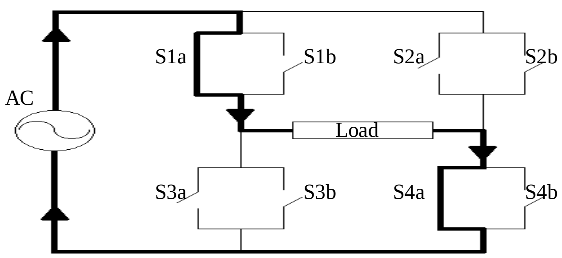

Figure 7: Switching Strategy for Positive Cycle.

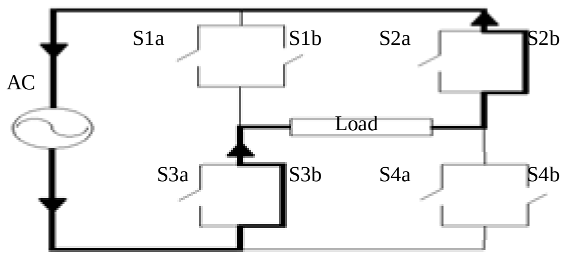

Figure 8: Switching Strategy for Negative Cycle.

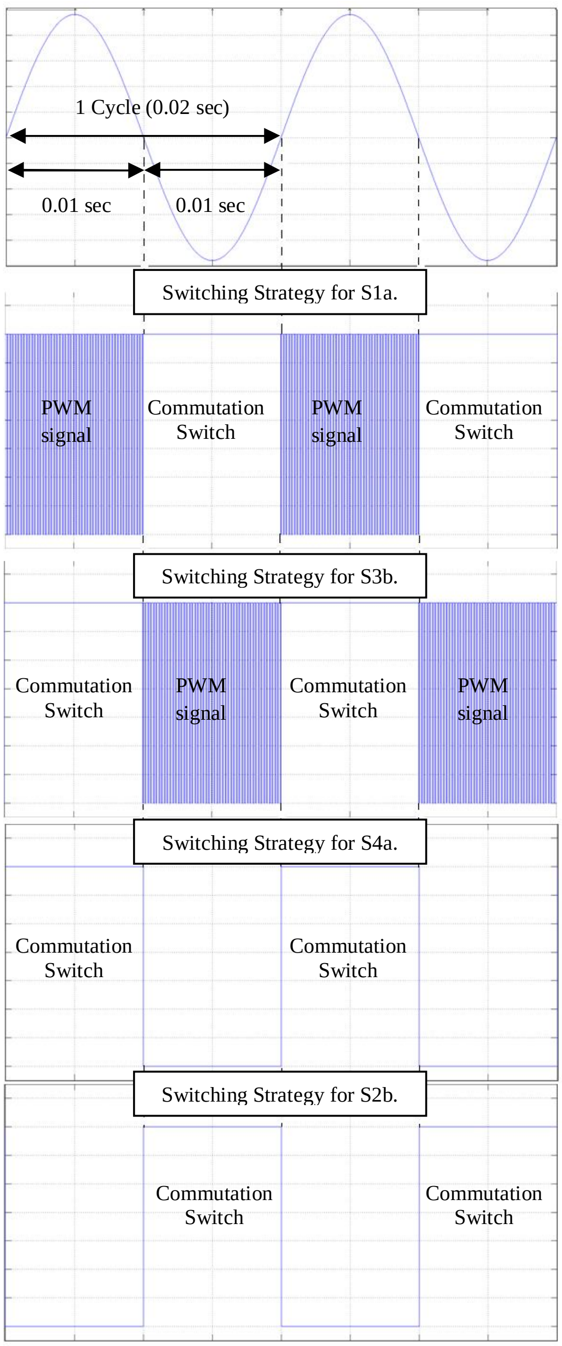

Figure 9: Switching Strategy.

Table 1: Switching Strategy.

	PWM Switch	*Commutation Switch*
Positive Cycle	S1a	S3b & S4a
Negative Cycle	S3b	S1a & S2b

One of the problems associated with using of matrix converter topology is that spikes generated during switch transitions when supplying RL loads; limiting the use in industry applications [8]. To avoid this problem, safe commutation was developed to prevent from current and voltage spikes induced by manipulating the switch according to the Table 1.

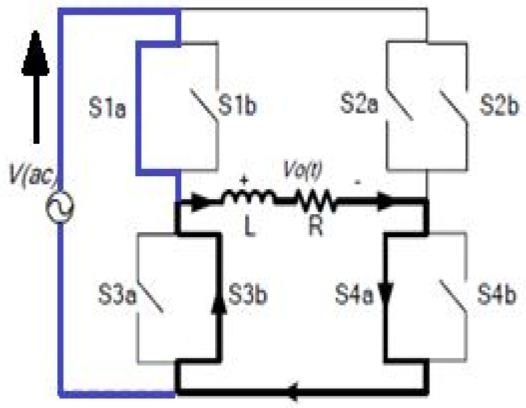

Figure 10: Commutation Switching for Positive Cycle.

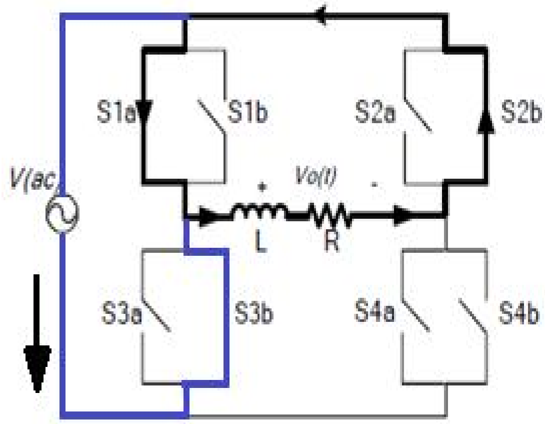

Figure 11: Commutation Switching for Negative Cycle.

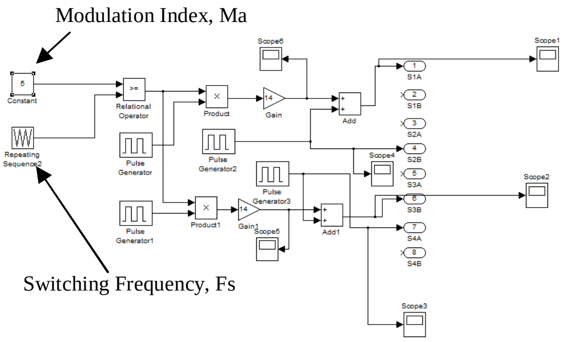

Figure 12: PWM Pulse Controller for Switching Strategy.

4. Constant Power Load (CPL)

In general, there are two kinds of loads in power systems. One group is conventional loads, which have positive incremental impedance characteristics. The other group is constant power loads (CPLs) sinking constant power from their input and having negative incremental impedance characteristics [9]. This is a destabilizing effect for the power electronic converters interfacing CPLs and is known as negative impedance instability. The calculation of negative input resistance is as follows. It is known that the input power and output power of a CPL are equal.

$$Pin = Po = P = v.i \qquad (1)$$

And

$$v = pi\text{-}1 \qquad (2)$$

Differentiating the voltage with respect to the current yields.

$$dv\ di = -i-2P = -\ P\ i2 = -\ v2\ P = -RL \quad (3)$$

Equation (3) shows the general equation to calculate the small-signal input resistance of a constant power load. The resistance is negative as expected and is also non-linear, depending upon the current and voltage.

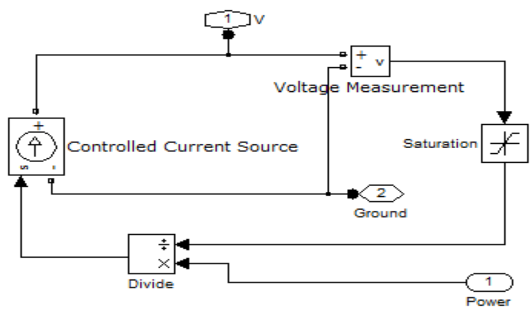

Figure 13: A block diagram of a CPL.

A CPL simulink block diagram is shown in Figure 13. The block diagram consist of controlled current source(CCS), voltage measurement, saturation block, and a function block to perform a mathematical calculation. The voltage port "V" and ground "gnd" will be connected to the DC source. The CPL power port, P, is an input signal which define the load power. The voltage signal saturation block is use to avoid the problem of a divide by-zero error when the voltages measurement approaches value near zero, the saturation level are set at 0.01 and infinity. The operation of the CPL is, firstly, the DC voltage is measured by the voltage measurement block. This voltage measurement signal is then passed through the saturation block. The result will enter the function block. The second signal is the CPL power. Both data will be calculate in function block, in which the division of the signal is performed to generated the current signal, which represents the characteristic of CPL.

5. Result and Discussion

The simulation of this project has been done by using MLS. To produce the DC output, LC filter is needed at the output site. The value of both capacitor ang inductor must be verified. The value of the capacitor must be lower to avoid the voltage at the output side increase significantly if the value is high. The LC filter at the output side will give impact on the THD at the supply current. To reduce the THD, several methods were used; changing the modulation index (between 1 to 9) and switching frequency of the IGBTs. Those methods can indicate the suitable modulation index and switching frequency to get the lowest THD. The suitable values then were used and connected to CPL.

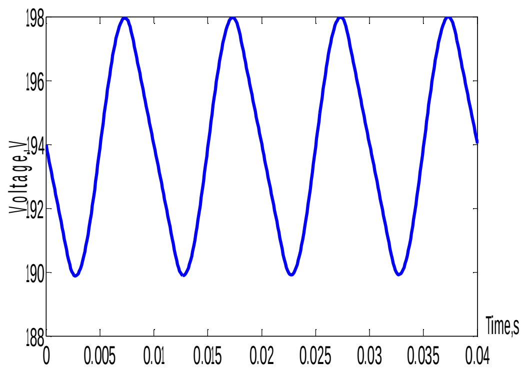

Figure 14: Voltage across the CPL.

Figure 14 shows the result from simulation; output voltage at the load from the SPMC connected with CPL for Ma=7 and Fs=70kHz .

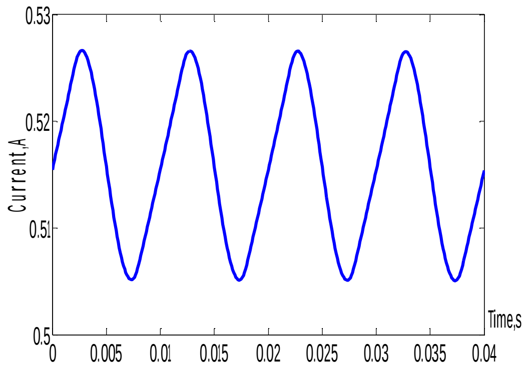

Figure 15: Current through the CPL.

Figure 15 shows the result from simulation; output current at the load from the SPMC connected with CPL for Ma=7 and Fs=70kHz.

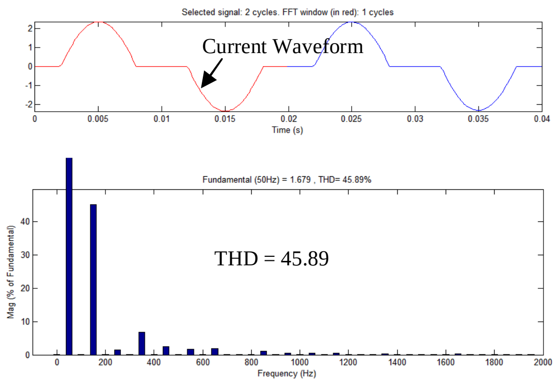

Figure 16: THD at supply current.

Figure 16 shows the result from simulation; THD at supply current from the SPMC connected with CPL for Ma=7 and Fs=70kHz.

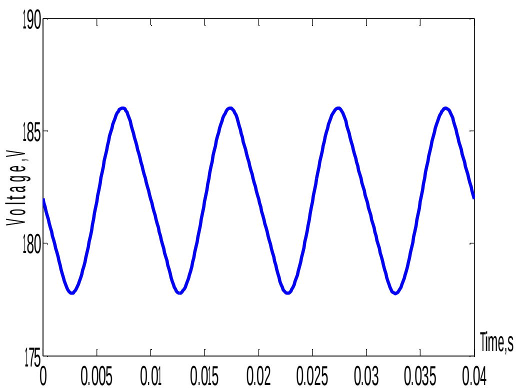

Figure 17: Voltage across the CPL.

Figure 17 shows the result from simulation; output voltage at the load from the SPMC connected with CPL for Ma=6 and Fs=70kHz .

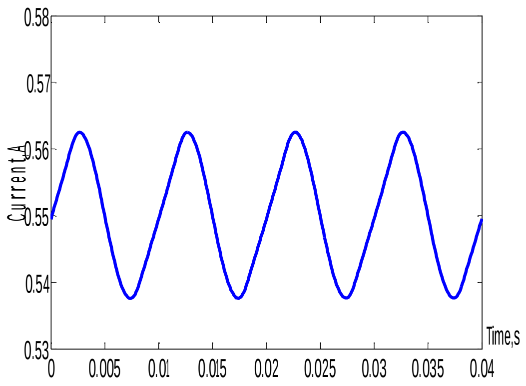

Figure 18: Current through the CPL.

Figure 18 shows the result from simulation; output current at the load from the SPMC connected with CPL for Ma=6 and Fs=70kHz.

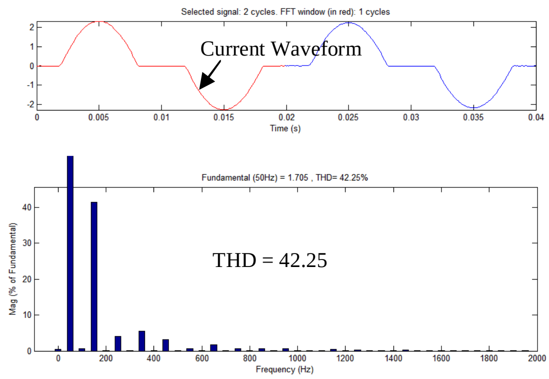

Figure 19: THD at supply current.

Figure 19 shows the result from simulation; THD at supply current from the SPMC connected with CPL for Ma=6 and Fs=70kHz.

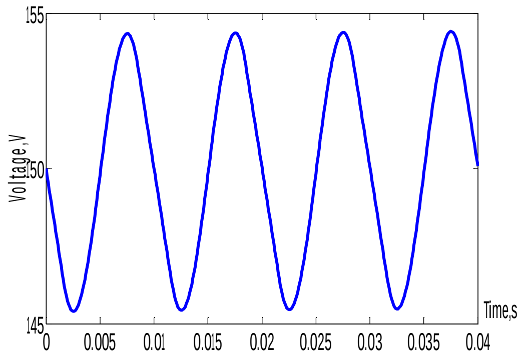

Figure 20: Voltage across the CPL.

Figure 20 shows the result from simulation; output voltage at the load from the SPMC connected with CPL for Ma=5 and Fs=70kHz .

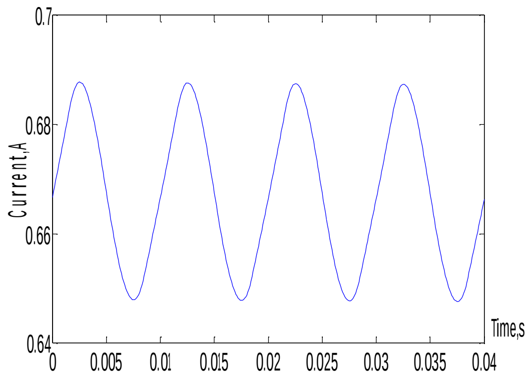

Figure 21: Current through the CPL.

Figure 21 shows result from simulation; output current at the load from the SPMC connected with CPL for Ma=5 and Fs=70kHz.

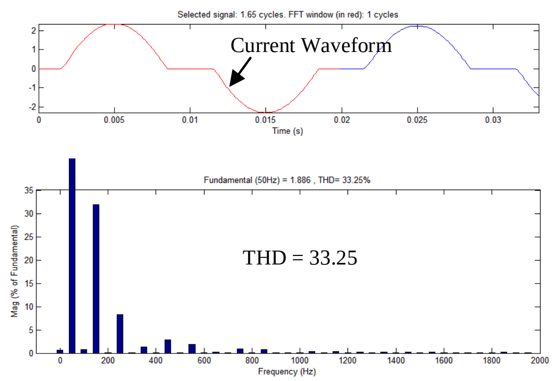

Figure 22: THD at supply current.

Figure 22 shows the result from simulation; THD at supply current from the SPMC connected with CPL for Ma=5 and Fs=70kHz.

Since the CPL injected with 100 watt of power, by multiplying the voltage and current value at one point, it will result the amount of the power injected (100 watt). Figure 28 shows the complete circuit diagram of a SPMC with a CPL along with the input and output LC filter.

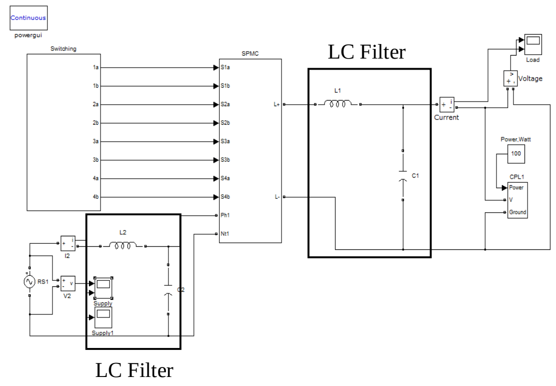

Figure 23: SPMC with CPL.

Table 2 : Results of the SPMC before and after connected with CPL

Modulation Index, Ma	Switching Frequency, Fs	% THD Before CPL	% THD with CPL	% THD with CPL and LC Filter (Intput)
5	70kHz	3.68	33.25	1.58
6	70kHz	4.29	42.25	1.49
7	70kHz	4.80	45.89	1.34

Table 2 shows the results of the THD at supply current before SPMC connected with CPL, after SPMC connected with CPL and CPL with input filter. It shows that THD can be reduced by introducing the LC filter at the input side.

6. Conclusion

This paper illustrates the details on the simulation SPMC operating as rectifier driving a constant power load (CPL) complete with theoretical. The results confirmed that the SPMC which is operating as a rectifier is able to control the CPL without any problems and the THD can be reduced below 5%. During this simulation, there were values to be considered; the output voltage and current and the THD of the input current. To get the expected result, some configuration in the MLS must be justified such as Configuration Parameters.

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