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CHARACTERIZA TION OF GaAs MESFETs USING NOVEL TEST FIXTURES

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ABSTRACT

This paper reports on the characterization of GaAs MESFETs using novel test fixtures. The S-parameters of NEC NE76038 MESFETs were measured from 4 to 12 GHz using the fixtures in conjunction with a Wiltron 37269B vector network analyser. The test fixtures were constructed in-house using microstrip laminates having relative permitivity 2.33, and substrate and copper thicknesses of 0.5 mm and 0.0356 mm respectively. The results obtained from the measurement were found to agree quite well with data supplied by the manufacturer.

INTRODUCTION

We have embarked on a project to build microwave sub-systems for use in mobile telecommunications. The project entailed design and fabrication of several core components of cellular sub-systems, namely low noise amplifiers, high power amplifiers, oscillators, filters, mixers, couplers and antennas, details of which have been reported elsewhere [1-12].

GaAs metal-semiconductor field effect transistor (MESFET) is used extensively in the design of high frequency/high speed circuits. The rapid progress seen with mobile telecommunications has spawned the need for accurate characterization of these transistors to improve design and reliability.

A test fixture is necessary in order to mount a transistor in a test circuit with microstrip connecting lines. The fixture acts as an interface for non-coaxial devices to a network analyzer. In addition to this, the fixture must introduce minimum change to the test signal without destroying the device under test (DUT) while at the same time provide repeatable connection. Ideally, a good test fixture should provide a transparent connection between the test instrument and the DUT. It should introduce no loss and has a flat frequency response to prevent distortion of the actual signal. A perfect match to both the instrument and the DUT eliminates reflected test signals. The signal should be effectively coupled into the test device, rather than leaking around the device and resulting in crosstalk from input to output.

Standard test fixtures are already available in the market. We are however proposing a new design which allows the fixture to be fabricated in the faculty while at the same time offering the ease of use and accuracy comparable to those available commercially. The fixture consists of two 50 Ω transmission lines fabricated on microstrip laminate [13]. The lines tare separated by a 3 mm gap in the middle to place the transistor (Fig. 1).

A transistor mounted in a test fixture requires appropriate bias voltage to be applied to their terminals. A biasing network is necessary to supply this voltage because the bias cannot be supplied through a connector.

For our test fixture, a low- pass filter circuit is used to provide the required bias. This is preferable to those found in the market whereby no biasing network is provided on the board. This necessitates the use of micro- positioners and thus adds extra complexity to the user. The novel fixturing approach here is designed and implemented not only to eliminate the need for expensive test fixtures but also to cater for transistors of specific packages.

DESIGN PROCEDURES

Some important criteria that should be taken into account in designing test fixtures are ease of use (getting the device in and out of the fixture), ruggedness, low parasitics and more importantly, adaptable to standard calibration techniques. The main goal here is to develop a system featuring exceptional flexibility, repeatability and high measurement accuracy.

DC Bias Design

The necessary biasing and earth return paths to the main microstrip transmission line are made using biasing networks that take the form of a low pass filter. The principle of operation is that RF signal is prevented from going into the dc source but allowed to bias the transistor. The filter consists of two series inductor and a shunt capacitor as shown in Fig. 1. These series inductors and shunt capacitor are approximated by a short length high impedance transmission line and by a low impedance open circuit stub respectively [14].

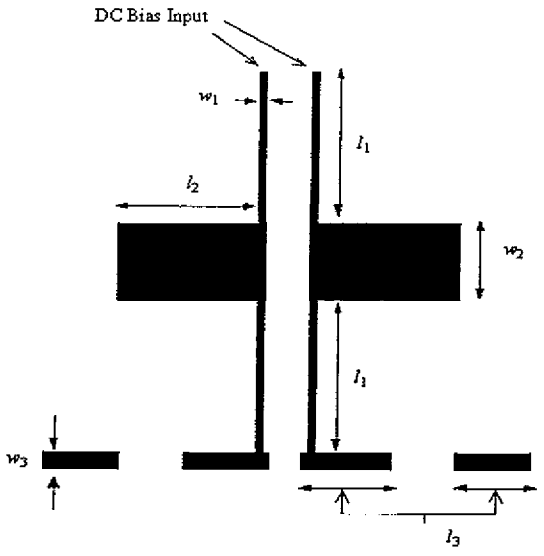


Figure 1: Layout of the test fixture showing the biasing circuit

Calculation of Microstrip Line Dimensions

The line dimensions are synthesized in *LineCalc* in *Eesof Libra*. In the software, entering the value of the characteristic impedance of the line Z_o yields the corresponding line width w and effective relative permittivity k_{eff}. The line length l_m was then calculated using

$$l_m = \frac{\lambda_m}{4}$$

where $\lambda_m = \lambda_o/\sqrt{(k_{eff})}$ and $\lambda_o = c/f$; λ_o and λ_m are the wavelength of the signals in free space and in microstrip medium respectively, c is the speed of light and f is the frequency of measurement.

Using transformation formulae in [14], each series inductor and shunt capacitor will yield lines of different lengths and Z_o. The characteristic impedance of the transmission line is taken as 50 Ω whereas for the series inductor and shunt capacitor they are 90 Ω and 15 Ω respectively. Table 1 below depicts the line dimensions for each element and Figure 1 shows the layout.

Frequ-ency (GHz)	Transmis-sion line l_3 (50 Ω)	Width w_3	Series Inductor l_1 (90 Ω)	Width w_1	Shunt Capacitor l_2 (15 Ω)	Width w_2
4	13.393	1.440	13.860	0.488	12.728	6.936
6	8.929	1.440	9.240	0.488	8.466	6.953
8	6.679	1.442	6.930	0.489	6.350	6.972
10	5.344	1.444	5.544	0.489	5.068	6.994
12	4.442	1.447	4.608	0.491	4.214	7.018

Table 1: Line dimensions for the biasing circuit. All dimensions are in mm.

FABRICATION PROCESS

The circuit layout was then generated within *Libra* and then imported into *Freehand 9.0* to generate the mask. The circuit was produced in the laboratory using standard printed circuit processing techniques [15]. Fig. 2 shows an example of a test fixture fabricated in this study.

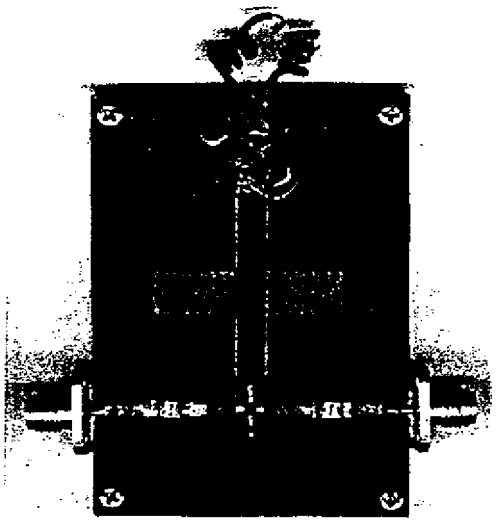


Figure 2 : Actual test fixture fabricated in this study

CALIBRATION

The accuracy of any measurement is dictated by the precision of test equipment used and the errors introduced by the test fixture. Data obtained from measurements are then corrected by error correction models. In high frequency measurements, errors from the fixture comprise of transistor package parasitics which can be dominant as the frequency is increased. Care must therefore be taken to ensure the parasitics are properly subtracted out to yield the actual data. This explains the rather elaborate calibration procedures adopted for microwave measurements. In the case of transistor characterization, calibration is the first task required before the S-parameters are measured on the vector network analyzer.

In this work, a full two-port calibration model was employed for the error correction. The model comprises reflection and transmission measurements whereby all twelve systematic error terms which result are measured and removed. This required twelve measurements on four known standards (short-open-load-thru or SOLT) at the selected frequencies, details of which have been reported in [11]. Upon completion, the calibration process was verified using standard loads different from the ones used in the calibration. This was then followed by the S-parameter measurement.

RESULTS AND DISCUSSION

Data obtained from the experiment are tabulated below. Also shown are data from the manufacturer for comparison. The data were measured from 4 GHz to 12 GHz at 2 GHz intervals.

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
4	0.55	-87	3.09	85	0.07	74	0.57	-64
6	0.62	-114	2.35	67	0.08	42	0.54	-97
8	0.50	-157	1.90	43	0.13	-1	0.34	-139
10	0.45	-172	1.66	13	0.15	-25	0.25	-161
12	0.35	157	1.26	-7	0.25	-37	0.30	179

Table 2 : Data obtained from measurement at selected frequencies

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
4	0.84	-68	3.1	115	0.08	47	0.54	-46
6	0.70	-106	2.8	84	0.10	28	0.45	-70
8	0.61	-145	2.5	55	0.11	16	0.37	-92
10	0.57	175	2.2	27	0.11	7	0.30	-118
12	0.60	139	1.9	2	0.12	0	0.27	-157

Table 3 : Data from manufacturer

Owing to their complex nature, S-parameter values are more conveniently presented graphically on Smith chart. These are shown in

Figs. 5.1 to 5.4 together with the manufacturer values for comparison. Each transistor was biased at V_{DS} = 3V and I_{DS} = 10 mA as specified in the data sheet. It is important this is adhered to since S-parameters depend on biasing.

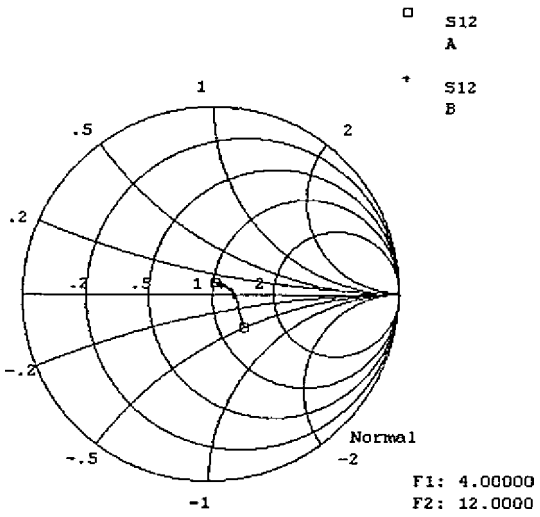


Figure 3 : Comparison between measured ( ) and manufacturer (+) S_{11}

Fig. 3 shows S_{11} - the input reflection coefficient of the transistor which is related to the input impedance. As can be seen, the agreement is excellent, especially at the lower frequency end. The manufacturer values traverse over bigger distance across the Smith chart than measured values. The manufacturer data started out inductively at the lower frequencies and move towards the capacitive region as the frequencies increase.

The trace for measured values obtained from the experiment is shorter however. This implies the parasitics present in the transistor package are actually lower than predicted by the manufacturer since the length of the trace depends on the amount of parasitics. The magnitudes of our S_{11} (indicated by the distance of the trace from the center of the chart) are also lower. This may be explained in terms of errors which arise when the position of the reference plane was determined. Transistor bonding leads in particular have been known to give rise to this error since it is difficult to determine the electrical length of the leads inside the transistor package. The leads are normally modeled as a series inductance, which increases the parasitic inductance of the transistor [16]. Other possible explanation to this discrepancy is the input gate inductance which we could not determine accurately due to the nature of the transistor package. In sum the agreement between our data and those obtained from the manufacturer is reasonably good, especially from 4 to 8 GHz.

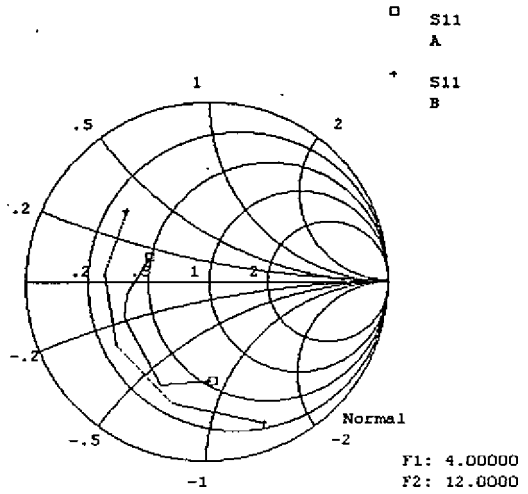


Figure 4 : Comparison between measured ( ) and manufacturer (+) S_{12}

Figure 4 shows the reverse transmission coefficient of the transistor (S_{12}). Here the agreement is not so good. The measured data however traverse longer, indicating a higher presence of parasitics. Since transmission of signals in the reverse direction is small, the errors involved are thus smaller. Both traces demonstrate capacitive behaviour at the low frequency end, becoming more inductive as the frequency is increased. This is due to parasitic elements which spread the data broader at higher frequencies. In general, data obtained from the measurement are very close to the quoted values. This indicate the high accuracies possible with our test fixtures, especially with measurements of S_{11}.

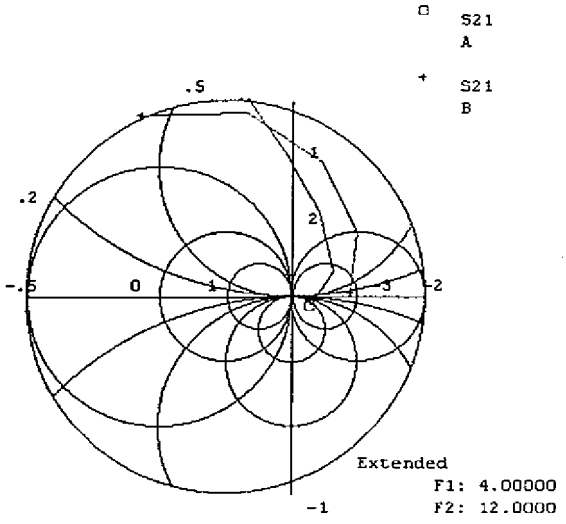


Figure 5 : Comparison between measured ( ) and manufacturer (+) S_{21} from 4 GHz - 12 GHz

Figure 5 shows the forward transmission coefficient (S_{21}), the magnitude of which indicates transistor gain. The agreement seen here is generally good although the magnitude of our data is slightly smaller than quoted values, especially at the high frequency end. This implies the actual gain offered by the transistor is smaller than that claimed by the manufacturer. The reduced values can be explained in terms of the effect of parasitic elements which negate the amplification of the transistor as the frequency is increased. The amplifier thus exhibits less gain as shown in the chart. The angles of S_{12} however concur with the manufacturer quite well throughout the range.

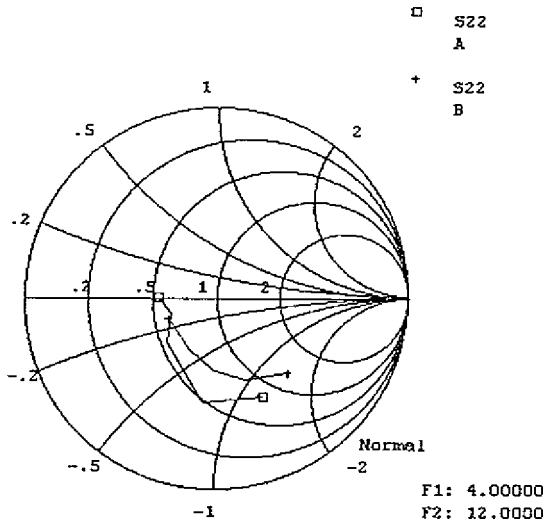


Figure 6 : Comparison between measurement ( ) and datasheet (+) S_{22} from 4 GHz - 12 GHz

The S_{22} is related to the output reflection coefficient. These are plotted in Figure 6. There is reasonable agreement between the two sets of data, both curves being capacitive for most part of the frequency range. The measured values differ slightly at the lower end. This may be due to the effect of parasitic elements at the output drain which spread the data out across the frequency range.

CONCLUSION

In sum we can conclude that the fixtures performed quite well through out the whole frequency range. The measured S-parameters were quite close to manufacturer data especially S_{11} and S_{22}. There are however some discrepancies which were probably due to improper dc biasing and uncertainties involved in defining the reference planes. The former affects the operating point of the transistor, thereby yielding slightly different S-parameter values. The latter were due to errors which arise from the

fabrication process which affected the microstrip line dimensions, giving rise to errors in setting the refrence plane. Given time this can be reduced further by improved fabrication process.

The discrepancy between measured values and quoted data were not only caused by the above factors but also due to the fact that manufacturer data were sampled at random across the whole batch of the transistor. The data quoted by them are therefore average representation of the transistor performance.

In this project, we have managed to fabricate several test fixtures to measure MESFETs. Although the fixtures were fabricated in-house they offered a reasonable degree of repeatability. This improved the contact made to the transistor for each measurement, which in turn enhanched the accuracy of the readings. The novel fixturing approach we adopted not only eliminated the need for expensive test fixtures but more importantly allowed us to fabricate fixtures customized to specific applications with accuracies comparable to commercially available test jigs.

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