DIGEST

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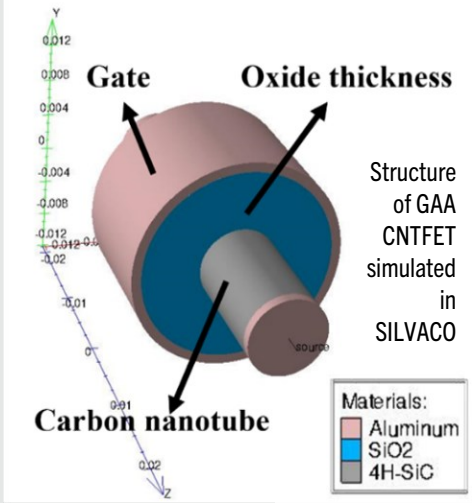
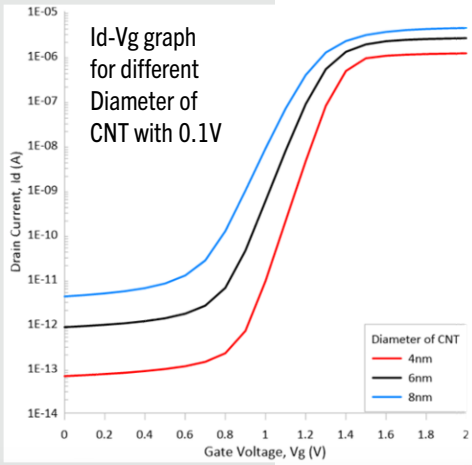
CARBON NANOTUBE FIELD EFFECT TRANSISTOR: Taguchi approach for device and circuit level optimization

by Ir. Ts. Dr. Hanim Hussin

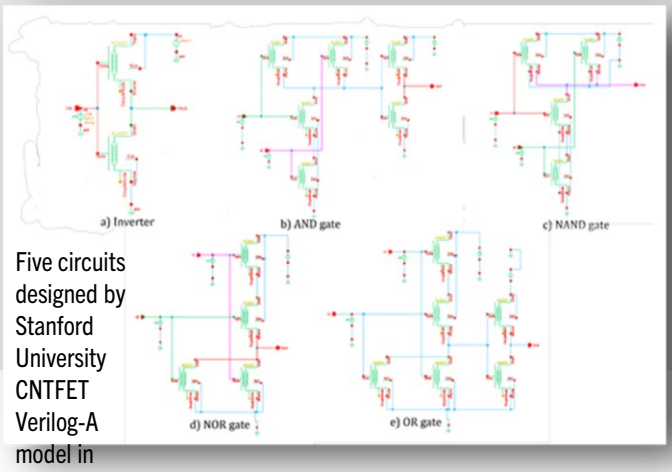
The research problem that motivated the study titled "CARBON NANOTUBE FIELD EFFECT TRANSISTOR: Taguchi Approach for Device and Circuit Level Optimization" is the increasing demand for energy-efficient, high-performance transistors, particularly as traditional silicon-based transistors encounter physical and performance constraints at nanoscale dimensions. The study utilizes the Taguchi method, a statistical optimization technique, to enhance the design and performance of carbon nanotube field-effect transistors (CNTFETs). This approach enables the systematic optimization of multiple parameters at both the device and circuit levels, resulting in improved energy efficiency and performance hence effectively addressing the limitations of conventional silicon-based technologies. The optimal combination for achieving the highest current ratio in CNTFETs consists of the CNT diameter, oxide thickness and dielectric material. The implementation of the Taguchi method results in a significant reduction in the power delay product (PDP) for the optimized CNTFET. These findings demonstrate that the Taguchi method provides substantial improvements in power efficiency and circuit speed, underscoring its potential for energy-efficient and high-speed circuit design. The research results are significant because they demonstrate a method for optimizing carbon nanotube field-effect transistors (CNTFETs), leading to more energy-efficient and faster electronic devices, which can contribute to reducing power consumption and improving performance in advanced technologies, benefiting society through more sustainable and powerful computing solutions.



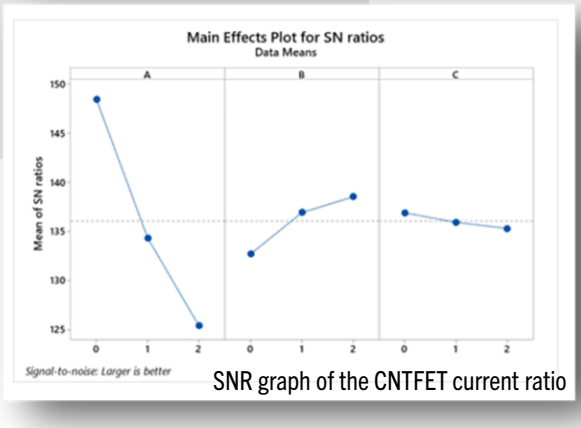
Structure of GAA CNTFET simulated in SILVACO



Id-Vg graph for different Diameter of CNT with 0.1V



Five circuits designed by Stanford University CNTFET Verilog-A model in Cadence Virtuoso



SNR graph of the CNTFET current ratio

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