Comparison Study of Lightly Doped Drain (LDD) and Double Diffused Drain (DDD) to Overcome Hot Carrier Effect on 90nm CMOS Devices

Mohd Hafizi Bin Surani
Faculty of Electrical Engineering, Universiti Teknologi MARA Malaysia
40450 Shah Alam, Selangor, Malaysia
hafizisurani@gmail.com

Abstract — **In this project, the analysis and the simulation of the comparison between lightly doped drain (LDD) and double diffused drain (DDD) were studied to overcome the hot carrier effect on 90nm CMOS devices. Silvaco TCAD is a tools that used to measure substrate current (Isub), gate current (Igate) and gate voltage (Vg), where Vg at Isub and Igate directly related to impact ionization that occurred during hot carrier effect in deep submicrometer MOSFET's. The comparison will be make in order to know which method is the best to overcome hot carrier effect on 90nm CMOS devices. As a result, it can be conclude that LDD structure is better to overcome hot carrier effect on 90nm NMOS device, which Isub and Igate were reduce to 48.12 % and 79.67 % respectively, while on 90nm PMOS device, DDD structure is better which Isub and Igate were reduce to 88.17 % and 65.83 % respectively.**

Keywords: LDD, DDD, 90nm CMOS, Hot Carrier Effect.

1. INTRODUCTION

With device feature size become scaling down, hot carriers is become a serious constrain on device scaling and hot carrier reliability is one of the major concern in modern technology [1][2]. The term hot carriers refers to either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor device. Because of their high kinetic energy, hot carrier can get injected and trapped in areas of device where they should not be and forming a space charge that cause the device to degrade or become unstable.

Hot carrier injection process occurs mainly in a narrow injection zone at the drain end of the device where the lateral field. Without consider decreasing the operating voltage in device, the electrical fields in the device will increase [3]. Due the electric field increase in the silicon gate and around the drain, the hot carrier became critical problem [2]. Increasing electric field of the channel, the drain current easily ionized electrons and holes around the drain. This phenomenon is called 'impact ionization'. It is happen when the electron and hole gain enough energy to excite and create a pairs in the silicon surface, as shown in figure 1. The impact ionization is possible to degrade the parametric characteristic of the device.

The simple methods to investigate the hot carrier in device are by measuring the Isub and Igate [4]. Isub is a product of drain current and the impact ionization. Usually the magnitude gate current is smaller than the substrate current due to avalanche multiplication. The gate current was representing direct measurement for the carriers were injected into the oxide [2].

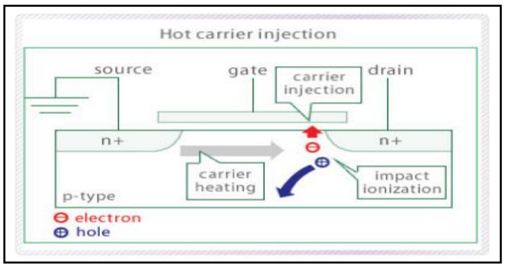


Figure 1: Injection involves impact ionization of carriers near the drain area in NMOS device.

1.1 Methods to overcome hot carrier effect

The injection of hot carrier into oxide will cause degradation of the transistor characteristic. This injection can shift the characteristic of transconductance, threshold voltage and drive current of the device. To overcome the problem of hot carrier effect, two methods are approaches; Lightly Doped Drain (LDD) and Double Diffused Drain (DDD).

1.1.1 Lightly Doped Drain (LDD)

LDD structure in MOSFET's are commonly used to improve hot carrier reliability of sub-micrometer device [6]. In the LDD structure, lightly doped, n^- regions were introduced between the channel and n^+ source/drain diffusions. This structure can reduce impact ionization by spreading out of the electric field in the n^- region [7]. Figure 2 show the example of LDD structure on NMOS device. Phosphorous was normally implanted to form the n^- LDD region for NMOS while Boron form p^- LDD region for PMOS device, after poly-silicon gate delineation. Then the oxide was deposited to form a spacer at the sidewall of the poly-silicon gate. The oxide spacer was used to serves a mask for the standard n^+ arsenic implant for NMOS, and p^+ indium implant for PMOS, at source and drain. The length and doping concentration of the n^- region control the electric field strength and distribution in the pinch off region independently from the existing device parameters. The n^- region is behaves as a series resistance in the device which this will cause increasing in power supply voltage or a reduction in channel length.

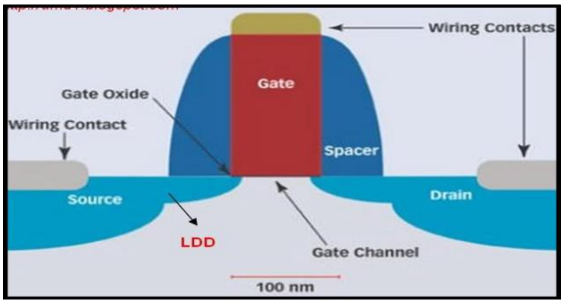


Figure 2: The LDD structure on NMOS device.

1.1.2 Double Diffuse Drain (DDD)

DDD is performed by two donor type implant that have provided a graded rather than an abrupt junction [9]. For NMOS, phosphorous (P) and arsenic (As) are used to implant at source/drain, while for PMOS, boron (B) and indium (In) were used. In DDD NMOS devices, the lightly n^- regions ring around the n^+ source/drain diffusions region by using double implantation of arsenic and phosphorus, as shown in figure 3. Phosphorus was used as n^- region because phosphorus diffused faster than arsenic, while for PMOS, boron was used as p^- region because boron diffused faster than indium. This structure will reduce the electric field at the drain. In DDD structure, the electric field is defined by the profile of the n^- diffusion layer. No additional masking like oxide sidewall required in DDD structure, hence will save the cost of fabrication for the device [8].

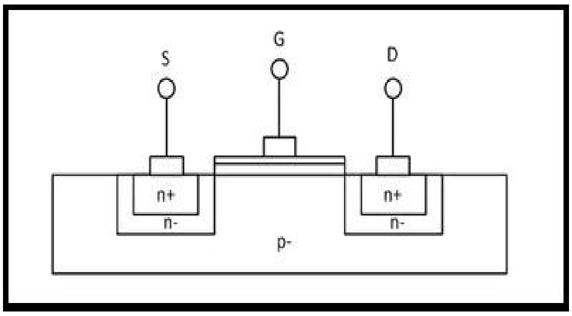


Figure 3: The DDD structure on NMOS device.

2. METHODOLOGY

In this analysis, the 90nm CMOS device using LDD and DDD were studied. Silvaco TCAD, the process and simulation software tool, were used to simulate the devices. Process simulation refers to the fabrication technology of a device based on process recipe and device simulation refers to the device performance analysis based on a given structure. In Silvaco TCAD, this is provided by the interactive modules that are Deckbuild and Tonyplot. Deckbuild is where the input will be type and view the simulation running in real time while Tonyplot is to view the output graphically.

Silvaco TCAD has two main frameworks that are ATHENA and ATLAS. ATHENA is a process simulation framework. In ATHENA, input information is the recipe like materials, temperature, chemical and time. Output of the ATHENA is the device structure as a result of the recipe. From the physical output, measurement likes thickness, Vth, sheet resistance and concentration profile can be determined. ATLAS is a device simulation framework. In ATLAS, the input information is the structure, the tests to be carried out likes biasing and current voltage sweep and numerical method applied. Outputs of the ATLAS are the device extract parameter, characteristics or cross section behavior under specified tests. From the output, the device parameters and characteristic can be determined.

2.1 Lightly Doped Drain (LDD)

To studied hot carrier effect in LDD structure, two types of investigations are used. These two types are specifically focusing on the concentration dose and implant energy, which on the n^- region for NMOS and p^- region for PMOS of the LDD structure. These investigations will produce the measurement of Isub and Igate, where Isub and Igate directly related to the hot carrier effect. From the previous research, already showed that suitable value on the concentration dose and implant energy in LDD simulation on NMOS device were equal to 3e13 ions/cm^2 and 20Kev respectively, while on PMOS device were equal to 1e13 ions/cm^2 and 20Kev respectively. Source was grounded, while Isub and Igate were measured at drain voltage equal to 3.3V, and gate voltage is set varied from 0.025V – 6V.

2.2 Double Diffuse Drain (DDD)

In DDD structure, Isub and Igate were measured by varying the n^- and p^- concentration dose on NMOS and PMOS device respectively. Previous research was showed the suitable value on the concentration dose in DDD simulation on NMOS device were equal to 8e13 ions/cm^2, while on PMOS device were equal to 9e12 ions/cm^2. In NMOS, the n^+ concentration, arsenic (As), was set to 5e11 ions/cm^2, while the p^+ concentration on PMOS, indium (In), was set to 5e12 ions/cm^2. After deposited the gate poly-silicon, n^- and p^- concentration were implant at source/drain respectively. Then the n^- and p^- region were annealing with N_2 atmosphere. After that the n^+ and p^+ concentration will implant at source/drain respectively. In DDD structure, no additional masking processes were required because the light and heavy concentration were implant at same region. Source was grounded, while Isub and Igate of this device was measured at drain voltage equal to 3.3V and gate voltage was set varied from 0.025V – 6V, similar as LDD simulation.

3. RESULT AND DISCUSSION

The comparison between LDD and DDD on 90nm CMOS devices were analyzed and simulated in order to know which method is the best to overcome hot carrier effect. To simulate the CMOS device, the structure separated to NMOS and PMOS because of our Silvaco TCAD was not in mix mode tools.

3.1 Lightly Doped Drain (LDD)

Figure 4(a) and Figure 4(b) show the completed 90nm NMOS and PMOS device with LDD structure respectively. Figure 5(a) and Figure 5(b) show the electrical characteristic curve for NMOS and PMOS device respectively. In this studied, lower substrate current (Isub), lower gate current (Igate) and larger gate voltage (Vg) were desirable. Table 1 shows the data collection.

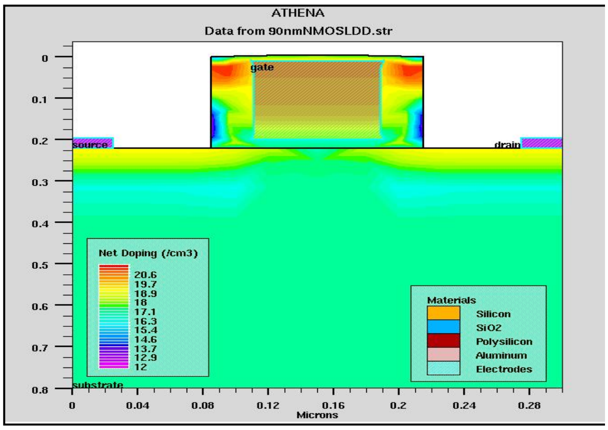


Figure 4(a): The structure of LDD on 90nm NMOS device.

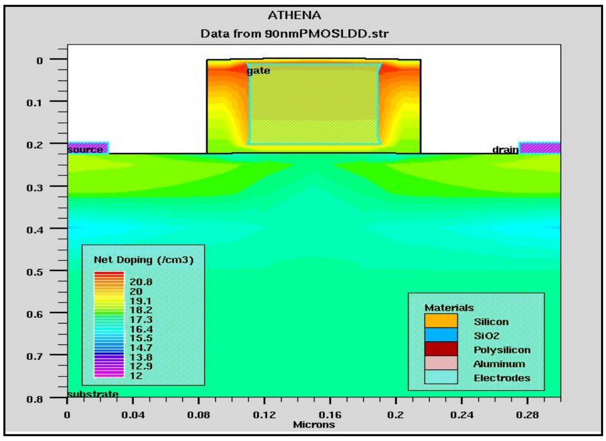


Figure 4(b): The structure of LDD on 90nm PMOS device.

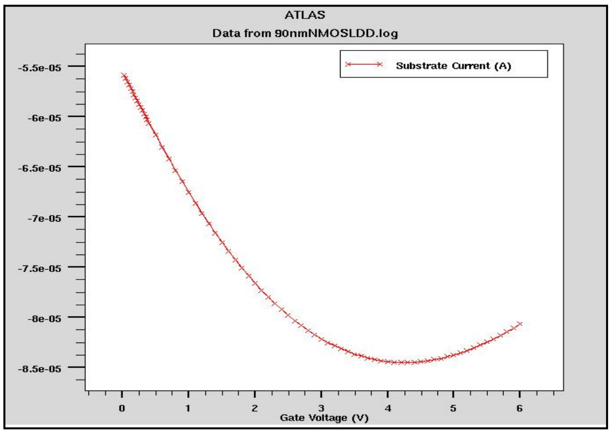


Figure 5(a): Graph Vg vs Isub for LDD on 90nm NMOS device.

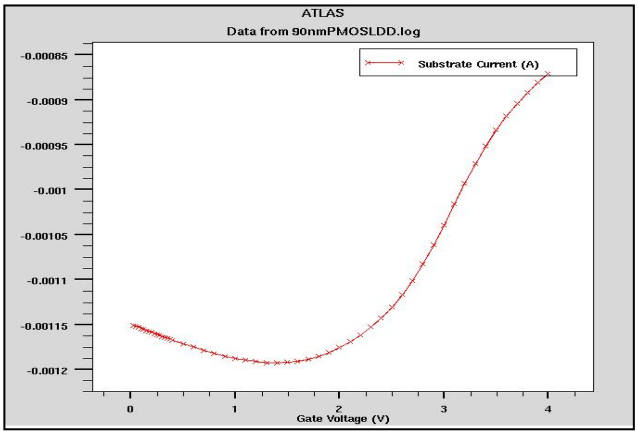


Figure 5(b): Graph Vg vs Isub for LDD on 90nm PMOS device.

Table 1: Electrical characteristics for LDD on 90nm NMOS and PMOS device

Device	Isub (10^{-5} A)	Vg (V)	Igate (10^{-12} A)	Vg (V)
NMOS	8.44817	4.2974	2.53	5.9
PMOS	119.248	1.3998	7.22	2.2

3.2 Double Diffuse Drain (DDD)

Figure 6(a) and Figure 6(b) show the completed 90nm NMOS and PMOS device with DDD structure respectively, while Figure 7(a) and Figure 7(b) show the electrical characteristic curve for NMOS and PMOS device respectively. In this studied also lower substrate current (Isub), lower gate current (Igate) and larger gate voltage (Vg) were desirable. Table 2 shows the data collection.

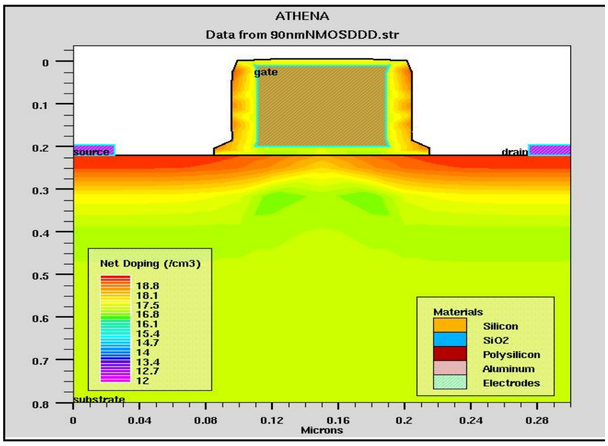


Figure 6(a): The structure of DDD on 90nm NMOS device.

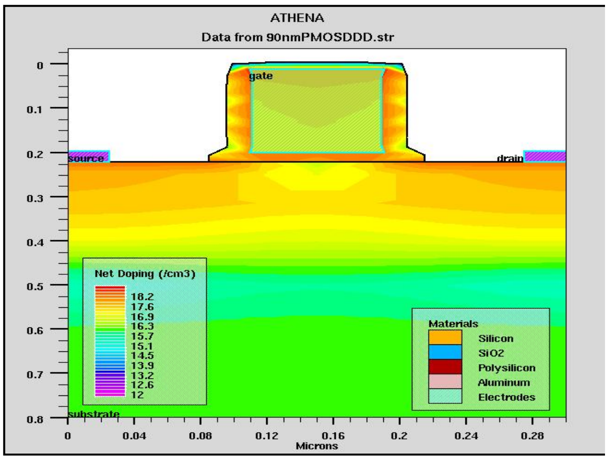


Figure 6(b): The structure of DDD on 90nm PMOS device.

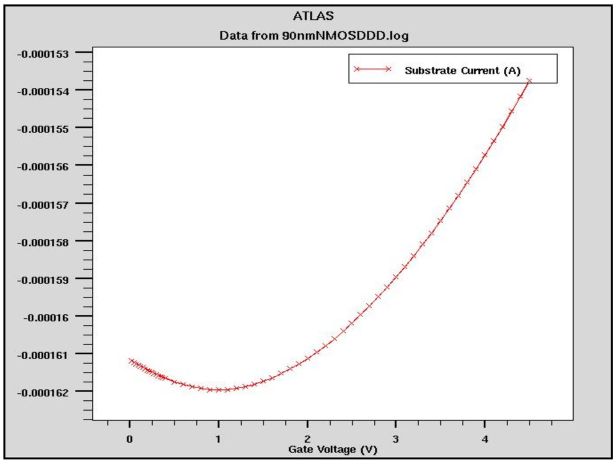


Figure 7(a): Graph Vg vs Isub for DDD on 90nm NMOS device.

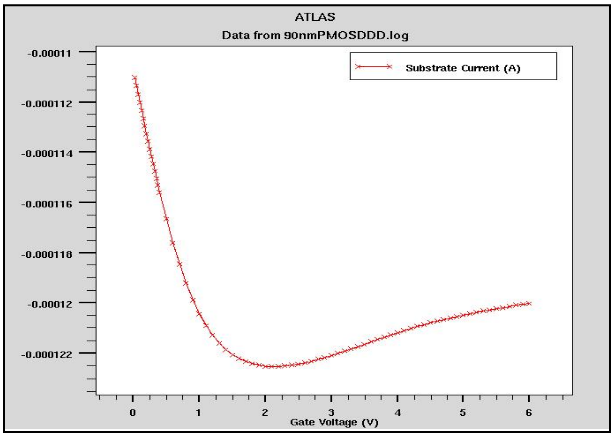


Figure 7(b): Graph Vg vs Isub for DDD on 90nm PMOS device.

Table 2: Electrical characteristics for DDD on 90nm NMOS and PMOS device

Device	Isub (10^{-5} A)	Vg (V)	Igate (10^{-12}A)	Vg (V)
NMOS	16.195	0.9985	12.38	4.5
PMOS	14.096	2.4	2.469	6

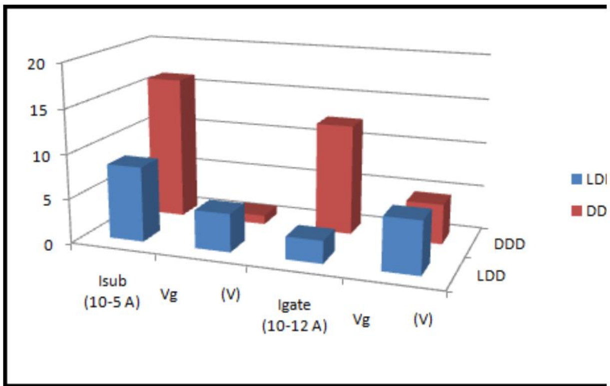
3.3 Comparison of LDD and DDD structure on 90nm CMOS device.

By referring to the Figure 5 and Figure 7, it shows that the electric field was reduced by the gate voltage increase after Isub was maximum. This happen because the corresponding higher Vdsat, so that electric field was lower according the equation below [8]:

$$Em = \frac{(Vd - Vdsat)}{l}$$

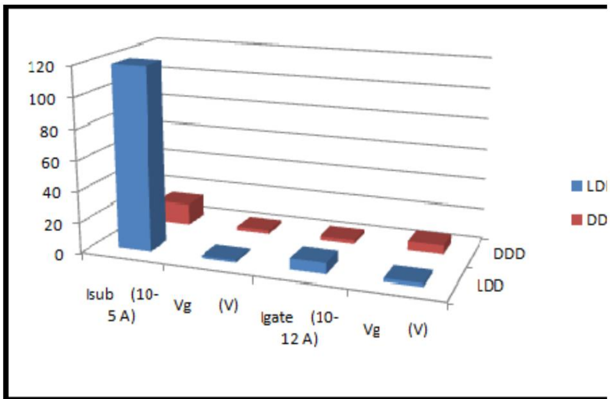
Where l = channel length
Vd = Drain voltage
$Vdsat$ = Saturation drain voltage

According to the data in Table 1 and Table 2, the best result for 90nm CMOS device by using LDD structure for NMOS and DDD structure for PMOS, because the result shows that the Isub and Igate were small and Vg was large, as shown in Figure 8(a) and Figure 8(b) respectively.



Device	Isub (10^{-5} A)	Vg (V)	Igate (10^{-12} A)	Vg (V)
LDD	8.44817	4.2974	2.53	5.9
DDD	16.195	0.9985	12.38	4.5

Figure 8(a): Comparison between LDD and DDD on 90nm NMOS device.



Device	Isub (10^{-5} A)	Vg (V)	Igate (10^{-12} A)	Vg (
LDD	119.248	1.3998	7.22	2.2
DDD	14.096	2.4	2.469	6

Figure 8(b): Comparison between LDD and DDD on 90nm PMOS device.

Comparison between LDD and DDD are shown as calculation where the percentages reduction of Isub and Igate.

1) NMOS device :

$$\% \; Isub = \frac{(16.19e^{-5}) - (8.4e^{-5})}{16.19e^{-5}} \text{x}100$$

$$= 48.12 \; \%$$

$$\% \; Igate = \frac{(12.3e^{-12}) - (2.e^{-12})}{12.3e^{-12}} \text{x}100$$

$$= 79.67 \; \%$$

2) PMOS device :

$$\% \; Isub = \frac{(119.2e^{-5}) - (14.09e^{-5})}{119.2e^{-5}} \text{x}100$$

$$= 88.17 \; \%$$

$$\% \; Igate = \frac{(7.22e^{-12}) - (2.46e^{-12})}{7.22e^{-12}} \text{x}100$$

$$= 65.83 \; \%$$

4. CONCLUSION

The comparison between LDD and DDD to overcome the hot carrier effect in 90nm CMOS device were studied. From the analysis, it can be conclude that all of the method can be use to overcome the hot carrier effect, that occurred during impact ionization. Impact ionization was the main problem in degradation of MOSFET's devices like shift the characteristic of trans-conductance, threshold voltage and drives current. As a result, LDD structure is better to the overcome hot carrier effect on 90nm NMOS device, which Isub and Igate were reduced to 48.12 % and 79.67 % respectively, while on 90nm PMOS device, DDD structure is better which Isub and Igate were reduce to 88.17 % and 65.83 % respectively.

ACKNOWLEDGMENT

In the name of Allah, God the almighty, I would like to pay my gratitude for providing me strength, patience, ability and guidance to accomplish this project successfully. In the role of supervisors, special credit goes to Pn Norhazlin Khairudin, lecturer of Universiti Teknologi MARA. My thanks go for your continued encouragement, support in idea, advising and supervising in this research. Your advice and insight have been a guiding light for me. I also express my appreciation to all lecturers whom help me especially PM Dr Mohamad Rusop Mahmud and Cik Harnani Hassan for her teaching in Semiconductor technology and responsible to introduce me with Silvaco TCAD simulation software. To my family, thanks for the support and advice that makes this work possible. Not forget to my entire friend who had given me support and contribution to finish this project. May Allah bless and reward them for their generosity.

REFERENCES

[1] Miryeong Song, Kenneth P. Macwilliams and Jason C. S. Woo, ''Comparison Of NMOS and PMOS Hot Carrier From 300K to 77K'', IEEE Transaction On Electron Devices, Vol. 44, No. 2, February 1997.

[2] Guido V. Groeseneken, ''Hot Carrier Degradation and ESD in Submicrometer CMOS Technologies: How Do They Interact?", IEEE Transactions On Device and Materials Reliability, Vol. 1, No. 1, March 2001.

[3] Hyun-Sik Choi, Seung-Ho Hong, Hee-Sung Kang, and Yoon-Ha Jeong, "Hot Carrier Stress in 70-nm nMOSFET with Various Bias Conditions", Nanotechnology Materials and Devices Conference, 2006 (NMDC 2006), IEEE Vol. 1.

[4] Sanchez, J.J., Hsueh, K., DeMassa, T.A., ''Hot Electron Device Monitoring and Characterization: a review", IEEE Proceedings, Vol. 135.

[5] Mizuki Ono, Masanobu Saito,Takashi Yoshitomi,Claudio Fiegna, Tatsuya Ohguro, Hisayo Sasaki Momose and Hiroshi Iwai ''A Study On Hot Carrier Effects on N-MOSFET's Under High Substrate Impurity Concentration" IEEE Transactions,Vol. 42

[6] Jone F. Chen, Jiang Tao, Peng Fang and Chenming Hu, ''Performance and Reliability Comparison Between Asymmetric and Symmetric LDD Device and Logic Gate".

[7] S. Ogura, P.J. Tsang, W. W. Walker, D.L. Critchlow and J.F. Shepard, ''Design and characteristics of LDD insulated gate field effect transistor", IEEE Trans. Vol. 34.

[8] Takeda. E., Yang C.Y., Miura-Hamada A. ''Hot Carrier Effect In MOS Devices", Academic Press, 1995, pp 147-172.

[9] Chen J.Y., ''CMOS Devices and Technology for VLSI" ,Prentice-Hall, 1990, pp 174.

[10] Mohd Khairi B Muhammad, ''Comparison Study of LDD and DDD To Overcome Hot Carrier Effect On 0.3um NMOS.