Electrical Properties of ZnO thin film prepared on Seeded Catalyst

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***Abstract*- This study focuses on the preparation ZnO thin film and effect on the surface morphology and electrical properties of ZnO thin film. The seeded ZnO catalyst was prepared by spin-coating technique using zinc acetate dehydrate (ZnAc) as starting material, 2-methoxyethanol as solvent, aluminium nitrate ($Al(NO_3)_3{\cdot}9H_2O$) as dopant and monoethanolamine (MEA) as stabilizer to coat onto silicon substrates. The ZnO thin films were deposited by thermal chemical vapor deposition (TCVD) method using zinc actetate dehydrate as a precursor and nitrogen as the carrier gas.The ZnO template as-deposited and post-annealed thin films are deposited and annealed at various temperatures from 400°C to 600°C. The effect of the surface morphology and electrical properties of ZnO thin film were investigated. Field gun emission scanning electron microscopy (FESEM) used to view the surface morphology of the samples. The surface morphology obtained from FESEM results showed the relationship between deposition temperatures for as-deposited and post-annealed thin films to the crystal structure and it also influenced the electrical properties of the ZnO thin films. The electrical properties are characterized using solar simulator measurement unit. This indicates that the electrical properties are improved in terms of conductivity for as-deposited thin film.**

Keywords : ZnO, FESEM, TCVD method, Thin films,Template, II-VI semiconductor.

I. INTRODUCTION

The semiconductor oxide materials e.g ZnO and TiO_2 have received considerable much attention in recent years due to their unique advantages: stable, inexpensive, wide band gap etc. Among them, ZnO is a unique material that exhibits both semiconducting properties which are intensively studied and applied in various applications such as gas sensor, dye sensitized solar cell, laser diodes (LDs) and light emitting diodes (LEDs) [1].

ZnO is an inorganic compound which that often called a II – VI semiconductor because zinc and oxygen belong to the 2nd and 6th groups of the periodic table respectively. This metal oxide semiconductors with a wide direct bandgap energy of 3.37eV and a larger free-exciton binding energy of 60meV at room temperature[2]. The property of ZnO is dependent partly on the crystallinity, crystallographic orientation, crystallite size and morphology. Due to various applications in electronic field, research has been focused to prepared ZnO thin films which are not only good in the optoelectronic an structural properties, non-toxicity, high lumineous transmittance, low cost [3,4] but also good in electrical properties.

There are many techniques to fabricate ZnO such as R.F. magnetron sputtering [5,6], reactive magnetron sputtering, chemical vapor deposition [7,8], ion-beam evaporation, electron-beam evaporation, spray pyrolysis [9,10], laser ablation and sol-gel process [11,12]. Among of them, the chemical vapor deposition technique have advantages in growth on large area substrates and mass production with a continous system. However, the deposition of zinc oxide by chemical vapor deposition has seen increased research activity over the past several years as the need for high quality zinc oxide thin film has increased [13,14].Post annealing treatment is a conventional and effective technique to reduce intrinsic defects and to improve the crystallinity in thin films [15].

In this study, thermal CVD has been used because of its relatively low cost and simple method [16]. The seeded ZnO catalyst were prepared by the spin-coating method. Zinc acetate dehydrate($Zn(CH_3COO)_22H_2O$),2methoxyethanol,aluminium nitrate ($Al(NO_3)_3{\cdot}9H_2O$) and monoethanolamine (MEA) were used as starting material, solvent, dopant and stabilizer,respectively, to coat onto silicon substrates. The ZnO thin film was deposited by thermal chemical vapor deposition (TCVD) technique where zinc acetate dehydrates (ZnAc) was used as a precursor and nitrogen as the carrier gas. The experimental result of the effect on the surface morphology and electrical properties of Zno thin films will be discussed.

II. Methodology

Generally this project consists of six steps which are substrates preparation, solution preparation, template preparation, thin film preparation, film annealing and characterization. The whole process of this project is simplified in the flow chart shown in Fig. 1.

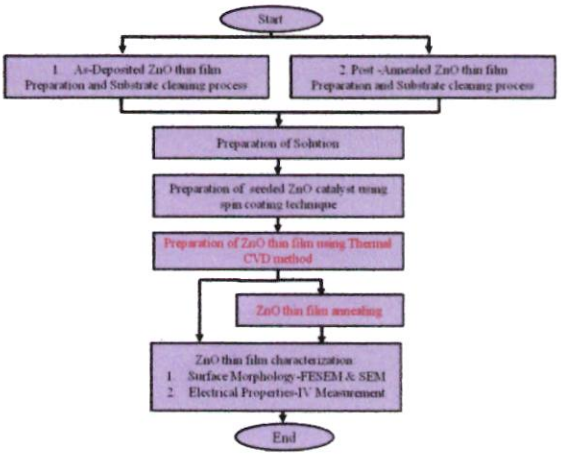

Fig. 1 : Flow chart of ZnO thin film experiment.

A. *Substrate Cleaning Process*

The substrate preparation involves 2 processes which are cutting and cleaning process. The substrate is cut using diamond wafer blade with the desired scale of 1cm x 1cm. The cleaning process is one of the important steps in this project because it affects the substrate properties and its performance. In this process, all the contaminants on the substrate are removed. Different substrate may have different cleaning technique so it is important to use the right cleaning technique to ensure the substrate is free from contamination. Silicon substrates are immersed with acetone and followed by ultra sonic cleaning method for 20 minutes. Then the acetone is discarded and replaced by new acetone. This step is repeated by replacing acetone with methanol and deionized (DI) water. Then the silicon substrates were etched with hydrogen fluoride (HF: H_2O at ratio 1:10) for 5 minutes and the process is repeated twice in order to remove the resistive native oxide layer formed over the surface [17]. Nitrogen gasses are then blown to the glass substrate to dry it.

B. *Spin Coating Technique*

The solution preparation stage involved four steps which are determination of material used, weighing, mixing, and solution stirring at 80°C and ageing 24 hours at room temperature. The material used to produce 0.4M ZnO solution is zinc acetate (ZnAc) as starting material, 2-methoxyethanol as solvent, aluminium nitrate ($Al(NO_3)_3{\cdot}9H_2O$) as dopant and monoethanolmine (MEA) as stabilizer.

ZnAc is dissolved in 2-methoxyethanol, aluminium nitrate and MEA for 100ml solution. 2-methoxyethanol is used to dissolved reactants and reagents and provides temperature control, either to increase energy of the colliding particles or to absorb heat that is generated during an exothermic reaction, while MEA is used to prevent colloids from aggregating and aluminium nitrate to increase the conductivity of the thin film. Solution are then stirred and heated at 80°C for 3 hours to increase reaction process between all the materials in the solution. The solution is then aged for 24 hours at room temperature to reinforce gel network and yield clear solution [18].

In the thin film preparation process, ZnO solution is deposited on the silicon substrate using spin coating technique. The solutions are dropped onto substrate while it is spun at the rate of 3000 rpm for 1 minute. Then the substrates undergo drying process. In this process the substrates is heated at 150°C for 10 minutes to evaporate solvent and eliminate organic component in the film [18]. This drop and dry process is repeated for 5 times to yield required thickness. The process is summarized in Fig.2.

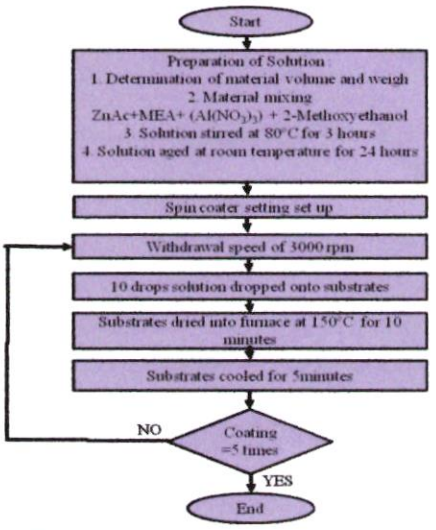

Fig. 2 : Flow chart of ZnO template preparation.

C. *Thermal CVD Method*

The growth of ZnO thin film was obtained by thermal CVD method which is performed in a horizontal furnace as shown in Fig.3.

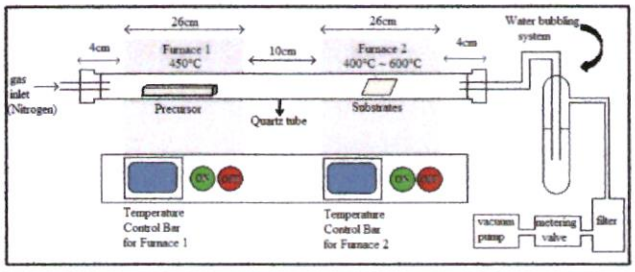

Fig. 3 : Thermal CVD (TCVD) apparatus.

The furnace holds a pre-heated quartz tube with a heated length of 70cm.Gases are taken from high pressure gas tanks without further purification and fed into the hot zone of the first furnace (Furnace 1) through gas inlet.Nitrogen is used as the carrier gas and also a dopant. A fraction of the carrier flow transport the ZnAc vapor into the second furnace (Furnace 2) . A water in gas bubbler cools the exhaust gas and serves as a condenser for gas phase reaction products.

D. *Thin Film Deposition Process*

ZnO thin films were carried out using a double furnace setup, one for heating the source material (precursor) and another for controlling the deposition temperature of the substrate, using nitrogen gas. Firstly, the quartz tube was cleaned with acetone and ethanol to ensure the tube is free from contamination. Secondly, the temperature is set for furnace 1 at 450°C (fixed temperature) and for furnace 2 the temperature is varied from 400 °C to 600 °C. In this process, zinc actate dehydrate were choosen as a precursor. After the desired temperature is achieved, the substrates and precursor were placed in the lamina boat and both were inserted into quartz tube to be heated together with nitrogen gas for 1 hour. The nitrogen gas pressure was selected at 0.4 bars at 0.001 LPM flow rate condition.

The last stage of thin film preparation is film annealing. In this stage the film was annealed in Proterm Furnace equivalent to the deposition temperature ranging from 400°C to 600°C. As-deposited was also prepared to compare the effect of surface morphology and electrical properties of ZnO thin film. As-deposited means the sample that does not experience annealing process after the TCVD process.

The film characterization stage involves surface morphology and electrical properties. The surface of the film were observed with field emission gun scanning electron microscopy (FESEM and the electrical properties are characterized using Solar Simulator measurement unit.

III. Results and Discussion

A. *Surface Morphology Analysis*

Fig.4 and Fig.5 below show the images for 5 different temperature samples of as-deposited and post annealed respectively using FESEM and SEM.Fig.4 shows that the size of ball for as-deposited is decreased from 1.52um to 1.20um while in Fig.5 for post-annealed the size also decreased from 1.31um to 1.21um when the temperature is increased.The thorn size increased from 40nm to 200nm for as-deposited and for post-annealed also increased from 27nm to 200nm with increased of temperature as shown.

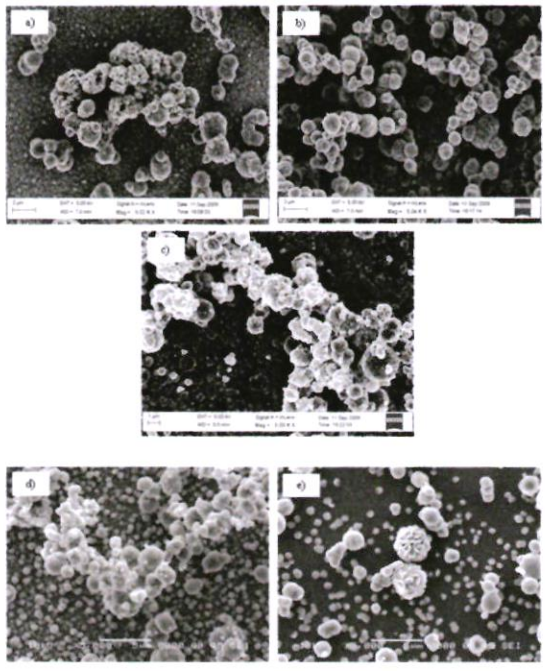

Fig. 4 : Images of the surface of ZnO thin films at magnification of 5K for as-deposited using FESEM a) 400°C, b) 450°C c)550°C and using SEM d) 500°C, e) 600°C.

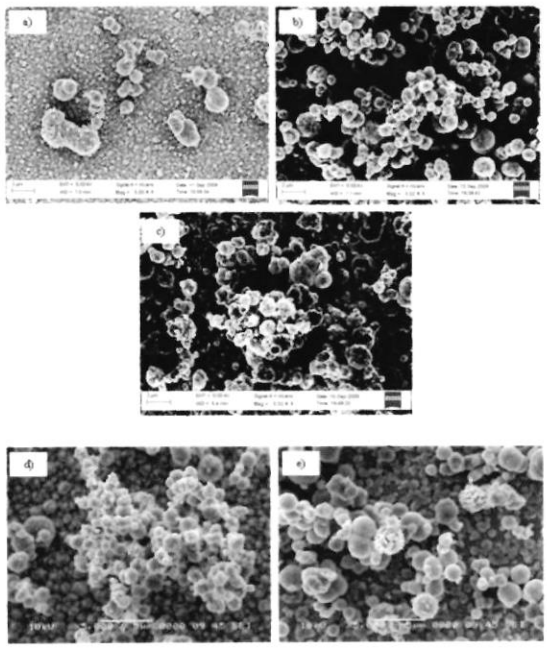

Fig. 5 : Images of the surface of ZnO thin films at magnification of 5K for post-annealed using FESEM a)400°C, b) 450°C c)550°C and using SEM d) 500°C, e)600°C.

From Fig. 4 and Fig.5 above shows that the microstructure become more smooth and more uniformity obtained in terms of particle ditribution at increasing temperature. It demonstrates that the quality of ZnO thin films was improved due to re-distributed of crystalline grain island has been joined into great crystalline surface[19].

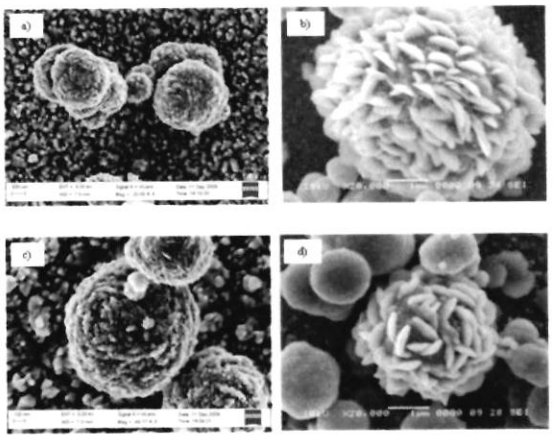

Fig. 6 : Images of the surface of ZnO thin films at magnification of 20K for as-deposited a) 400°C, b) 600°C and post-annealed c)400°C, d) 600°C.

The obvious change is that the thorn becomes more rough and bigger with increasing temperature especially for the post annealed ZnO thin film.This situation was shown in Fig. 6.

Post annealed temperature affects the particle interconnection i.e the interconnection between the balls increased when the temperature is increased.The size of ball and thorn had been simplify in Fig. 7 and Fig.8 below.

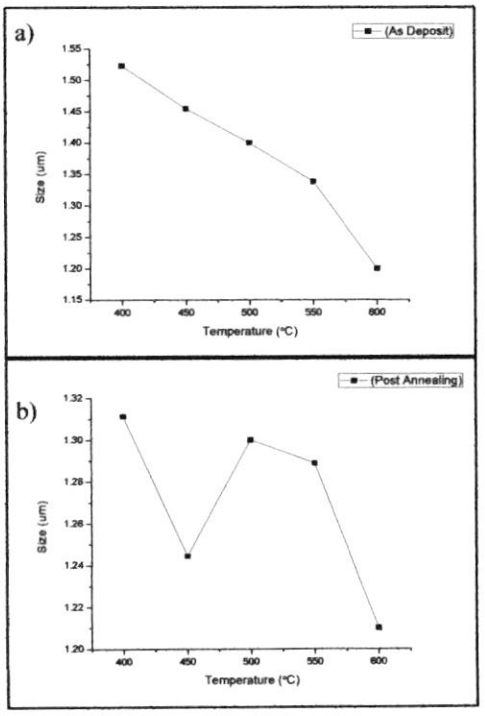

Fig. 7 : Diameter ball of ZnO thin film versus Temperature for a) As-deposited and b) Post-Annealed.

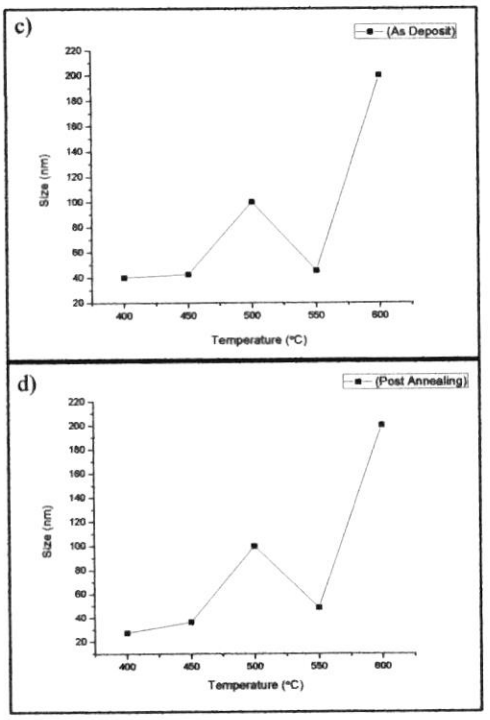

Fig. 8 : Diameter thorn of ZnO thin film versus Temperature for a) As-deposited and b) Post-Annealed.

B. *Electrical Properties*

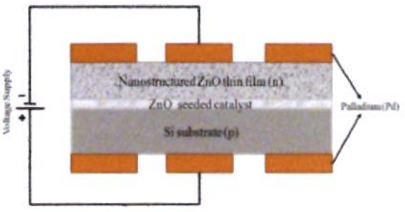

Fig. 9: Structure of ZnO thin film deposited on silicon substrate.

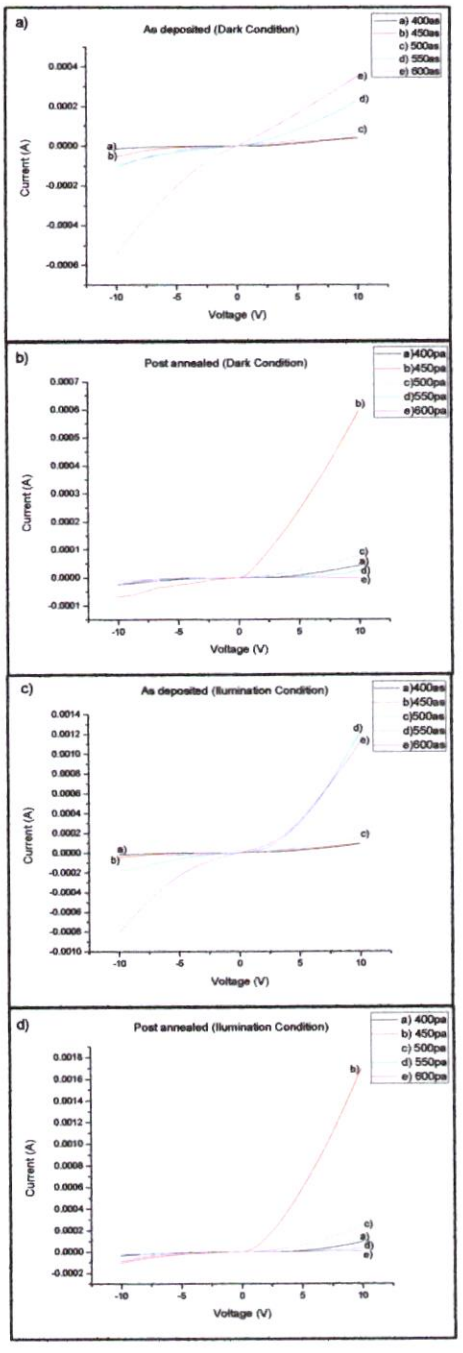

Fig.10 : The I-V characteristic of ZnO thin film for as-deposited and post-annelaed under a) and b) dark condition, c) and d)illumination condition.

The I-V measurement of ZnO thin films grown on silicon substrates were carried out by using Solar Simulator Test. The test was measured at room temperature under dark and illumination condition. Palladium (Pd) deposited onto ZnO thin film act as an electrode. The layer of ZnO thin films on the silicon substrate is as shown in Fig. 9. Two probes were tapped on the coated palladium in order to measure it electrical properties.

Fig. 10 shows the I-V characteristic of ZnO thin films for both as-deposited and post-annealed under dark and illumination condition. When voltage is applied, both electron and holes in the n-type and p-type material is pushed toward the junction. The holes recombine with electron at the junction hence increase the number of negative ion. This will leave the n-junction with less number of positive ions [20].Hence, decreasing the number of positive and negative ion at p-n junction. It results in the shrinking of the depletion region. As the applied voltage exceeds the internal electrical imbalance, current carriers of both types can cross the junction into the opposite ends of the crystal. The electrons in the p-type side attracted to the positive applied voltage, while holes in the n-type side are attracted to the negative applied voltage. This will generate a complete current path through the junction [20]. The current will flow and increase accordingly to the magnitude of the voltage applied to the circuit as in equation (1)

$$V=IR \qquad (1)$$

V = voltage (V)
I = current (A)
R = resistance (Ω)

Resistivity of ZnO thin films decreased when the resistance decreased (Refer to equation (2)).

$$\rho = RA / L \qquad (2)$$

A = film thickness x length of palladium (m_2)
L = length between palladium and palladium (m)
ρ = resistivity (Ωm)

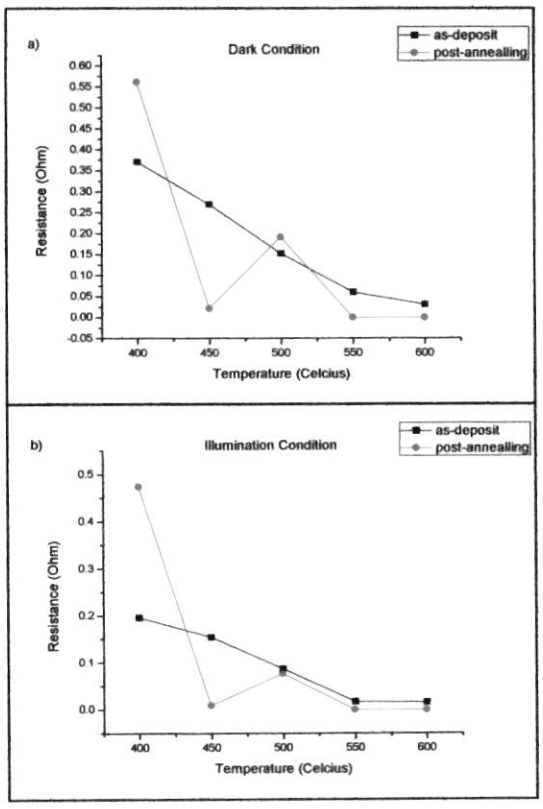

Fig. 11: The graph of resistance versus temperature of ZnO thin film for as-deposited and post-annealed under a) dark and b) illumination condition .

Fig. 11 shows the plotted result resistance versus temperature for both as-deposited and post-annealed. The parameter of A and L in equation 2 are assumed to be constant. Resistivity is decreased as resistance decreased. It can be concluded that resistivity of ZnO thin films decreased at higher temperature and post-annealed resistance is better than as-deposited. The number of Zn interstitial decreases with increasing temperature because the effect of Zn evaporation. ZnO contains numerous vacancies within crystal structure and it can accommodate interstitial atoms easily [19]. At above absolute zero, the lattice atoms are not always found in their lattice sites, it might participate and interfere with the directional electron movement. Thermal energy causes the atoms to vibrate about their equilibrium positions. At any moment in time many individual lattice atoms will be away from their perfect lattice sites and this interferes with electron movement [21].

$$G=1/R \qquad (3)$$

R=electrical resistance (Ω)
G=conductance (mho,S)

$$\rho = 1/\sigma \qquad (4)$$

σ = conductivity $(\Omega m)^{-1}$

ρ = resistivity (Ωm)

$$\rho=1/q\mu N \qquad (5)$$

ρ = resistivity (Ωm)
q = charge (1.602 x 10-19) (C)
μ = carrier mobility (cm^{-3})
N = carrier density (cm^2/s)

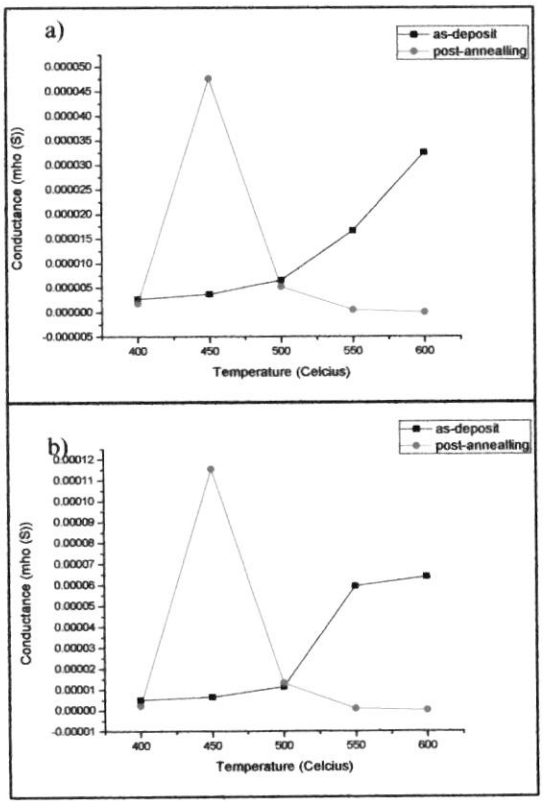

Fig. 12: The graph of conductance versus temperature of ZnO thin film for as-deposited and post-annealed under a) dark and b) illumination condition .

Fig.12 above shows the graph for conductance which is the reciprocal of electrical resistance (Refer to equation (3)). The graph shows electricity flows along a certain path through the ZnO thin film. It can be concluded that the conductance for as-deposited ZnO thin film under dark and illumination condition is increased while for post-annealed the conductance is decreased as the temperature increased. In other word, the conductance for as-deposited is better than post-annealed Zno thin film. But there is a slight increased in 450°C for post-annealed ZnO thin film.It shows that the resistivity is low but gives best conductivity.

The conductivity of ZnO thin films also reflects the carrier mobility of the film. That means when the conductivity is increased the resistivity is

decreased (Refer to equation (4)). Therefore, carrier mobility of the film is also increased when the resistivity is decreased (Refer to equation (5)).

IV. Conclusion

In conclusion, the surface morphology and electrical properties of ZnO thin films deposited on silicon substrate by using TCVD technique at various temperatures were studied by using FESEM/SEM and Solar Simulator Test. From the structural properties, there are correlation between the deposition/annealed temperature and the surface morphology. The high resolution FESEM and SEM showed that evolution of deposition/annealed temperature from 400°C to 600°C influenced the crystalline structure of ZnO. Besides, the nano structured of thorn grown on ZnO thin film for both as-deposited and post-annealed was demonstrated. The deposition/annealed temperature also influenced to the electrical properties of the ZnO thin films. From a graph of I-V curve it can be concluded that all films deposited/annealed on silicon substrate exhibited ohmic contact. The I-V curves show decreased in the resistance for post annealed (dark: from 561.61kΩ to 0.02kΩ, illumination: 473.93kΩ to 0.01 kΩ) while increased in the conductance for as deposited (dark: from 2.70E-6 mho to 32.52E-6 mho, illumination: 5.10E-6 mho to 63.94E-6 mho) as temperature is increased. This indicates that as the temperature is increased from 400°C to 600°C the resistivity of ZnO films is decreased and the conductivity is increased. The conductance for as-deposited is better than post-annealed ZnO thin film.

V. Future Development

A dopant of aluminium nitrate will be added to enhance the conductivity of the ZnO thin film by using three reactor furnace method instead of sol-gel method.

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