High Speed 4-bit Flash ADC with low INL and DNL Using 0.18µm CMOS Technology

Azrin Bin Wasli
Faculty of Electrical Engineering
Universiti Teknologi MARA
Shah Alam, 40450, Selangor, Malaysia
e-mail: yoztheelectrical@gmail.com

Abstract— **The purpose of this paper is to design a High Speed 4 -bit Flash Analog to Digital Converter (ADC) with low Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). A high speed Flash ADC is obtained by selecting the best topology for the comparator and encoder design. In this paper, the best topology used for the analogue side is the open-loop comparator replacing the conventional comparator. However, some modification is made on the comparator which is by adding hysteresis circuit. The purpose is to lower the non-linearity effect on the output of the ADC. Meanwhile, for the digital side, the best topology used to design the flash ADC is the XOR encoder. The technology used to design this ADC is 0.18µm CMOS technology. The software that is used to design this Flash ADC is Silvaco Electronic Design Automation (EDA) Tools. This includes schematic-drawings, simulations, layout-designs, and overall checking of the circuit. Summarizing the simulation results includes a lower delay comparator design which is 0.2569ns at maximum sampling frequency of 500MHz with analogue input of 1.8V. The simulation of the XOR encoder shows that the topology has the lowest power consumption which is 1.5343mW with a propagation delay of 25.4890ns. The overall DNL for this flash ADC ranging from -0.4LSB ~ 0.3LSB and the INL ranging from -0.6LSB ~ 0.4LSB. Simulation also shows an ADC power consumption of 38.8072mW and a propagation delay of 58.44ns for a 1.8V supply.**

Keywords-component; Flash ADC, Open-loop Comparator, hysteresis circuit, XOR Encoder, DNL, INL, low nonlinearity error

I. INTRODUCTION

Nowadays, in this modernity-growth world, humans are increasingly relying on high-tech gadgets. Hence, demands on the high quality yet simple and user-friendly gadget is becoming a complex challenges for the gadget producers. Since vast majority of signal processing is done digitally, while signal in nature is analogue, synchronization between these two types of signal is highly needed. This is where data conversion becomes important. To convert this analogue signal into digital that can be processed by the digital signal processors, Analog-to-Digital Converter (ADC) is needed [1]. In a high-rate data transfer communication environment, the conversion of data especially in ADC is the key to the perfection of communication between two sides (sender and receiver) which can be found in almost every modern mixed-signal integrated circuit [2]. Hence, a deep study and research is carried out to improve the ADCs performance.

The pipelined ADC is one of the most common ADC architecture nowadays. The advantage is it can achieve high resolutions and conversion rates, while having intermediate power consumption. The performance of the ADC depends on its resolution and speed. The ADC resolution will degrade because of some factors such as nonlinearity errors and noise and that is why the output resolution of the ADC usually less than the designed resolution [1]. Flash ADC is one of the important parts in pipelined ADC. It consists of comparator on the analogue side and encoder for the digital side. Due to the parallel structure of the flash ADC, data conversion can be done faster [3].

This paper presents the design of a high speed 4-bit flash ADC, with better delay and lower nonlinearity (INL and DNL) compare to the previous research on [2]. There is some modification to the comparator part of the flash ADC which will be the main part of study of this paper. Open-loop comparator is added with the hysteresis circuit to remove the instability output of the comparator especially in noisy environment. For the digital part, the XOR encoder topology is used to encode the thermometer code into binary code.

II. DESIGN OF FLASH ADC

A. Flow Chart of the Project

The design step of the 4-bit flash ADC is shown in Figure 1.

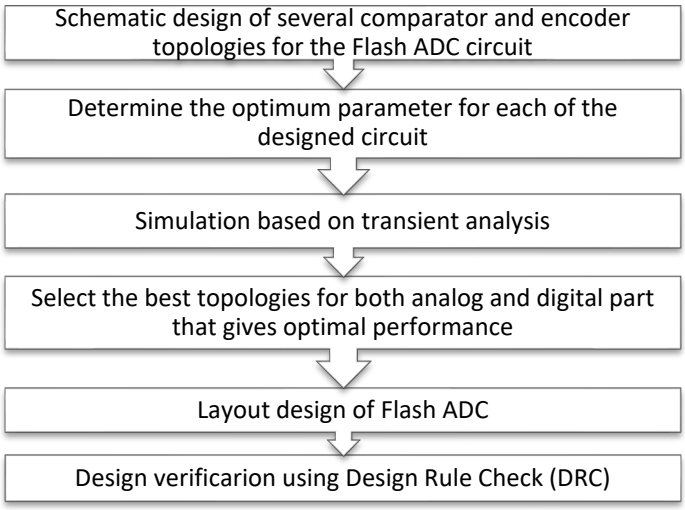

Figure 1. The design step of the 4-bit flash ADC

B. *Flash ADC*

The advantage of the flash ADC architecture is it is ideal for applications requiring very large bandwidth. Generally, this architecture achieves the highest sampling rate for high speed conversion. The performance of the embedded comparator typically determines the maximum sampling speed [4]. However, due to its parallel structure, where the number of comparator used in one flash ADC is 2^n-1 (n = number of bits), it typically consumes more power than other ADC architectures [2]. Reference voltage for each of the comparator is differentiates by the resistive ladder structure of the flash ADC. The number of resistor used in the resistive ladder is 2^n. The value of reference voltage at each level is differ by one least significant bit (LSB) with the top one is always greater than the one below it [3].

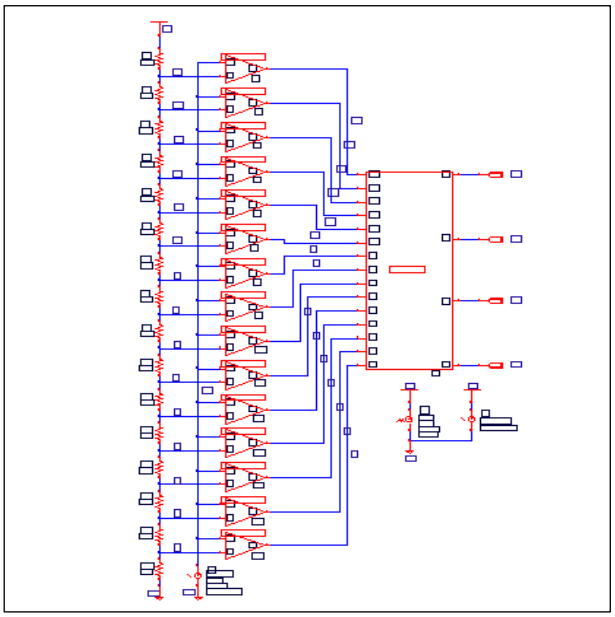

Figure 2. 4-bit flash ADC

C. *Comparator*

Comparator compares the voltage between both of its input. Usually, one of the inputs is set to be reference voltage meanwhile the other one is the input voltage from other source. The outcome/output depends on the comparison between both inputs. When analogue input voltage is greater than the reference voltage, the output will become '1'. Contrarily, when analogue input voltage is lower than the reference voltage, the output will become '0'. In the flash ADC architecture, the 2^n-1 comparators outputs are channelled to the input of the encoder in form of thermometer code [3]. Hence, in a high speed operation, sampling the input signals for every clock cycle in a parallel structure of the comparators increases the power consumption of the whole flash ADC [5]. There are 3 types of comparator that is compared in this paper which are conventional comparator, open-loop comparator and open-loop comparator with hysteresis circuit.

1) *Conventional Comparator*

There are 21 transistors used to build up the conventional comparator as shown in Figure 3. It consists of three stages which are an input preamplifier, a latch and an output buffer. Preamplifier circuitry is needed in this design as it is not suitable for a high resolution operation [2]. To amplify the signal coming from the latch while providing enough current to the load, the output buffer is needed [6].

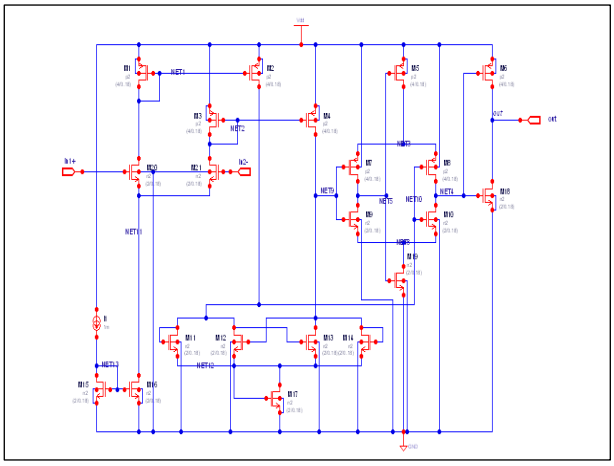

Figure 3. Conventional comparator

2) *Open-loop Comparator*

There is less number of transistors used to design the open-loop comparator. This means less delay and less power consumption for a single comparator. Besides, the open-loop comparator circuit area is small because of minimal number of transistors [7]. It consists of three stages which are input stage, push-pull inverter and output stage as shown in Figure 4.

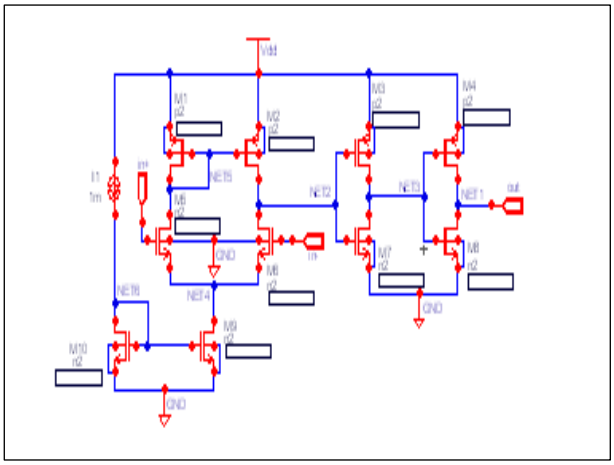

Figure 4. Open-loop comparator

3) *Open-loop Comparator with Hysteresis Circuit*

Open-loop comparator with hysteresis circuit is designed to improve the output of an open-loop comparator in the previous work in [2] which will lead to better overall output of the flash ADC mainly in term of its noise and errors (INL and DNL) by removing unwanted jitter. Hysteresis circuit is added externally to the open-loop comparator with some form of positive feedback as in Figure 6. The purpose is to improve the stability of the output especially in a noisy environment [6]. If the comparator sampling speed is high and the amplitude of noise is great enough, the output will have a

lot of faulty or noise. The idea is to have the threshold voltage level at the lower and upper trip of the input signal before it is converted as shown in Figure 8.

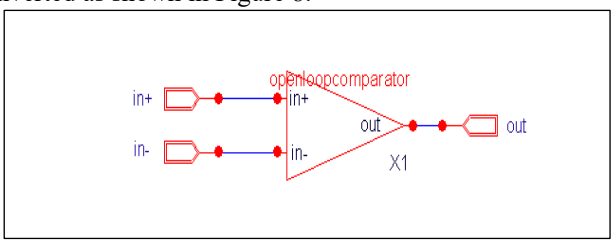

Figure 5. Open-loop comparator with no hysteresis circuit

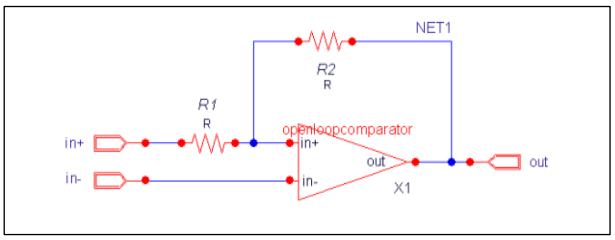

Figure 6. Open-loop comparator with external hysteresis circuit

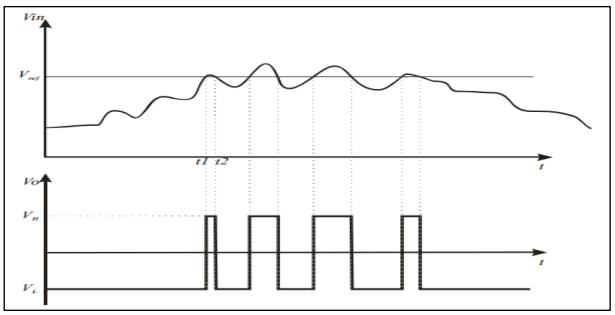

Figure 7. Output of normal open-loop comparator

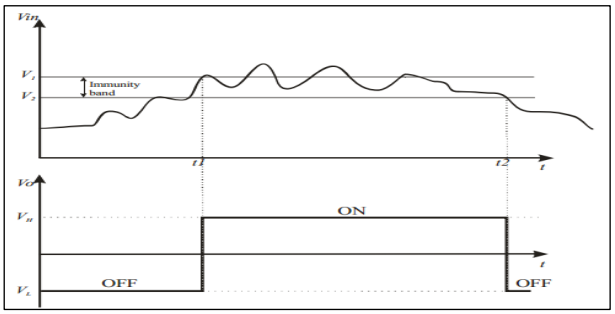

Figure 8. Output of open-loop comparator with hysteresis circuit

In particular, the output changes when the input signal passes the threshold level. Then, the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the output of the comparator changes state again. When the input starts negative and goes positive, the output remains until the positive trip point T is reach as shown in Figure 9. As the output goes high, the effective trip point changed to -T. The output will only change again after it reaches this negative trip point [6]. The transfer curve shown in Figure 9 is called counterclockwise bistable characteristic because of the non-inverting input.

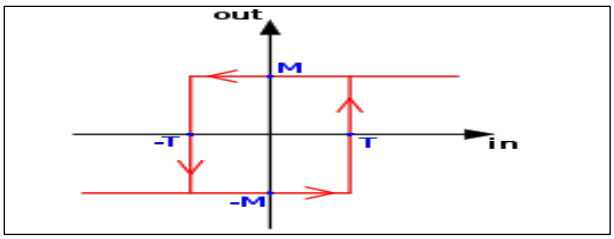

Figure 9. Comparator transfer curve with hysteresis

The positive trip point, T can be found by

$$T = -\frac{R_1 V_L}{R_2} \quad (1)$$

Meanwhile, the negative trip point, -T can be found by

$$-T = -\frac{R_1 V_H}{R_2} \quad (2)$$

The width of the bistable characteristic is given as

$$\Delta V_{in} = T - (-T) = \left(\frac{R_1}{R_2}\right)(V_H - V_L) \quad (3)$$

*note; in most of the reference books, T is refer as V_{TRP}^{+}, while –T is refer as V_{TRP}^{-}.

D. Digital Encoder

The function of digital encoder is to process the data received from the output of the comparator which is in form of a thermometer code into binary code. There are three types of digital encoder topologies being compared which are NOR Based ROM array encoder, XOR encoder and Wallace Tree encoder. Each of the encoder has different type of configuration and circuitry. The performance for each of it will be assessed based on its power consumption and the propagation delay where the best and suitable one will be chosen as the digital encoder for the flash ADC.

1) NOR Based ROM Array Encoder

The structure of a NOR based ROM array encoder is shown in Figure. 10. It is used to convert 1-out-of-n code to binary code. The sole purpose it was developed is to achieve high speed conversion. The operation is quite simple. The PMOS will always be in ON state as the gate voltage of it always connected to ground. Whenever the output of AND gate is zero or low, all of the NMOS in a same row will be turned OFF. Hence, the column voltage is pulled high by the PMOS load device producing high output at the corresponding encoder output bit. Contrarily, if the output of AND gate is high, the NMOS in the same row will be ON and the column voltage is pulled down producing low output at the corresponding encoder output bit. In flash ADC, the ROM speed is predominant factor of the overall ADC speed. This encoder depends too much on ROM input hence taking too much time to complete single conversion [2].

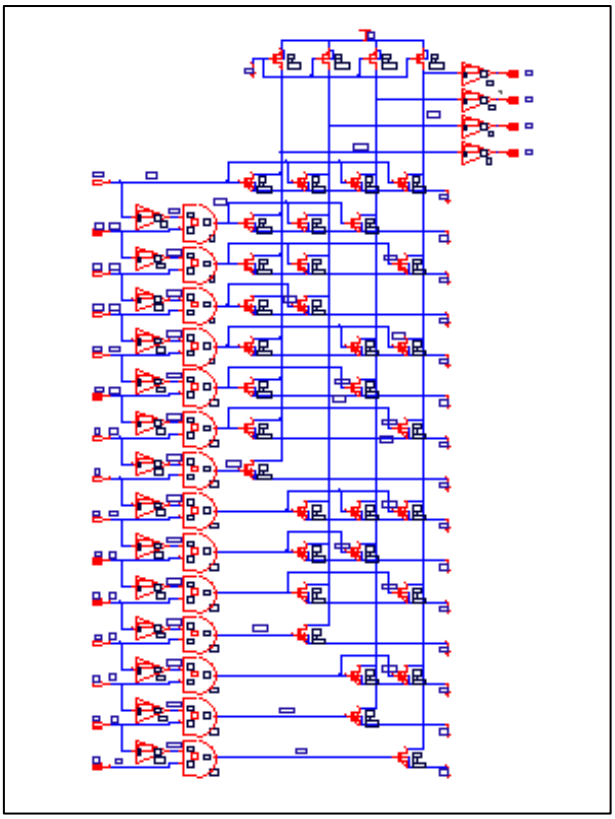

Figure 10. 4-bit NOR based ROM array encoder topology

2) XOR Encoder

The structure of XOR encoder is as shown in Figure 11. This encoder is designed by reducing and simplifying the logic function of the original encoder. Hence, wire crossings and delays are reduced [2]. It was designed mainly to minimize the effect of metastability and bubble errors. This is done by choosing gray code as an immediate code which only changed 1-bit form one code to the next. Main component that build up this encoder is XOR gate since it can be used to replace the AND/NAND gates due to the special format of the thermometer code itself. This can be proven by examining the Boolean equation below;

$$T_7 \cdot \overline{T_9} = T_7\overline{T_9} \tag{4}$$

$$T_7 \oplus \overline{\overline{T_9}} = T_7\overline{T_9} + \overline{T_7}T_9 \tag{5}$$

*note; refer to Figure 12 for (4) and Figure 11 for (5)

Due to the special format of thermometer code where only 1-bit is changed from one code to the next, assume that $\overline{T_9}$ is 0, while T_7 is 1. Product of this two will produce output 0. For the XOR gate, the summation of $T_7\overline{T_9}$= 0 and $\overline{T_7}T_9$= 0 will also produces output 0. It is proven to be similar.

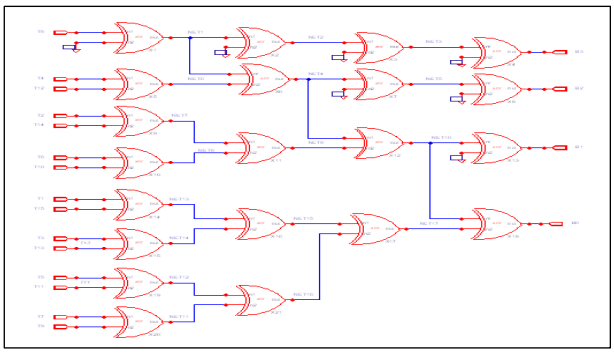

Figure 11. 4-bit XOR encoder topology

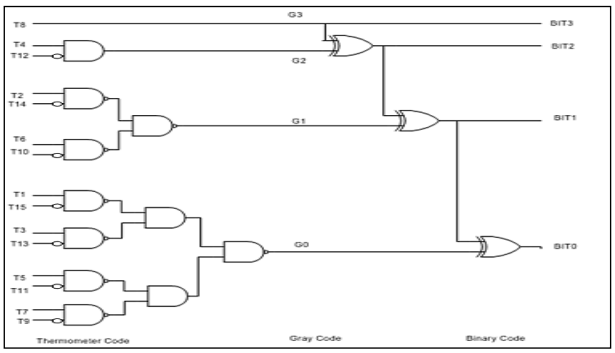

Figure 12. The AND/NAND gate version of XOR encoder

3) Wallace Tree Encoder

The Wallace Tree encoder is as shown in Figure. 13. This designed is originally used to implement high speed multipliers in computer arithmetic units since it is the most efficient. It is used because it can correct higher order bubbles. It is used along with the thermometer code in Flash ADCs where the number of "1's" is counted, instead of the 0↔1 transition being determined [2]. Main component that build up this encoder is full adder circuit. The disadvantage of this encoder design is the number of cells is doubled due to the tree structure. One stage need to be added for every 1 bit increase in resolution. This means the area becomes bigger.

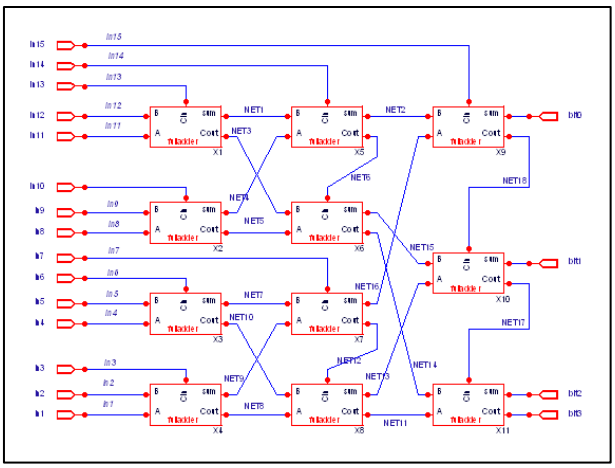

Figure 13. 4-bit Wallace Tree encoder topology

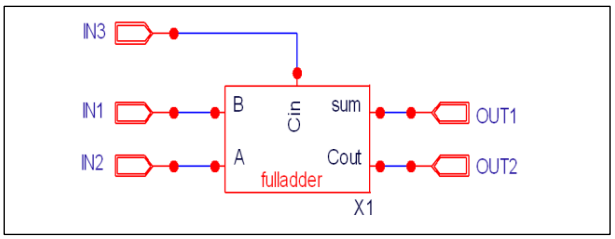

Figure 14. Full adder implemented in Wallace Tree encoder

III. Simulation Results and Discussions

The Flash ADC in this paper is designed using 0.18µm CMOS technology. The ADC is supplied with 1.8V with a bias current of 1mA for all gates in the comparator circuit.

A. Comparator Result

The three selected comparator topologies is tested and assessed in term of maximum sampling speed, power consumption, and propagation delay. Tested frequency ranging from 100 MHz to 500 MHz with the same parameter set for the input voltage (1.8V), reference voltage (0.45V), supplied voltage (1.8V), biased current (1mA) and the temperature (27 ^{O}C). The simulation is running using transient analysis which is with respect to time. The input signal that is used for this simulation is a continuous sinusoidal waveform signal. The output waveform for the open-loop comparator with hysteresis circuit is as shown in Figure 15.

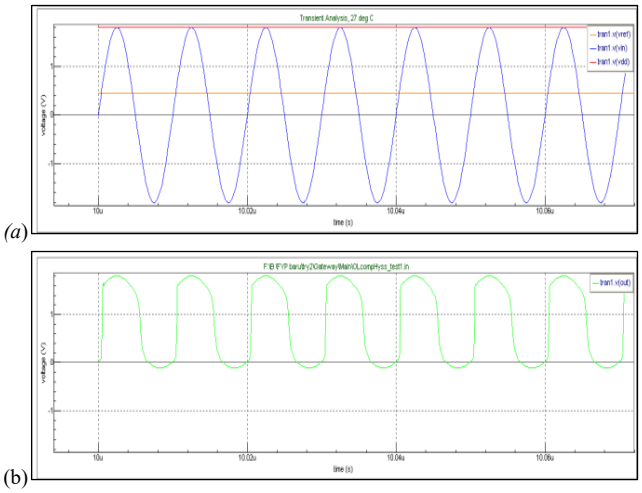

Figure 15. Output for open-loop comparator with hysteresis circuit at 100MHz; (a) $V_{IN,}$ V_{dd} and V_{ref} signal, (b) V_{out} signal

The output waveform seems uniform because the input signal that is supplied is also uniform. However, in real environment, other devices or signals might interrupt the original input signal. Hence, the converter needs to be highly precise and accurate. That's why the hysteresis circuit is needed to cope with this problem. From each of the graph, it can be seen that every time the input signal passes through the reference signal, the output signal will change with some delay. The rest of the results from the simulations are summarized in Table 1, Table 2, and Table 3.

TABLE I. OUTPUT RESULTS FOR CONVENTIONAL COMPARATOR

Frequency (MHz)	Average Power (mW)	Tphl (ns)	Tplh (ns)	Tp (ns)
100	2.8400	0.4104	9.7581	5.0843
200	2.8789	0.2377	4.8949	2.5663
500	2.9961	0.1328	1.9921	1.0625

TABLE II. OUTPUT RESULTS FOR OPEN-LOOP COMPARATOR

Frequency (MHz)	Average Power (mW)	Tphl (ns)	Tplh (ns)	Tp (ns)
100	3.0111	0.5245	9.8279	5.1762
200	3.1702	0.3227	4.9876	2.6552
500	3.9231	0.2135	0.6669	0.4402

TABLE III. OUTPUT RESULTS FOR OPEN-LOOP COMPARATOR WITH HYSTERESIS CIRCUIT

Frequency (MHz)	Average Power (mW)	Tphl (ns)	Tplh (ns)	Tp (ns)
100	3.641	0.2475	2.0289	1.1382
200	3.8853	0.1467	1.1299	0.6383
500	4.2301	0.1130	0.5949	0.3534

From the obtained data, the power consumption for all of the topologies ranging from 100MHz to 500MHz is around 2.84mW to 4.2301mW. The relation between frequency and power consumption is as shown below.

$$P \propto V_{dd}^2 f \tag{6}$$

P is the dynamic power consumed by a CMOS device, V_{dd} is the supply voltage, and f is the clock frequency [8]. Basically, based on the above relation, power consumption will increase if the sampling frequency for the circuitry is increase. Open-loop comparator with hysteresis has the highest average power consumption, followed by the normal open-loop comparator, and the lowest one is the conventional comparator.

Based on the results, it can be seen that the propagation delay for each of the topologies decrease with increment in frequency. Frequency and time can be relate using this formula,

$$f = \frac{1}{T} \tag{7}$$

Frequency is inversely proportional to time. So, logically, whenever frequency is increased, the time taken will reduced. This means the propagation delay will decrease [6]. Among all of the topologies, the open-loop comparator with hysteresis circuit generates the lowest propagation delay with as low as 0.3534ns at sampling frequency of 500MHz.

To conclude, the best comparator topology to be chosen for this paper flash ADC is open-loop comparator with hysteresis circuit. Although it consumes more power than the other compared comparator topologies, the main thing that is being aim in this paper is to have a high speed flash ADC. Other power reduction technique can be implemented to balance between the power consumption and high sampling frequency circuit such as using latched comparator which will

make the comparator consumes power only when the circuit needs to be operated. Another advantage of this comparator is the ability to operate optimally in a very noisy environment. The uniform waveform used to test the circuit can't simulate the true purpose of the circuit.

B. Encoder Result

There are three types of encoder being simulated which are NOR based ROM array encoder, XOR encoder, and Wallace Tree encoder. These circuits are tested using digital input signal which is square-wave signal. 4-bit means that the encoder has 15 inputs (2^N-1) and 4 outputs. All of the circuit is assessed in term of power consumption, and propagation delay. The simulation is running using transient analysis which is with respect to time. The output of the encoder is in the digital form which is in square-wave form. The high output is encoded as '1' while the low output is encoded as '0'.

The measurement of the propagation delay from low-to-high and high-to-low is a bit different for these encoder simulations. This is because the input signal is set to produce a signal that only step once which is to simulated the thermometer structure of the flash ADC. Basically, once the first input changed from '0' to '1', it will remain '1' until all of the 15 inputs already changed its states accordingly. Therefore, the tplh of the circuit can be found same as comparator circuit. The tphl of the encoder is found by setting the starting point of the first marker at the input signal (transition from '0' to '1') and the second marker at the transition from '1' to '0' of the bit0 (output signal).

The output waveform for the XOR encoder is shown in Figure 16.

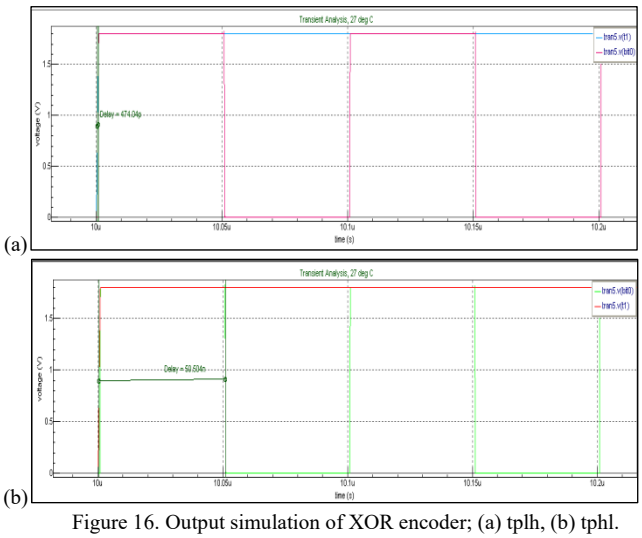

Figure 16. Output simulation of XOR encoder; (a) tplh, (b) tphl.

The output results for the propagation delay and the power consumption for each of the encoder topology is as shown in Table 4.

TABLE IV. OUTPUT RESULTS FOR THE ENCODERS

	ROM Encoder	**XOR Encoder**	**Wallace Tree Encoder**
Power	5.5688 mW	1.5343 mW	1.9238 mW
Tplh	264.32 ps	474.04 ps	631.91 ps
Tphl	50.124 ns	50.504 ns	50.627 ns
Tp	25.1942 ns	25.4890 ns	25.5629 ns

From the obtained result, it is seen that the delay for every topology is almost the same where only a little difference exist. It will not give a high impact because this study will only focus on using a single type of encoder for a single flash ADC. The combination of two or more encoder is not implemented in this paper. Therefore, the delay which is about 25ns to 26ns will not have a big difference between each of the topology. However, the propagation delay of the three topologies is considered good and it still provide the flash ADC with a high conversion rate. When it comes to comparing the power consumption of the three topologies of the encoder, a big difference can be seen from one another with the lowest power consumption among all is the XOR encoder which is 1.5343mW.

To conclude, the best topology that is chosen for the digital side of the flash ADC is XOR encoder. This is due to the minimum power consumption as compared to the other type of encoder. In term of speed, all of the encoder shows good results but the dominant picks is still the XOR encoder topology.

C. Full Flash ADC Result

The full flash ADC that is used in this paper consists of the open-loop comparator with hysteresis circuit on the analog part and the XOR encoder on the digital part. The full flash ADC it simulated using supply voltage of 1.8V. The reference voltage values are varied by the resistive ladder structure of the flash ADC. The value for the reference voltage at the non-inverting input of the comparator is 1 LSB starting from the most bottom comparator and increasing by 1 LSB as it goes up (refer to Figure. 2 for full view of the flash ADC structure). The value of 1 LSB can be calculated using

$$LSB = \frac{V_{ref}}{2^N} \tag{8}$$

For this flash ADC with N = 4 (N = number of bit), 1 LSB is equal to 0.1125 V which means for every single step of 1 LSB, the value of voltage will change at 0.1125 V [6]. The important results that need to be take into consideration in simulating this flash ADC is its DNL and INL. The result of the proposed 4-bit flash ADC simulation is as shown in Figure 17.

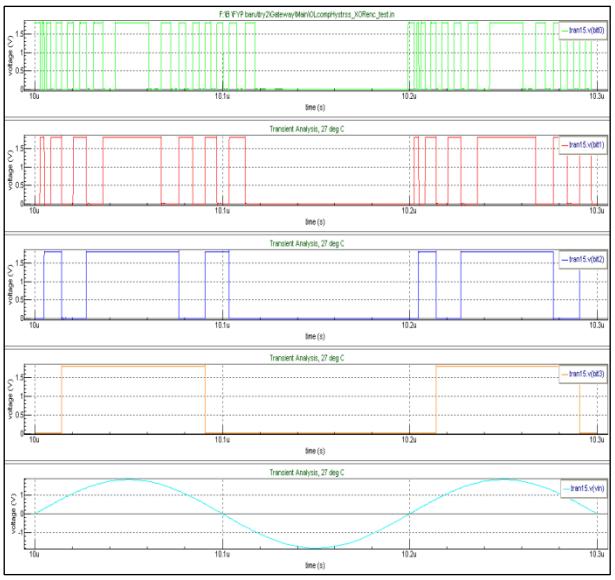

Figure 17. Simulation results for the proposed 4-bit Flash ADC

By referring to Figure 17, the sinusoidal waveform with cyan color is the input voltage, V_{in}. The orange, blue, red, and green square-waveform is the output of the flash ADC which is bit3, bit2, bit1, and bit0 respectively. The outputs represent the digital output code such as 0001, 0010, 1010, and so on.

1) Differential Non-Linearity (DNL)

The differential nonlinearity of an ADC is defined as the difference or measure of the separation between adjacent codes measured at each vertical step in percent or LSBs [6]. It can be written as

$$DNL = (D_{CX} - 1)\ LSBs \qquad (9)$$

D_{CX} is the size of the actual vertical step in LSBs. The result from the simulation of the flash ADC is transferred into a plotted graph as shown in Figure 18.

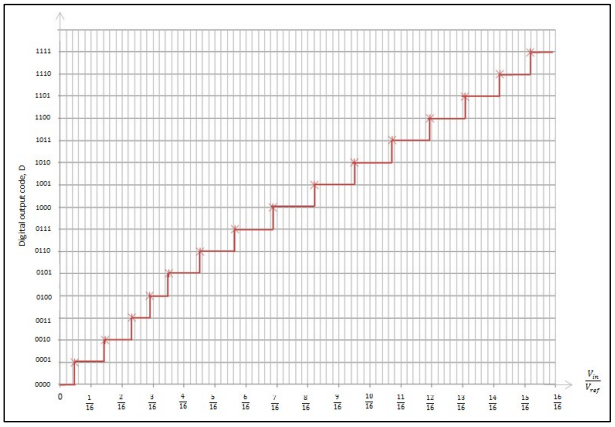

Figure 18. Transfer curve for proposed flash ADC

The transfer curve for the proposed flash ADC is drawn by taking consideration of the ideal characteristic being shifted 0.5 LSB backward [6]. When the ideal characteristic is shifted, the actual characteristic also follows. From the transfer curve of the flash ADC, the quantization error that illustrating the DNL is plotted and can be seen in Figure 19.

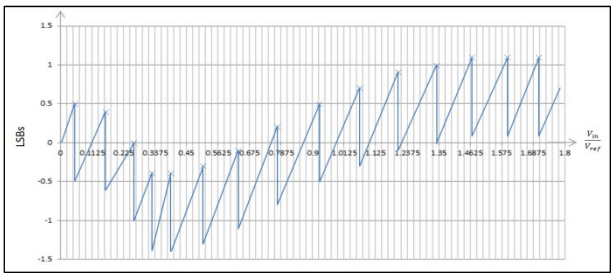

Figure 19. Quantization error illustrating DNL

From the formula in (9), the DNL of the flash ADC is calculated. DNL at 0 (DNL_0) is equal to zero since the ideal step width of the 0000 transition is ½ LSB. The step widths associated with 0001, 0101, and 1110 are equal to 1 LSB. Hence, DNL_1, DNL_5, and DNL_{14} are zero.

$$DNL1 = DNL\ 5 = DNL14 = 0\ LSB$$

The overall DNL for this flash ADC ranging from -0.4LSB ~ 0.3LSB. The quantization error worsens as the DNL increase in either direction [7]. Hence, from the overall results, a DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes.

2) Integral Non-Linearity (DNL)

The integral nonlinearity of an ADC is defined as the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically in percent or LSBs [6]. INL is measured by drawing a straight line through the end point of the first and the last code transition of ideal characteristic. Then, the difference between the maximum actual characteristic and the drawn straight line is measured. If any of the maximum actual finite resolution characteristic touches the ideal finite resolution characteristic line, the INL of the flash ADC is equal to zero. Hence, no error or noise affects the digital output code of the flash ADC at that point. If the actual finite resolution appears to be over the top of the ideal finite resolution line, the INL will have a negative value. Contrarily, when the actual finite resolution appears below of the ideal finite resolution line, the INL will have a positive value. The INL transfer curve of the flash ADC with the mentioned straight line is as shown in Figure 20.

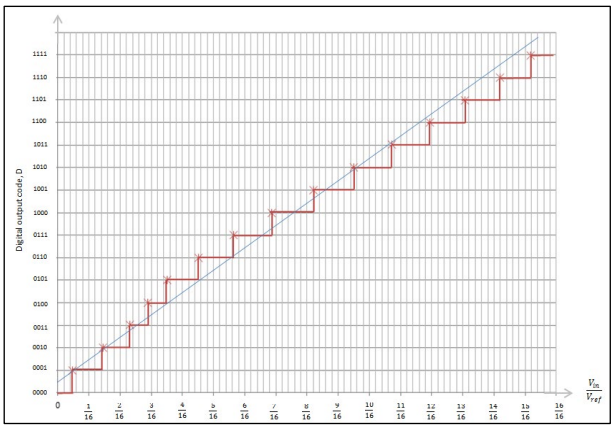

Figure 20. Transfer curve of the flash ADC with a straight ideal characteristic line for measuring INL

From the obtained data and plotted graph, the INL of the ADC is calculated. The step widths associated with code 0001, 0010, and 1010 occur on the best-fit line. So,

$$INL1 = INL2 = INL10 = 0\ LSB$$

The overall INL for this flash ADC ranging from -0.6 LSB ~ 0.4 LSB.

D. Comparison With Previous Work

The important parameter that is compared from this paper with the previous work in [2] is the speed of the designed Flash ADC and the DNL and INL. The flash ADC is tested to operate at the maximum sampling frequency 500MHz at the temperature of 27 ˚C. The full comparison of the current work with the previous one is as shown in Table 5.

TABLE V. OUTPUT RESULTS OF THE SIMULATED FLASH ADC

	Flash ADC	
	Previous work in [2]	**Proposed design**
Technology	0.18 µm	0.18 µm
Power Supply	1.8 V	1.8 V
Resolution	4-bit	4-bit
Maximum Sampling Speed	500 MS/s	500 MS/s
Temperature	27 ˚C	27 ˚C
Power Consumption	24.2662 mW	38.8072 mW
Tphl	135.7 ns	109.65 ns
Tplh	3.52 ns	7.23 ns
Tp	69.61 ns	58.44 ns
DNL	-0.8LSB ~ 0.5LSB	-0.4LSB ~ 0.3LSB
INL	-0.5LSB~0.8LSB	-0.6LSB ~ 0.4LSB

The previous work in [2] used the open-loop comparator topology on the analog side while the XOR encoder on the digital side. The proposed new flash ADC which is being study in this paper used the same comparator topology but with some modification which is by adding hysteresis circuit. The encoder still remains the same which is XOR encoder. The power consumption of the proposed flash ADC increased which is from 24.2662mW to 38.8072mW. However, the propagation delay and the DNL and INL of the proposed ADC has a lower values compared with the previous work.

IV. CONCLUSION

As a conclusion, the best topology chosen is the open-loop comparator with hysteresis circuit and the XOR encoder. The chosen comparator has a better speed compared to other comparator topologies but with some trade-off in power consumption. The XOR encoder is chosen because of its low power consumption. The total power consumption of the proposed flash ADC is considerably high. However, some trade-off in power makes the designed flash ADC operate faster with a lower propagation delay which is 58.44ns. One of the objectives of this paper which is to design a flash ADC with lower INL and DNL is achieved. The proposed flash ADC operate with lower INL and DNL which are -0.6LSB ~ 0.4LSB and -0.4LSB ~ 0.3LSB respectively. For future development, the design of the flash ADC can be further improve by applying the 90nm technology, or testing and choosing more variety type of comparator and encoder circuit.

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