Study the Effect of Butterworth Filter's Order on the Ideal Filter Approximation for Butterworth Low Pass Filter.

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Abstract- **This paper presents the study and analysis on Butterworth Low Pass filter, to discover the filter's order effect on the ideal filter approximation. Theoretically, as the numbers of order increased, the filter will approximate ideal filter characteristics. The challenges are; by increasing the filter's order, it will increase the circuit complexity and the cost. In order to reduce the circuit complexity, the Sallen-Key topology has been selected since the topology requires fewer components. This paper also presents the techniques and issues that should be considered while designing the schematic and layout of the filter.**

Key Words: Butterworth Low Pass Filter; number of order; ideal filters approximation; Silvaco GATEWAY; Silvaco EXPERT.

I. INTRODUCTION

The Butterworth filter is commonly referred to as a maximally flat or flat-flat filter while the low pass filter is describes as a filter which passes low frequency signals, and rejects signals at frequencies above the filter's cut-off frequency.

The filter will approximate ideal filter characteristics by increasing the number or filter's order**.** The degree of passband flatness increases as the order N is increases and as the order N is increased the filter response approaches the ideal brick-wall type of response [1]. Thus, the complexity or filter type is determined by the filter's order.

It also known that the roll-off rate and therefore the width of the transition band depend upon the order number of the filter and that for a simple 1st-order filter it has a standard roll-off rate of 20dB/decade. As numbers of order increased by one, the roll-off rate will increased by 20dB/decade. It will result in the increases of filter approximation toward ideal filter characterization since the filter roll-off rate has been increased.

There are various types of filter topologies. As for this study, the Sallen-Key topology is used due to the simplicity of the designs. Sallen-Key is represented as second order filter. There are four different designs available in Sallen-Key topology. But the design that will be taking into consideration is Sallen-Key equal components since both resistors and capacitors are assumed to be equal.

Higher order filters can be realized by cascading lower order filters [2]. Cascading filters for even and odd numbers of order might be different. Figure 1 below shows the cascading of filter stages up to the sixth order. A filter with an even order number consists of second-order stages only, while filters with an odd order number include an additional first-order stage at the beginning [3].

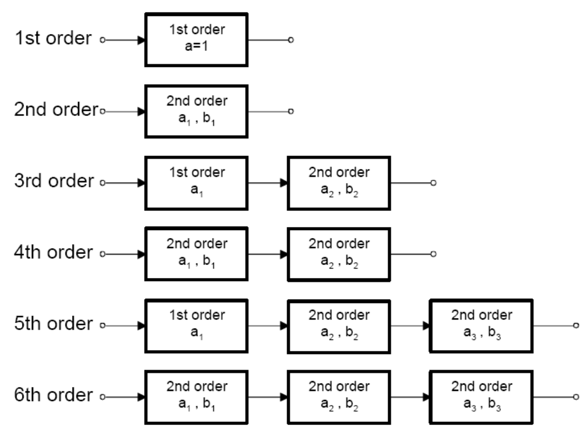

Figure 1. Cascading Filter Stages for Higher-Order Filters.

Another way to cascade the odd numbers filter for higher order is; the last pole can be added with a simple passive filter at the output of the active filter as shown in Figure 2 [2].

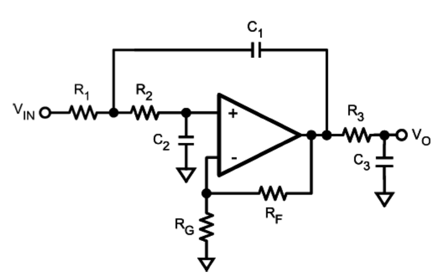

Figure 2. 3rd order Sallen-Key Filter

There are some issues and techniques that should be taking into consideration while design the layout. Because the Butterworth low pass filter is an analog signal circuit, the problems of uniformity and balancing are more critical due to the sensitivity of analog signal circuit to variation in electrical parameters. Small variation within the components will affect the circuit performances.

The circuit is design and simulated using Silvaco GATEWAY while the layout for the filter is designed using Silvaco EXPERT tool.

II. EXPERIMENTAL

Figure 3 shows the process flow in designing the Butterworth Low Pass Filter. The process flow for the experiment is elaborated as follow.

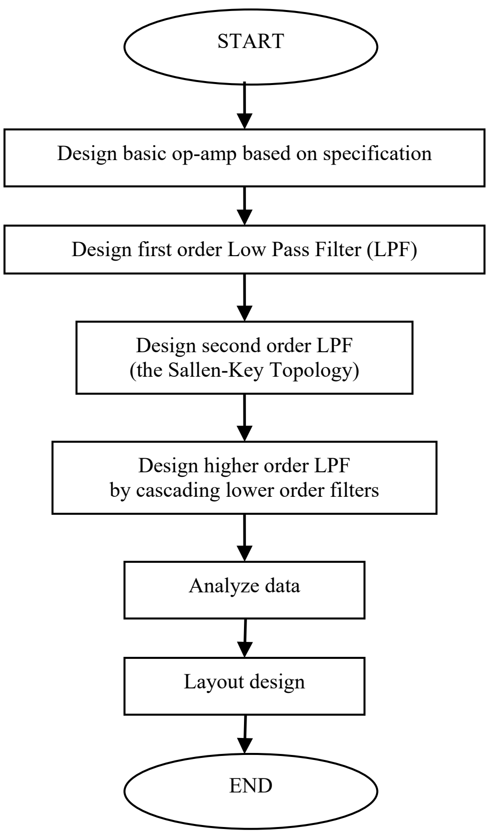

Figure 3. The process flow for the experiment.

A. *Design basic op-amp (two stages op amp)*

The op amp is design based on the specification. Table 1 shows the general specification for basic op amp.

TABLE 1. SPECIFICATIONS FOR BASIC OP-AMP

Specifications	**Design Requirement**
Phase Margin	> 60˚
Unity Gain Frequency	> 5MHz
DC Gain	>100 (40dB)
Voltage Swings	1.0V to 4.0 V
Slew Rate	> 5V/μs

Some equations are related to the specifications (Table 1). By implement both specifications parameters and equations, some important parameters can be derived.

$$GB = \frac{gm_2}{Cc} \quad (1) \qquad Cc \geq 0.22C_L \quad (2) \qquad SR = \frac{I_{D7}}{Cc} \quad (3)$$

$$gm_2 = \sqrt{2\beta_2 I_2} \quad (4) \qquad \beta_2 = k'n_2 \frac{W_2}{L_2} \quad (5)$$

For transistor sizing, Eq (4) and (5) will be used. The equations also are used to determine other transistor size (W/L). Simply set all transistor length, L=1µm for calculation wise.

B. *Design first-order LPF*

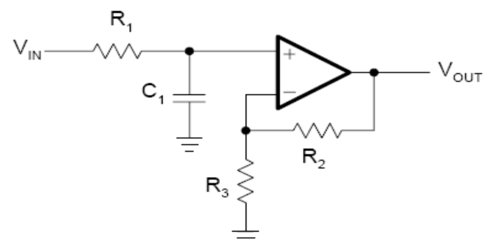

Figure 4. First-order Non-inverting LPF

The transfers function for the circuit in Figure 4:

$$A(s) = \frac{1 + \frac{R_2}{R_3}}{1 + \omega_c R_1 C_1 s} \quad (6)$$

Note that, to dimension the circuit, specify the corner frequency (fc), the dc gain (A_0) and capacitor C_1, and then solve for resistor R_1 and R_2. The coefficient a1 is taken from the Butterworth coefficient tables (Table 16-5: Butterworth Coefficients) [3].

$$A_0 = 1 + \frac{R_2}{R_3} \quad (7) \qquad a_1 = \omega_c R_1 C_1 \quad (8)$$

$$R_1 = \frac{a_1}{2\pi f_c C_1} \quad (9) \qquad R_2 = R_3(A_0 - 1) \quad (10)$$

C. *Design second-order LPF (Sallen-Key Topology)*

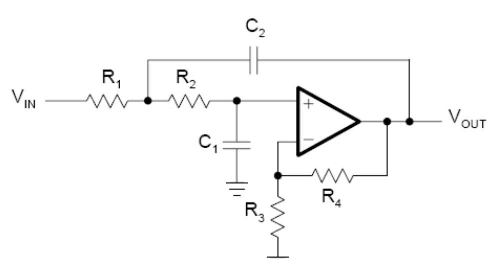

Figure 5. General Sallen-Key LPF

The transfers function for the circuit in Figure 5:

$$A(s) = \frac{A_0}{1 + \omega_c\left[C_1(R_1 + R_2) + (1 - A_0) R_1 C_2\right] s + \omega_c^2 R_1 R_2 C_1 C_2 s^2} \quad (11)$$

Since the Sallen-Key equal component is used, the transfer function of Figure 5 would be different from (11).

$$A(s) = \frac{A_0}{1 + \omega_c RC(3 - A_0)s + (\omega_c RC)^2 s^2} \quad (12)$$

with

$$A_0 = 1 + \frac{R_4}{R_3} \quad (13)$$

$$a_1 = \omega_c RC(3 - A_0) \quad (14) \qquad b_1 = (\omega_c RC)^2 \quad (15)$$

Set the value for C and solve for R and A_0

$$R = \frac{\sqrt{b_1}}{2\pi f_c C} \quad (16) \qquad A_0 = 3 - \frac{a_1}{\sqrt{b_1}} = 3 - \frac{1}{Q} \quad (17)$$

Thus, A_0 depends solely on the pole quality Q and vice versa; Q, and with it the filter type, is determined by the gain setting of A_0 [3]:

$$Q = \frac{1}{3 - A_0} \quad (18)$$

D. The Butterworth response is analyzed for various filter's order by applying the AC analysis.

E. The final step is design the layout for first order Butterworth Low Pass Filter.

There are some issues arises in analog signal design such as matching transistor, transistor scale sizing, number of contact required, components sizing, placing nmos and pmos, metal routing and component's body. Some techniques have been used in order to avoid such issues that affect the performance of the analog signal circuit.

III. RESULTS AND DISCUSSIONS

A. Op-amp design

The calculation is done based on the requirement stated in Table 1. Some of the parameter (such as width, length, load capacitor and etc.) was specified to fulfill the requirements. The AC and Transient analysis has been done to discover the required parameters. At this level, the value of width and length has been adjusted since it control the amount of current in a transistor, so that the op-amp meets the requirements.

In order to have a stable op-amp, the value for Cc must satisfy equation (1) for 60°ΦM. The value of total current I_{D7}, is determined using Eq (3) since the slew rate, SR is given. The transistor size (W/L) is determined by Eq.(4) and (5) once the value of gm_2 is found by using Eq (1).

Table 2 shows the simulation results for the op-amp. From Table 2, it is clearly shows that the op-amp has met the specifications.

TABLE 2. THE SPECIFICATION RESULTS FROM OP-AMP SIMULATION

Specifications	Results	Note
Phase Margin	> 60˚	Achieved
Unity Gain Frequency	6.5065MHz	Achieved
DC Gain	58.076dB	Achieved
Slew Rate	5.1442V/µs	Achieved

B. First-order LPF circuit

Based on the circuit in Figure 4, the value for capacitor is set to 100pF while the value for the resistor R_1 is determined using equation (9). Since first-order LPF did not have the quality factor Q, the values for R_2 and R_3 (refer to Figure 4) has been calculated using equation (7) by setting the gain A_0=2. Hence, the values for R_1 is 19kohm and for R_3=R_2 are 10kohm with the cutoff frequency (f_c) of 82 kHz.

C. Second-order LPF circuit

The second order circuit in Figure 5 is represented as Sallen-Key topology. Similar to analysis in section 3.2, the capacitor is set to 100pF. Since the circuit applied the Sallen-Key equal components method, the value for capacitors C_1= C_2=100pF and so for the resistors R_1= R_2 =19kohm. The value of R_3 remains 10kohm while R_4 has changed from 10kohm to 5.9kohm due to the value of gain A_0 given by the value of Q in Table 16-5: Butterworth Coefficients [3]. The value of R_4 must be different for every stage in every single order since the quality factors for every order are different.

D. Analysis of Ideal filter for Butterworth LPF approximation

Obviously, by increasing the filter's order, the filter characteristics will approximate the ideal filter. In order to have higher filter's order, the lower filter's order is cascaded (refer Figure 1). The AC analysis is applied for various orders of Butterworth LPF circuits to discover the filter approximation toward the increasing of filter's order. As for this analysis, the highest numbers of order would be 6 due to the complexity of the circuit.

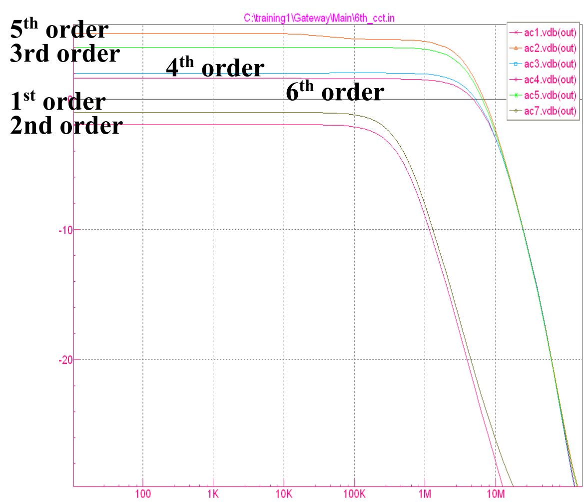

Figure 8. The Butterworth LPF response for different filter's order.

Figure 8 shows how the filter's order affects Butterworth filter approximation. By increasing the number of filter's order, the degree of response flatness increased and the transition band became narrow. This will result in Butterworth filter approximation. All response did not start at the same magnitude as the gains produced for every order are different from each other.

E. First- order Butterworth low pass filter layout.

As discussed before, some issues arises while design analog layout such as matching transistor, transistor sizing (large transistor), number of contact required, transistor body and etc.

MOSFETs with large channel width, W, usually employs multiple gate fingers. One reason is to obtain an overall shape that is easier to integrate into layout. Long skinny transistor are difficult to place and wire, while FETs that have shape closer to a square are much easier to deal with [8]. Figure 9 shows how large channel width, W has been integrate into square shape.

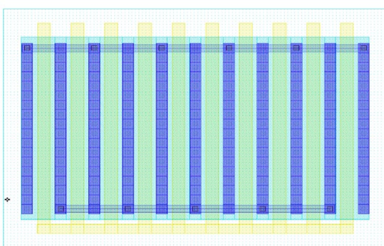

Figure 9. Large channel width of pmos with multiple gate fingers

Circuit such as differential amplifiers and current mirror are sensitive to differences [8]. In order to reduce the effect of variations, the common-centroid design is applied. Figure 10 shows how common-centroid design has been implemented for current mirror circuit.

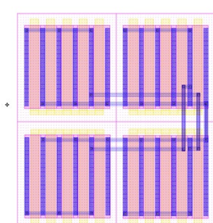

Figure 10. The common-centroid design for current mirror circuit.

Number of contact required for every transistor are unlimited since the more contact is placed; the routing process would be easy.

The transistor bodies are very important to reduce the variation effect. For transistor, the body will surround the transistor itself, but for some other components such as resistor will only used dummy elements for the same purpose.

Figure 11 shows the layout for op-amp. Every component in op-amp circuit has been surrounded by the body to avoid the effect of process variation.

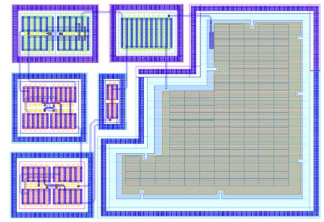

Figure 11. Op-amp layout

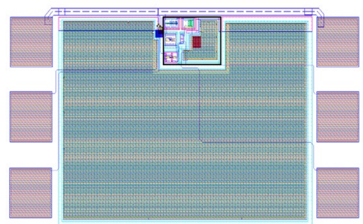

Figure 12. First-order Butterworth Low Pass Filter Layout

Figure 12 is the layout for first order Butterworth lowpass filer. The size of capacitor was not suitable for the circuit since it fill most of the chip area. Good assumptions are important at design stage since it will affect the layout design.

CONCLUSIONS

By completing this study, it can be concluded that by increasing the filter's order, the degree of passband flatness will increase and the filter will approximates the ideal filter characterization. Even though the circuit became more complicated due to the increases of the order, the Sallen-Key topology is a good choice in reducing the circuit complexity. It is important to choose the suitable sizing for every component while doing the schematic design for layout purposes.

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