Investigation of electrical characteristics of partially depleted silicon on insulator device

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Abstract **- Well constructed models for n-type n-MOSFET using bulk technology and partially depleted (PD) silicon on insulator (SOI) technology had been developed. The models were simulated using Silvaco-Athena software to find electrical properties such as threshold voltage, sub-threshold and leakage current. Comparison of electrical properties for both technology and channel length were done accordingly from each result. This paper was focus on investigation of the electrical characteristics of the devices at 0.5 micron and 0.35 micron channel length. Silvaco Athena structure and simulation results using Atlas were presented, that shows PD SOI technology is better than Bulk technology in the small scaling of channel length.**

Index term**- n-MOSFET, SILVACO-ATHENA, ATLAS, PD SOI.**

I. INTRODUCTION

Over the past decade, the MOSFET has continually been scaled down in size such as the typical channel length was once several micrometres [1]. Nowadays, the modern integrated circuits are research on incorporating MOSFET with channel lengths of ten nanometres [2]. Producing MOSFET with channel length much smaller than a micrometer is a challenge and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. The small size has created electrical operational problem in the MOSFET such as threshold voltage, sub threshold voltage and leakage current.

SOI n-MOSFET technology has become another advanced technology for very large scale integrated (VLSI). The advantage of SOI is the capability to provide deep submicron VLSI device for generating high speed, low power and low voltage supply. SOI technology also preferred for its advantages such as full dielectric isolation and reduction of junction capacitance and kink effect.

There are two types of SOI available in the market, which are fully depleted (FD) and partially depleted (PD) depending on the extent of the silicon thickness on the insulator. [3]. usually, the thickness of silicon for PD SOI device is in range between 100nm to 500nm [4].

The cross section of partially depleted SOI compared to bulk is shown in Fig.1. The major difference between them is the insertion of an insulation layer beneath the device.

In this paper, three electrical characteristics are simulated which are threshold voltage, sub threshold voltage and leakage current for two scales of channel length, 0.35um and 0.50um.

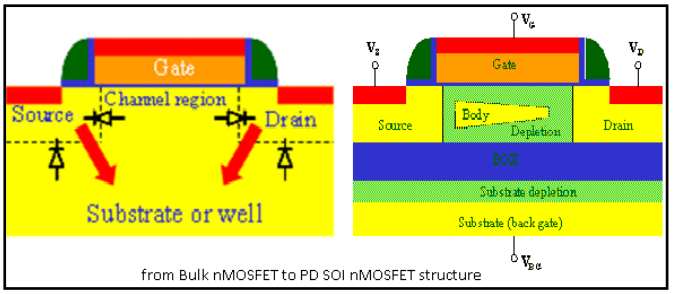

Fig 1: Migration from bulk to PD SOI structure

II. METHODOLOGY

The statistical analysis was employed in order to create bulk n-MOSFET and PD SOI n-MOSFET structures. This preliminary study was done in order to be able to compare the result between bulk and SOI .The electrical engineering software like TCAD SILVACO ATHENA tool was used to run the process simulation of n-MOSFET model structures and SILVACO ATLAS tool was used to plot the graph and extract its electrical parameters.

Once the pre study completed, the device structure was formed. The bulk n-MOSFET device structure formed by plotting the structure out file Athena mode while the PD SOI device structure was created by using the Silvaco Atlas syntax mode directly.

Bulk and PD SOI n-MOSFET device structures with both channel lengths were simulated using Silvaco Atlas device simulator. It was observed that the value of threshold voltage, sub threshold and leakage current changed according to the behaviours that were applied on each device.

The graph of electrical properties was plotted by atlas tool log and solution files. The values of the parameter such as threshold voltage, sub threshold and leakage current were extracted using atlas according to the Tonyplot appeared. The variable such as temperature, impurities dose and doping concentration are varied in order to get acceptable value of electrical parameters

The values of threshold voltage and sub threshold were extracted from the Id-Vg curve while the values for leakage current from the Id-Vd curve. The graphs and the values obtained were compared between bulk n-MOSFET and PD SOI n-MOSFET device.

The flows of all the processes were summarized as shown in Fig.2 flowchart.

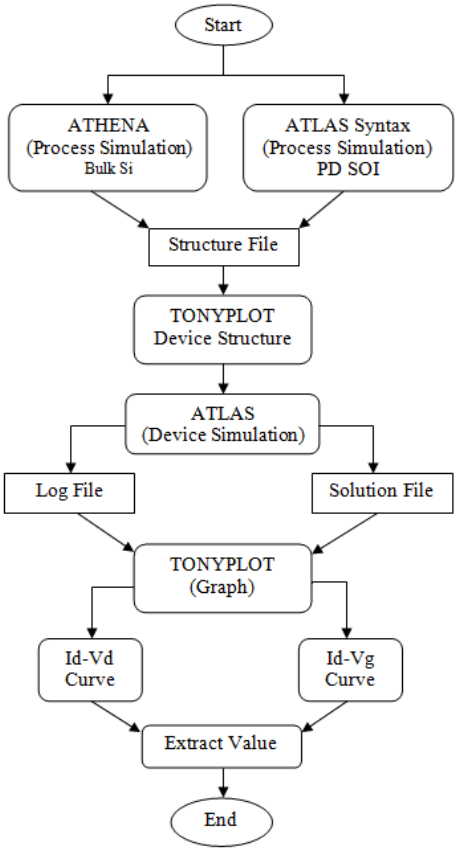

Fig.2. The research methodology.

III. RESULT AND DISCUSSION

There are three parts of comparison in this reserch. Firstly comparison between 0.35um and 0.5um bulk n-MOSFET technology. Secondly comparison between 0.35um and 0.5um PD SOI n-MOSFET. Thirdly comparison between both technologies at the same channel length.

A. Electrical Properties at 0.35um and 0.5um bulk n-MOSFET

The bulk n-MOSFET was constructed using Silvaco Athena at 0.35um and 0.5um. The device structure for both channel lengths of bulk n-MOSFET are shown in Fig.3 and Fig.4. The channel length can be differentiate by looking the length of gate. The channel region of 0.35um structure was doped with concentration of boron 7.8E12cm^{-3} while for drain and source region was doped with concentration of arsenic 3E13cm^{-3}. For the 0.5um structure, the channel region was doped with 2.6E12cm^{-3} boron while for drain and source region was doped with concentration of arsenic 2.8E13cm^{-3}.

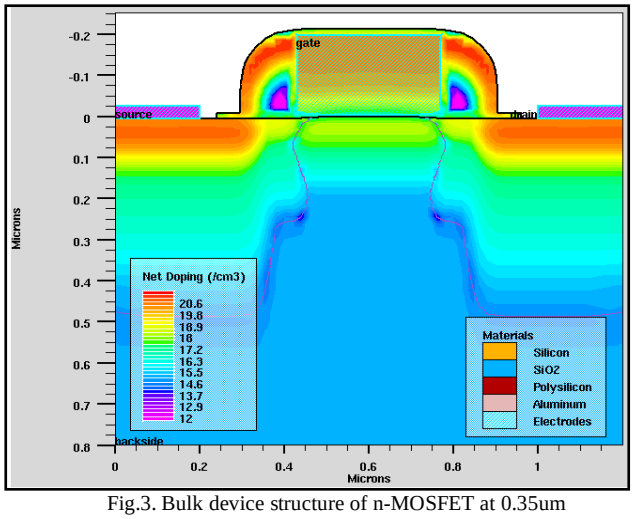

Fig.3. Bulk device structure of n-MOSFET at 0.35um

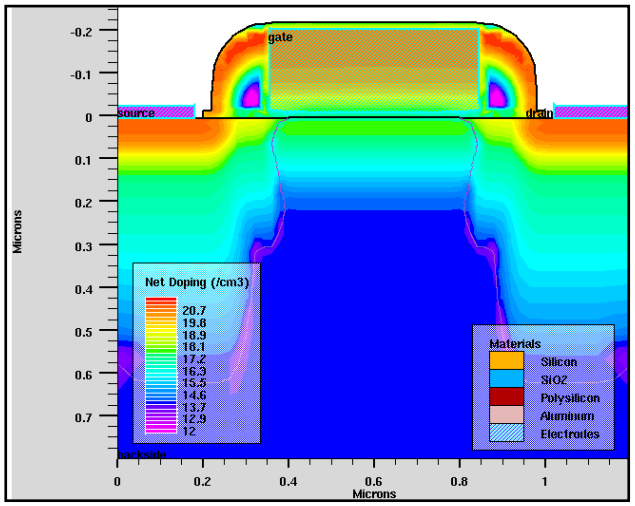

Fig.4. Bulk device structure of n-MOSFET at 0.5um

In extracting result, the tonyplot was considered. The tonyplot for the threshold voltage of bulk n-MOSFET at 0.35um and 0.5um is shown in Fig.5 and Fig.6 respectively. The plots of Id versus Vgs was applied with dc bias of Vds=0.1 V and ramp the gate voltage from 0 V to 3 V with a bias step size of 0.1 V. The threshold voltage for 0.5um is 0.741768 V higher than 0.35um channel length which is 0.626317 V. There are because the channel doping for 0.35um has been doped with concentrantion 7.8E12cm^{-3} greater than channel doping for 0.5um which is 2.6E12cm^{-3}. When the channel doping concentration increase, the depletion charge in the channel also increase, which causing the threshold voltage decrease [6][7].

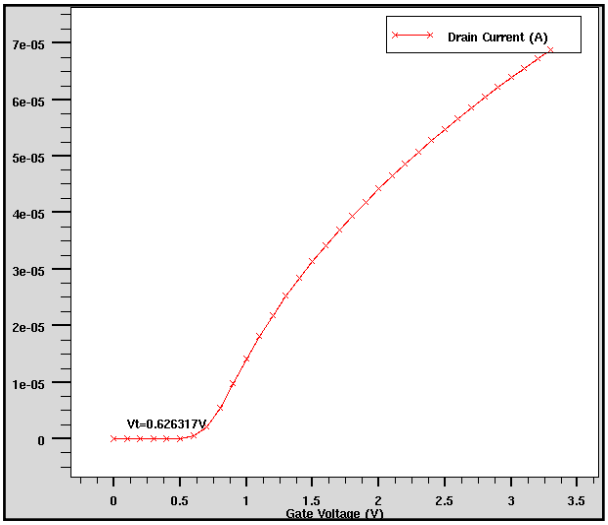

Fig.5.Threshold voltage of bulk n-MOSFET at 0.35um

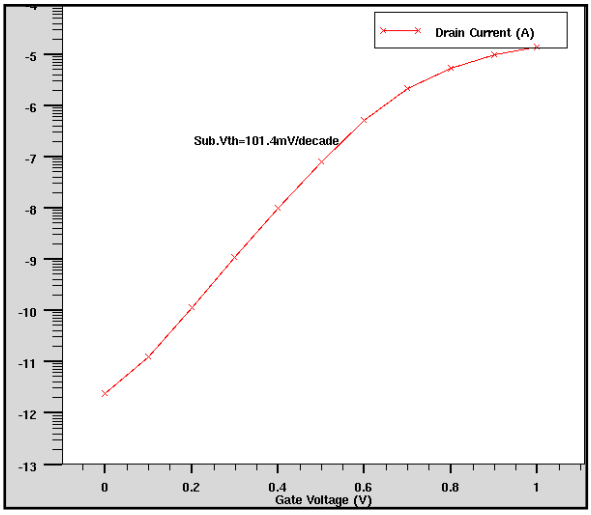

Fig.7.Subthreshold of bulk n-MOSFET at 0.35um

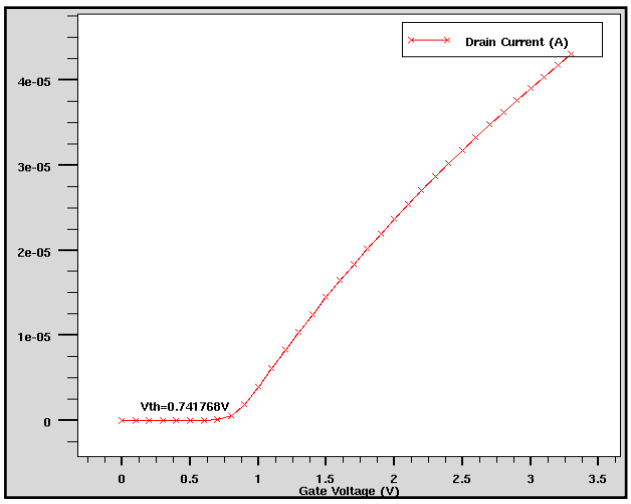

Fig.6.Threshold voltage of bulk n-MOSFET at 0.5um

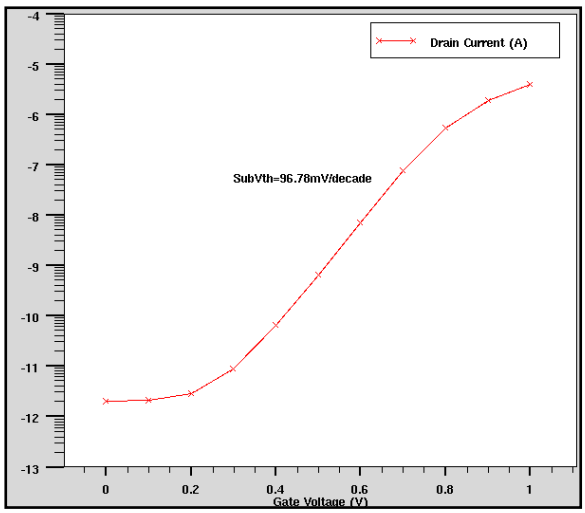

Fig.8.Subthreshold of bulk n-MOSFET at 0.5um

The tonyplot for the Subthreshold voltage of bulk n-MOSFET at 0.35um and 0.5um is shown in Fig.7 and Fig.8 respectively. The plots of log Id versus Vgs with fixed Vds was applied with bias the drain from 0.025 V to 0.1 V with a bias step size of 0.025 V and ramp the gate voltage from 0 V to 0.1 V with a bias step size of 0.1 V. The subthreshold slope for 0.35um and 0.5um bulk n-MOSFET device is 101.42mV/decade and 96.77mV/decade respectively. The subthreshold for 0.35um is higher than 0.5um. As the gate length decreased, the short channel effect became serious because the roll off of threshold voltage so the subthreshold increased [8].

The tonyplot for the leakage current of bulk n-MOSFET at 0.35um and 0.5um is shown in Fig.9 and Fig.10. The plots of Id versus Vds was applied with dc bias of Vds = 0.1 V and ramp the drain voltage from 0 V to 3.3 V with a bias step size of 0.1 V. The leakage current for 0.35um and 0.5um bulk n-MOSFET device is 8.797E-7A and 1.739E-7A respectively. Shorter channel length will give the effect on the ionization and conducting the excitation of the electron [7]. So it is reasonable that the leakage current for 0.35um is higher than 0.5um channel length.

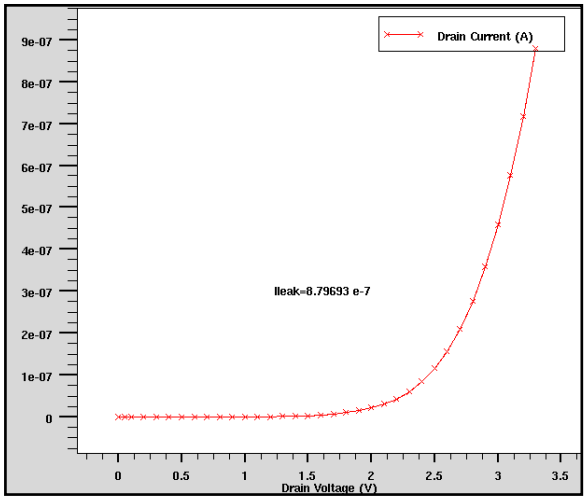

Fig.9.leakage current of bulk n-MOSFET at 0.35um

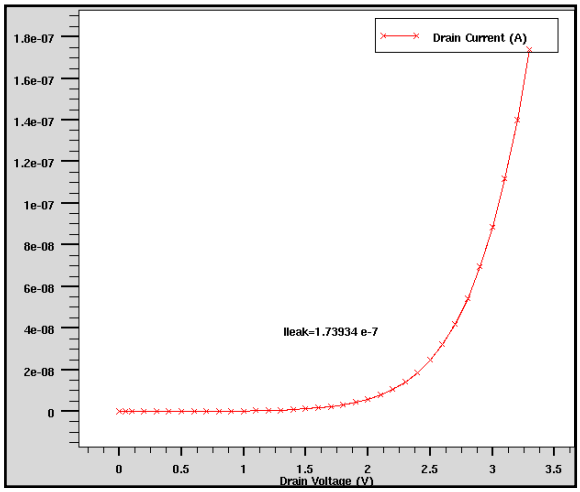

Fig.10.Leakage current of bulk n-MOSFET at 0.5um

TABLE.1 shows the comparison of the electrical properties of bulk n-MOSFET at different channel length. The threshold voltage is decrease while subthreshold and leakage current are increase as the channel length reduced.

TABLE.1
THE EXTRACTED VALUES OF THE ELECTRICAL CHARACTERISTICS OF BULK n-MOSFET AT DIFFERENT CHANNEL LENGTH

Electrical characteristics	0.35 um	0.5 um
Vth (V)	0.6263	0.7418
SubVth (mV/decade)	101.42	96.77
Ids leakage (A/um)	87.97	17.39

B. Electrical Properties at 0.35um and 0.5um PD SOI n-MOSFET.

The PD SOI n-MOSFET is constructed using Silvaco Atlas syntax at 0.35um and 0.5um technology. The device structure of PD SOI n-MOSFET for both channel length is shown in Fig.11 and Fig.12. The p-type material channel doping concentration of 0.35um structure is 1.2E17cm^{-3} while for n-type drain and source doping concentration is 6.4E18cm^{-3}. For the 0.5um structure, the channel doping concentration is 9.8E16cm^{-3} while for drain and source doping concentration is 1E17cm^{-3}. Besides that, the silicon thickness on insulator which is 0.2um reasonable as partially depleted region device. The silicon thin film thickness (Tsi) for PD SOI is in range of 0.1um till 0.5um.

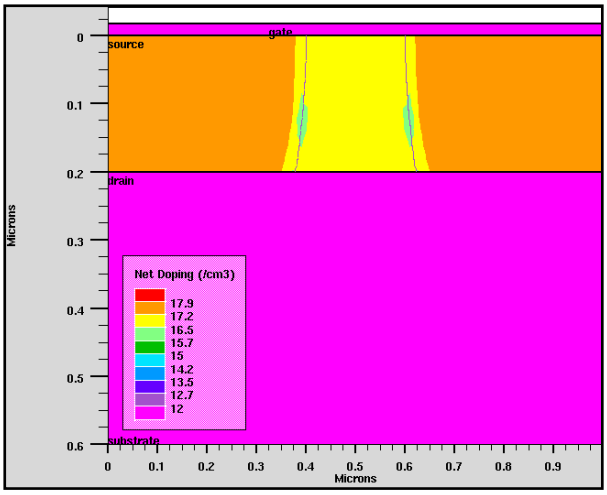

Fig.11. PD SOI device structure of n-MOSFET at 0.35um

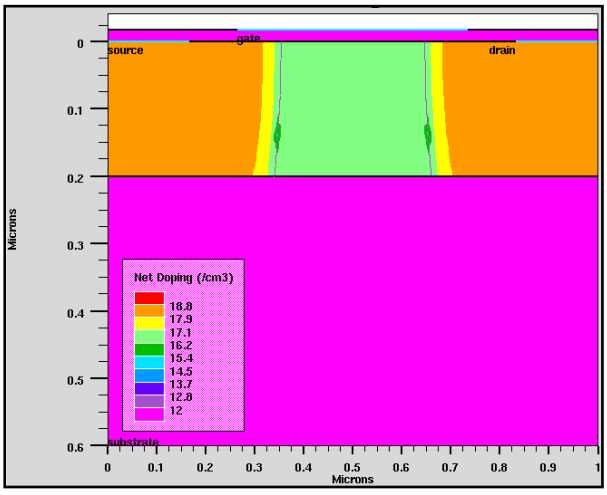

Fig.12. PD SOI device structure of n-MOSFET at 0.5um

In extracting result, the tonyplot was considered.The plots for the threshold voltage of PD SOI n-MOSFET at 0.35um and 0.5um is shown in Fig.13 and Fig.14 respectively. The plots of Id versus Vgs was applied with dc bias of Vds= 0.1 V and ramp the gate voltage from 0.10 V to 1.5 V with a bias step size of 0.1 V. The threshold voltage PD SOI for 0.35um is 0.50208V while for 0.5um is 0.52017V. There are because the channel doping for 0.35um has been doped with concentrantion 1.2E17cm^{-3} greater than channel doping for 0.5um which is 9.8E16cm^{-3}. When the channel doping concentration increase, the depletion charge in the channel

also increase, which causing the threshold voltage decrease. When PD SOI models are compared for different device sizes then threshold voltage is decrease as the channel length reduced [6][7].

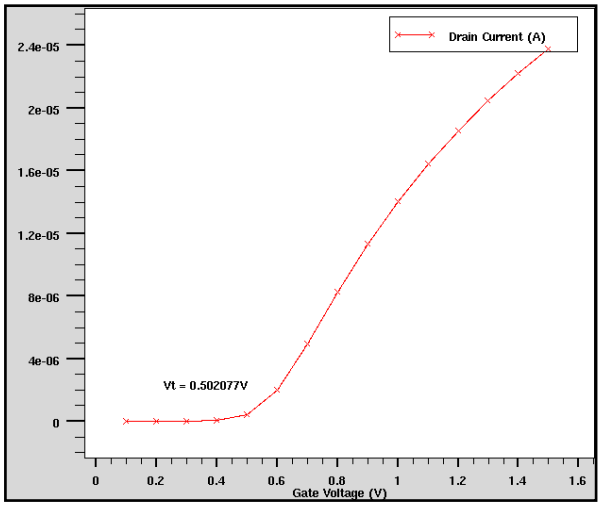

Fig.13.Threshold voltage of PD SOI n-MOSFET at 0.35um

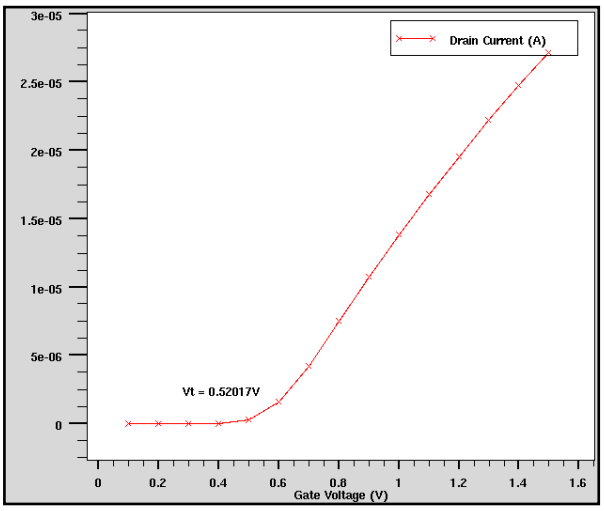

Fig.14.Threshold voltageof PD SOI n-MOSFET at 0.5um

The plots for the subthreshold voltage of PD SOI n-MOSFET at 0.35um and 0.5um is shown in Fig.15 and Fig.16 respectively. The plots of log Id versus Vgs was applied with fixed Vds at 0.05 V and 0.1 V and ramp the gate voltage from 0.1 V to 1.5 V with a bias step size of 0.1 V. The subthreshold slope of the 0.35um and 0.5um PD SOI device is 98.24mV/decade and 94.36mV/decade. When PD SOI models are compared for different device sizes then subthreshold voltage is increase as the channel length reduced. The subthreshold behaviour of an SOI n-MOSFET device depend on the thickness of the silicon thin-film, the doping density of the silicon thin-film and the channel length [10].

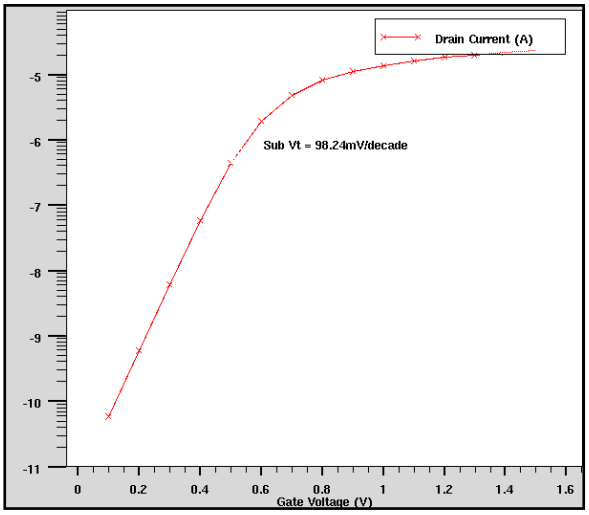

Fig.15.Subthreshold of PD SOI n-MOSFET at 0.35um

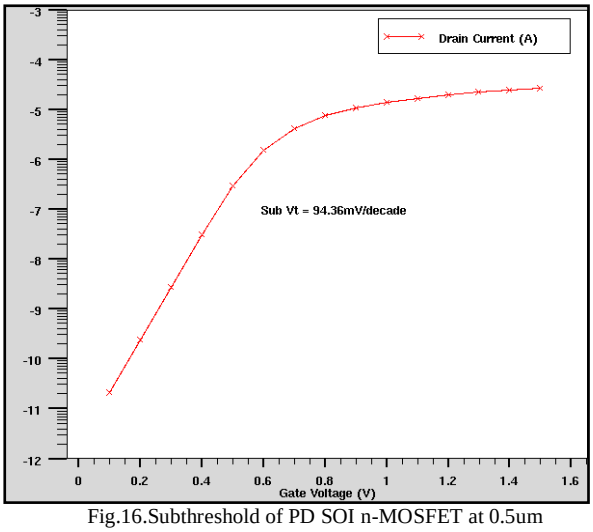

Fig.16.Subthreshold of PD SOI n-MOSFET at 0.5um

The plots for the leakage current of PD SOI n-MOSFET at 0.35um and 0.5um is shown in Fig.17 and Fig.18. The plots of Id versus Vds was applied with dc bias of Vds= 0.10 V and ramp the drain voltage from 0 V to 3.3 V with a bias step size of 0.1 V. The leakage current of the 0.35um and 0.5um PD SOI device is 1.965E-7A and 8.407E-10A. When PD SOI models are compared for different device sizes then leakage current is increase as the channel length reduced. That is reasonable where shorter channel length will give the effect on the ionization and conducting the excitation of the electron [9][10]. So that, the leakage current increase as the channel length decrease.

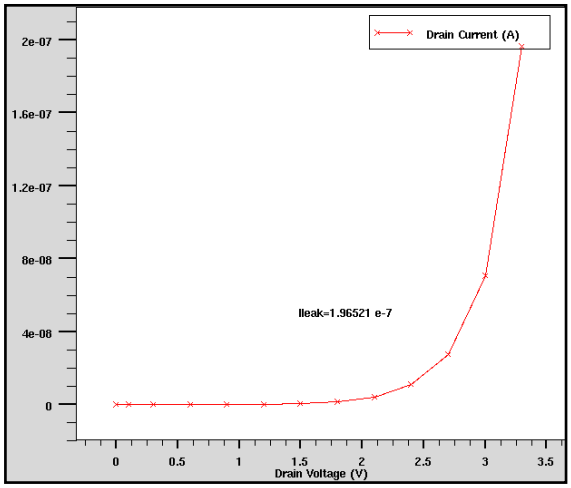

Fig.17.Leakage current of PD SOI n-MOSFET at 0.35um

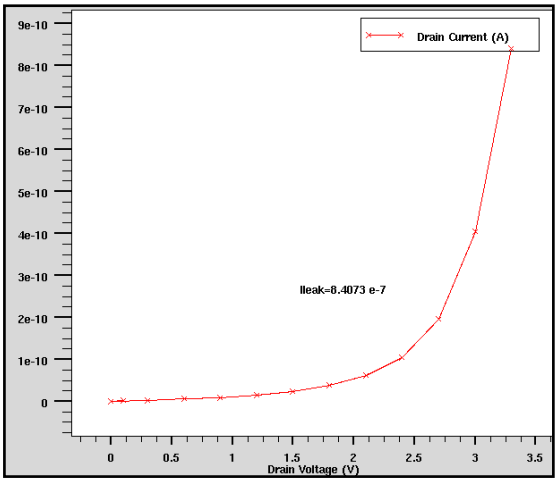

Fig.18.Leakage current of PD SOI n-MOSFET at 0.5um

TABLE.2 shows the comparison of the electrical properties of PD SOI n-MOSFET at different channel length. The threshold voltage is decrease while subthreshold and leakage current are increase as the channel length reduced.

TABLE.2
THE EXTRACTED VALUES OF THE ELECTRICAL CHARACTERISTICS OF PD SOI n-MOSFET AT DIFFERENT CHANNEL LENGTH

Electrical characteristics	0.35 um	0.5 um
Vth (V)	0.5021	0.5202
SubVth (mV/decade)	98.24	94.36
Ids_leakage (A/um)	19.65	84.07n

C. The comparison of electrical properties between bulk n-MOSFET and PD SOI n-MOSFET at 0.35um and 0.5um.

TABLE.3.
THE VALUE OF THRESHOLD VOLTAGE, SUBTHRESHOLD AND LEAKAGE CURRENT AT 0.35um FOR BULK AND PD SOI TECHNOLOGY.

Electrical Characteristics	0.35um Bulk n-MOSFET	0.35um PD SOI n-MOSFET
Threshold voltage (V)	0.62632	0.50208
Sub-threshold voltage (mV/dec)	101.42	98.24
Leakage current (A)	$8.797e^{-7}$	$1.965e^{-7}$

TABLE.4.
THE VALUE OF THRESHOLD VOLTAGE, SUBTHRESHOLD AND LEAKAGE CURRENT AT 0.5um FOR BULK AND PD SOI TECHNOLOGY.

Electrical Characteristics	0.5um Bulk n-MOSFET	0.5um PD SOI n-MOSFET
Threshold voltage (V)	0.74177	0.52017
Sub-threshold voltage (mV/dec)	96.77	94.36
Leakage current (A)	$1.739e^{-7}$	$8.407e^{-10}$

TABLE.3 and TABLE.4 shown that the threshold voltage of bulk n-MOSFET found to be bigger than PD SOI model and then threshold voltage decrease as the channel length decrease. The subthreshold of bulk n-MOSFET is found to be more than PD SOI n-MOSFET model but there are quite similar to each other. The subthreshold increase as the channel length decrease. The leakage current of bulk n-MOSFET model is found to be more than PD SOI n-MOSFET model and then the leakage current is increase as the channel length decrease.

The PD SOI device is largely identical to the bulk device, except for the addition of buried oxide (BOX) or Silicon Oxide (insulator) layer. Since the source and the drain region extended into the BOX, the junction surface is minimized which reduced the junction capacitance and the leakage current. The charge sharing between the gate and junction is reduced because of the limited extension of the source and drain regions [11]. So, the SOI devices are less affected by short channel length.

The subthreshold behaviour of an SOI nMOSFET device depend on the thickness of the silicon thin-film, the doping density of the silicon thin film and the channel length. When the silicon thin film is thick (partially depleted), the subthreshold slope of the PD SOI n-MOSFET device is similar to that of the bulk n-MOSFET device. When the silicon thin film is thin (fully depleted), its subthreshold much better with its value close to the ideal case due to the BOX

isolation between the channel and the ground substrate[11][12]

IV. CONCLUSION

The investigation on the PD SOI n-MOSFET structure using process simulator Silvaco Athena at 0.35um and 0.5um is compared with the bulk n-MOSFET at the same technology nodes for the various electrical properties. The investigation on the both technology shows the improvement of electrical characteristics of SOI as compared to the bulk device n-MOSFET structure. Even thought SOI give a positive result, the parasitic effect will also appear increasing of sub-threshold and leakage current when the scale was reduced in SOI continuously.

V. ACKNOWLEDGEMENT

The author gratefully acknowledges the facilities provided in Laboratory of Electrical Engineering, Universiti Teknologi MARA, Shah Alam, Malaysia.

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