STUDY ON THE EFFECT OF THE POLYSILICON DOPING ON THE JUNCTION DEPTH IN THE 65 NM STRUCTURE

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ABSTRACT

An analysis on the effect of the polysilicon doping on the junction depth in the 65 nm structure was conducted in this paper. Several parameters presented in the polysilicon doping process were investigated and the TONY PLOT profile for the junction depth was developed to help understanding the polysilicon doping effect which is crucial to produce stable threshold voltage and also how some of these parameters have effect on the n^{++} sheet resistance. For this doping process, it was conducted using ion implantation technique with two type of impurities; phosphorus and arsenic on crystalline material. The cutline to extracting the junction depth at gate and source/drain in TONY PLOT was done for investigation in dependence of the polysilicon doping profile. All simulations were done by using SILVACO.

Keyword:
Polysilicon doping, junction depth, ion implantation, phosphorus, arsenic.

1.0 INTRODUCTION

It is generally recognized that miniaturization is the key to improve performance and functionality of an integrated circuit technology. As CMOS devices are scaled down to nanometer and below, with the increased doping levels and reduction of channel length and gate oxide thickness, junction depth profile is becoming a significant contributor to stability of threshold voltage in CMOS circuits[1].

Different methods of doping procedure has been introduced to improve the thermal diffusion process in order to find the better way in producing the precise distribution of impurities in which a better electrical characteristics of polysilicon films successfully tailored into specific application[2] since for the modern device, the thermal processing must be minimized for suppressing dopant diffusion[3]. Ion implantation is another alternative technique of introducing such impurities into polysilicon with a more precise manner and mostly employed to forming shallow junctions. The dopant atom is fired into the polysilicon surface through accelerated ions with specified energies. The latter provides a better lateral registration of doped regions and superior control of dopant concentration, depth and uniformity. Besides, ion implantation also offers better control of the doping process, resulting in higher reproducibility of electrical parameters and also improved yield[4].

The development of polysilicon technology was driven by the use of polysilicon as a gate electrode or as an intermediate conductor in two-level structures for integrated circuits. In CMOS processes particularly, one of the main reasons for using the polysillicon is due to the fact that polysilicon allows the integration of "dual-flavoured" gates: p- and n-type polysilicon for PMOS and NMOS, respectively. Grain sizes and the surface texture of these films are functions of the polysilicon deposition and doping conditions as well as subsequent oxidation and thermal cycle[5]. In CMOS devices, the polysilicon gate must be doped to render it conductive and this is done with either diffusion or ion implantation. For ease of fabrication, the deposited polysilicon film has traditionally been doped with an n^{+} dopant for both n-channel and p-channel devices prior to the gate patterning process.

For source and drain junction depths greater than the CMOS's gate depletion-layer width, negligible benefit is obtained from scaling the junction depth. However, for source and drain junction depths less than the CMOS's gate depletion-layer width, a decrease in short-channel effect (SCE) can be obtained through scaling these junction depths[6].

The main objective of this paper is to study the effect of polysilicon doping profile on junction depth. Junction depths are extracted after polysilicon doping and annealing process.

2.0 METHODOLOGY

The main objective was to study the effect during the process of polysilicon doping on the junction depth in NMOS using 65 nm technologies but the additional information about the n^{++} sheet resistance and threshold voltage are also included. Firstly, the NMOS structure was fabricated using 65 nm technologies. The fabrication process starts with well (initial substrate), and for the NMOS, the well that fabricated uses P-type impurity of Boron with <100> orientation. Process continued by forming polysilicon gate and gate optimization purposely to have better gate oxide thickness. After deposited the polysilicon, the polysilicon then was defined with the desired length in geometrical etches process before it was covered up by oxidation process. Process of polysilicon doping took part, which two N-type impurities were observed; Phosphorus and Arsenic. The parameters involved in this process are varied including concentration dosage and energy used. The concentration used range from 1e13 ions/cm^2 up to 5e13 ions/cm^2 while for energy used range from 20 KeV to 24 KeV. This range was chosen since it gave reliable value for threshold voltage. The default value for tilt and rotation used were 7^0 and 30^0 respectively since these were the value commonly used in industry.

For each of the impurities observed during the polysilicon doping process, it were observed in two models which was Dual-Pearson and Gauss model to determine junction depth majorly while sheet resistance and threshold voltage value as additionally. The defects presented in the polysilicon doping process were observed and to determine either there were any significant changes due to the defect of Point Defect, Cluster Defect and Dislocation Defect, which every defect have their own parameters to be studied. For these defect, it were observed by using the impurity of Phosphorus and Arsenic with the value that gave reliable threshold voltage in Dual-Pearson model. For all the observation in the polysilicon doping process, it was done with crystalline material type.

The NMOS fabrication process continued with spacer oxidation and formation and formation of source/ drain before the annealing process. The junction depth graph was obtained after the annealing process in order to observe of the effect during the process of polysilicon doping on the junction depth of the source/ drain. The process continued with the inserting the open contacts windows and the additional info for sheet resistance was extracted. The process fabricating the NMOS structure was completed with the structure being mirrored to the right. This process gave the full structure of NMOS.

To obtain the additional value of the threshold voltage, the simulation was run in Atlas mode since it needs to log the graph for threshold voltage.

The flow chart below summarize the processes involve in fabricating the NMOS structure.

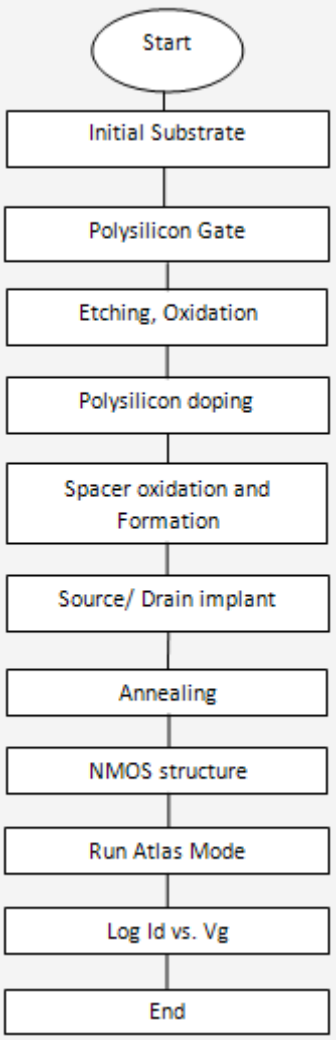

Figure 1: Flowchart of summarized NMOS fabrication

3.0 RESULT AND DISCUSSION

3.1 Energy

3.1.1 Dual-Pearson Model

Table 1 and table 2 show the result for junction depth, sheet resistance and threshold voltage by using the Dual-Pearson model when different values of energies were applied with impurity of:

a) **Phosphorus**

Table 1: Result by using impurity Phosphorus

Dos (ion/ cm^2)	Energy (KeV)	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
4e13	20	0.0438377	3937.98	0.435682
4e13	21	0.0456977	4018.32	0.431596
4e13	22	0.0477468	4002.14	0.431427
4e13	23	0.0505853	3983.98	0.419283
4e13	24	0.0540408	4019.56	0.402368

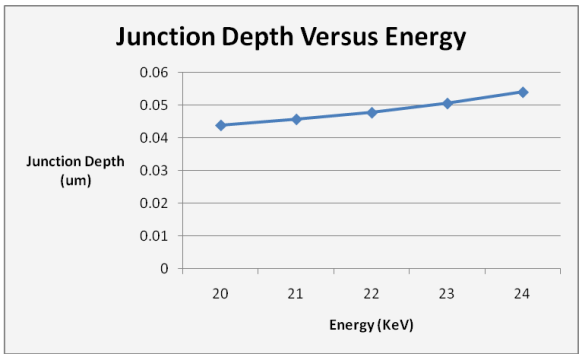

Figure 2: Graph junction depth versus energy

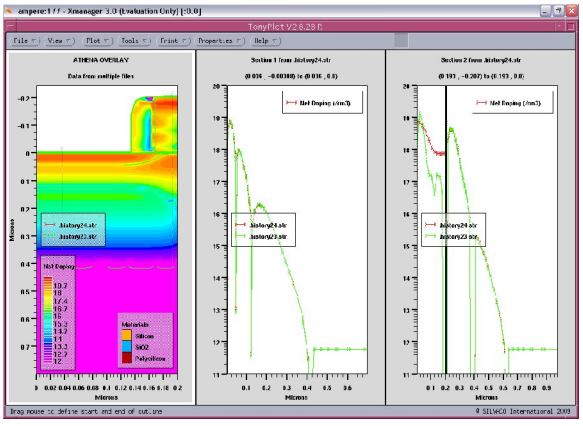

Figure 3: TONYPLOT cutline extracted at gate and source/ drain for energy of 20 KeV using Phosphorus for Dual-Pearson model.

b) **Arsenic**

Table 2: Result by using impurity Arsenic

Dos (ion/ cm^2)	Energy (KeV)	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
4e13	20	0.0339045	3261.27	0.315965
4e13	21	0.0346387	3304.82	0.320409
4e13	22	0.0353847	3349.48	0.316016
4e13	23	0.0361463	3412.93	0.30999
4e13	24	0.0369279	3474.38	0.307191

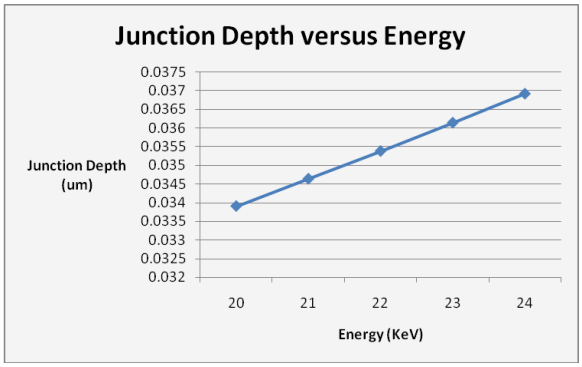

Figure 4: Graph junction depth versus energy

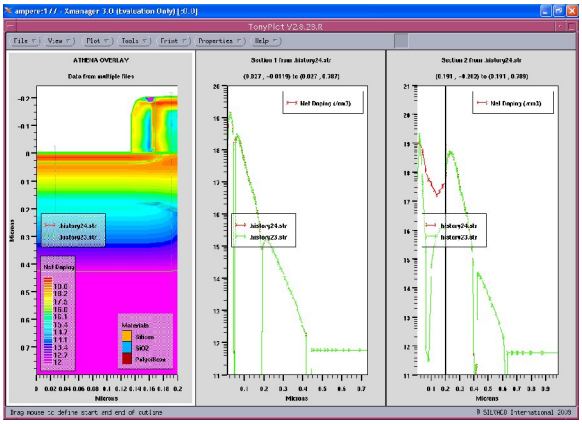

Figure 5: TONYPLOT cutline extracted at gate and source/ drain for energy of 20 KeV using Arsenic for Dual-Pearson model.

3.1.2 Gauss Model

Instead of Dual-Pearson model, the process continued by using the Gauss model and table 3 and 4 show the result for junction depth, sheet resistance and threshold voltage for each of the energies applied with impurity of:

a) **Phosphorus**

Table 3: Result by using impurity Phosphorus

Dos (ion/ cm^2)	Energy (KeV)	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
4e13	20	0.0516082	3753.62	0.41262
4e13	21	0.0547104	3821.51	0.40832
4e13	22	0.0582012	3872.55	0.39597
4e13	23	0.0622957	3901.07	0.38363
4e13	24	0.0671941	3910.23	0.37271

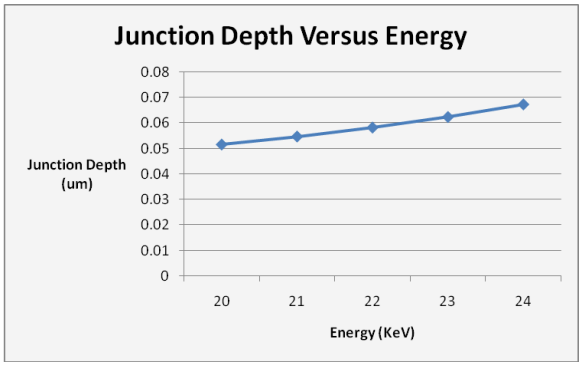

Figure 6: Graph junction depth versus energy

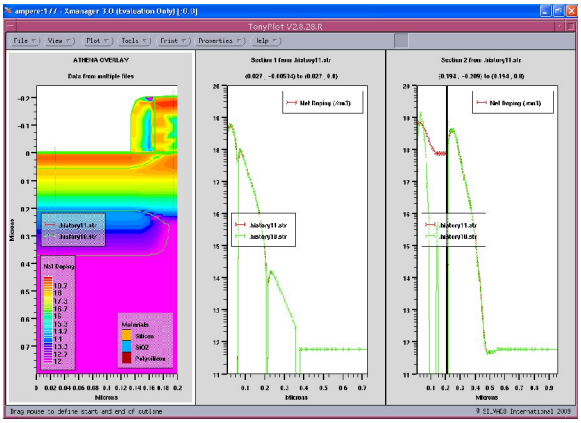

Figure 7: TONYPLOT cutline extracted at gate and source/ drain for energy of 20 KeV using Phosphorus for Gauss model.

b) **Arsenic**

Table 4: Result by using impurity Phosphorus

Dos (ion/ cm^2)	Energy (KeV))	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
4e13	20	0.0353486	3075.22	0.325686
4e13	21	0.0362113	3114.31	0.331359
4e13	22	0.0371272	3160.33	0.328982
4e13	23	0.0381019	3203.8	0.324991
4e13	24	0.0391401	3245.97	0.322599

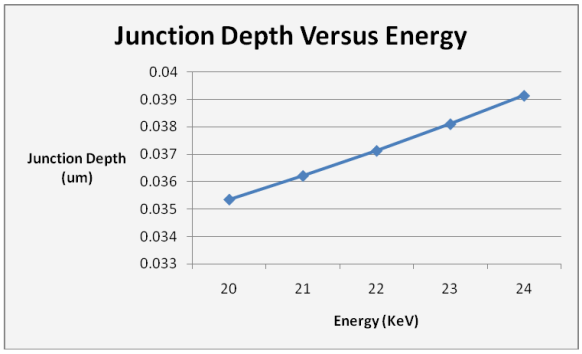

Figure 8: Graph junction depth versus energy

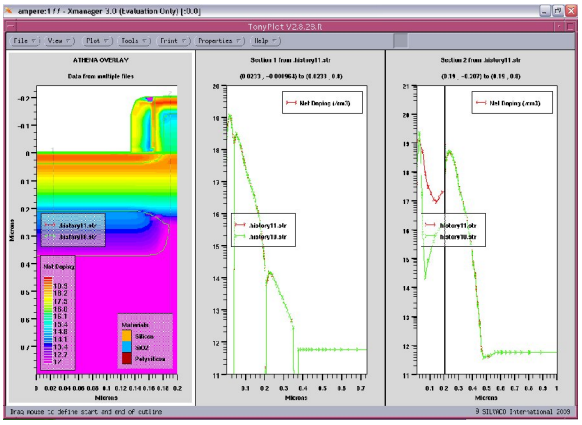

Figure 9: TONYPLOT cutline extracted at gate and source/ drain for energy of 20 KeV using Arsenic for Gauss model.

From the results tabulated in the Table 1 and Table 3 for the impurity of Phosphorus and Table 2 and Table 4 for the impurity of Arsenic, the junction depth value for impurity of Phosphorus is deeper than shown by Arsenic impurity with the same amount of concentration and energy applied as pictured in TONYPLOT in Figure 3 for Phosphorus and Figure 5 for Arsenic in Dual Pearson model while for Gauss model, Figure 7 for Phosphorus and Figure 9 for Arsenic.

For the doping process, ions of the desired element were produced, and an accelerator, where the ions were electrostatically accelerated to a high energy and the ions impinged on a target, which was the

material to be implanted. From the graph of Figure 2, 4, 6 and Figure 8, it shows that for both models; Dual-Pearson and Gauss, the implantation process at high energy can increase the junction depth since the characteristic for junction depth is proportional with the energy applied during the polysilicon doping process. This is because when the energy was applied to 'attack' the sample, it caused the impurity ions have more energy and will increase the diffusion speed thus the impurity ions will diffuse deeper into substrate[7]. The energy should not too high since it will cause the junction depth to go deeper into the substrate since junction depth must not exceed the polysilicon gate depletion layer in order to avoid degrading current drivability[8]

3.2 Concentration

3.2.1 Dual-Pearson Model

Table 5 and 6 show the result for junction depth, sheet resistance and threshold voltage by using the Dual-Pearson model when different values of concentrations were applied with impurity of:

a) **Phosphorus**

Table 5: Result by using impurity Phosphorus

Dos (ion/ cm^2)	Energy (KeV))	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
1e13	20	0.0139266	1.26879e9	1.74239
2e13	20	0.0272247	29404.2	0.489657
3e13	20	0.0362457	7401.24	0.46497
4e13	20	0.0438377	3937.98	0.435682
5e13	20	0.0508434	2548.28	0.346627

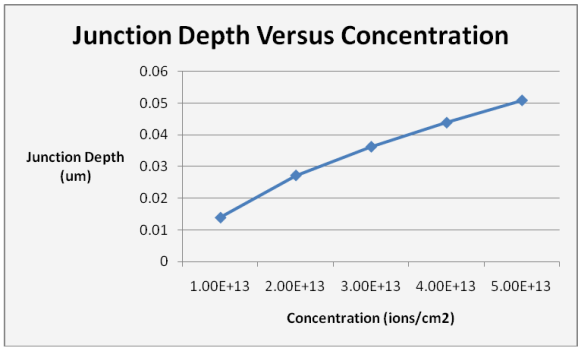

Figure 10: Graph junction depth versus concentration

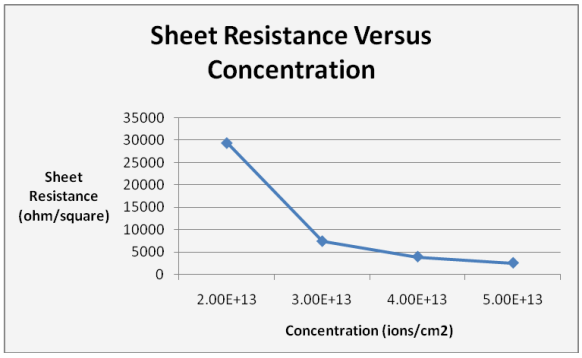

Figure 11: Graph sheet resistance versus concentration

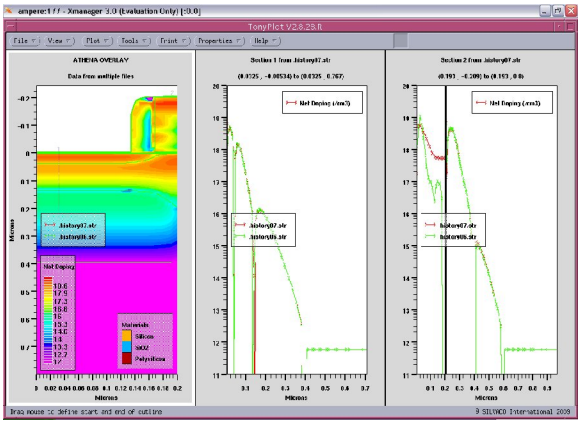

Figure 12: TONYPLOT cutline extracted at gate and source/ drain for concentration of 3e13 ions/cm^2 using Phosphorus for Dual-Pearson model.

b) **Arsenic**

Table 6: Result by using impurity Arsenic

Dos (ion/ cm^2)	Energy (KeV))	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
1e13	20	0.0198612	1.84666e6	1.76025
2e13	20	0.0271765	12922	0.339921
3e13	20	0.0312508	5258	0.332851
4e13	20	0.0339045	3261.27	0.315965
5e13	20	0.0357456	2338.05	0.278027

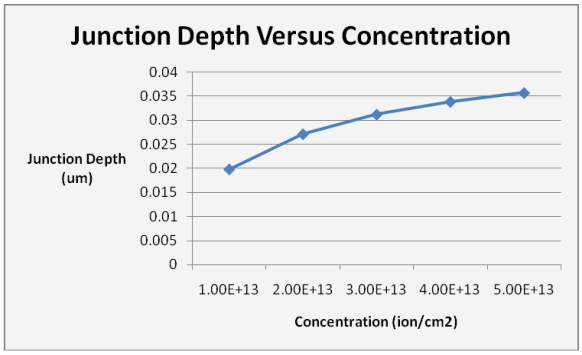

Figure 13: Graph junction depth versus concentration

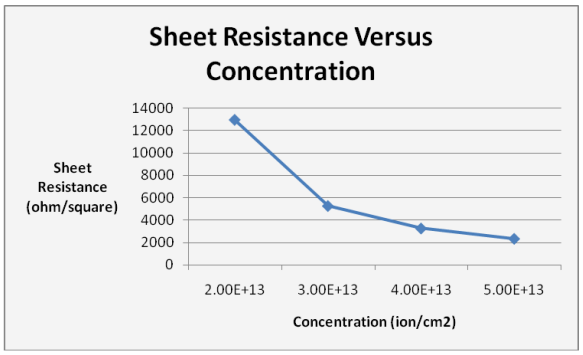

Figure 14: Graph sheet resistance versus concentration

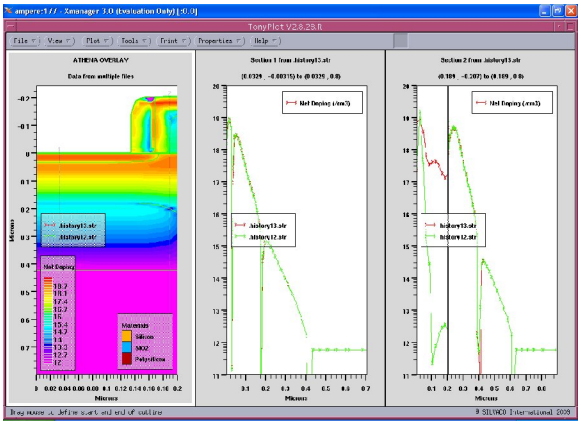

Figure 15: TONYPLOT cutline extracted at gate and source/ drain for concentration of 3e13 ions/cm^2 using Arsenic for Dual-Pearson model.

3.2.2 Gauss Model

The process continued with the Gauss model and table 7 and 8 show the results for junction depth, sheet resistance and threshold voltage when different values of concentrations applied to impurity of:

a) **Phosphorus**

Table 7: Result by using impurity Phosphorus

Dos (ion/ cm^2)	Energy (KeV))	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
1e13	20	0.0066362	1.7636e12	0.471447
2e13	20	0.0298802	37671.8	0.466588
3e13	20	0.0434143	7360.05	0.438361
4e13	20	0.0516082	3753.62	0.372705
5e13	20	0.0571726	2478.33	0.292724

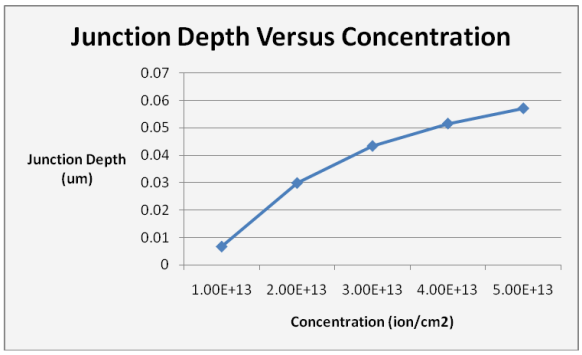

Figure 16: Graph junction depth versus concentration

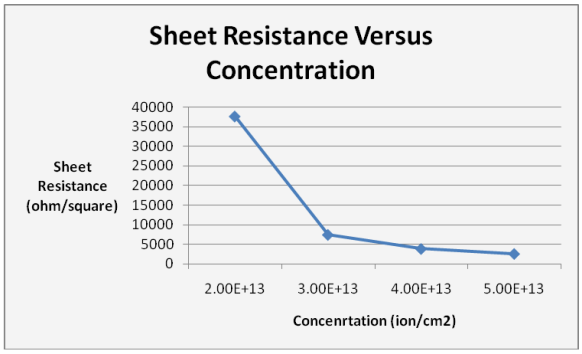

Figure 17: Graph sheet resistance versus concentration

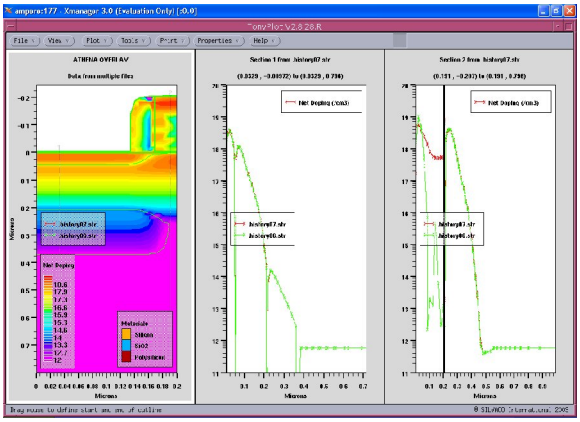

Figure 18: TONYPLOT cutline extracted at gate and source/ drain for concentration of 3e13 ions/cm^2 using Phosphorus for Gauss model.

b) **Arsenic**

Table 8: Result by using impurity Arsenic

Dos (ion/ cm^2)	Energy (KeV))	Junction depth (um)	Sheet resistance (ohm/square)	V_{TH} (V)
1e13	20	0.0204184	2.73282e6	1.87212
2e13	20	0.0296513	12261.5	0.353136
3e13	20	0.0333186	4988.21	0.340073
4e13	20	0.0353486	3075.22	0.325686
5e13	20	0.0367394	2221.87	0.292834

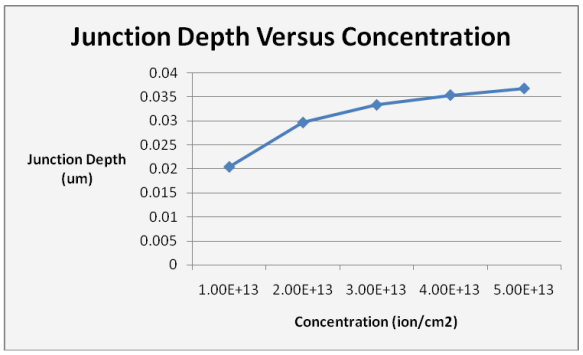

Figure 19: Graph junction depth versus concentration

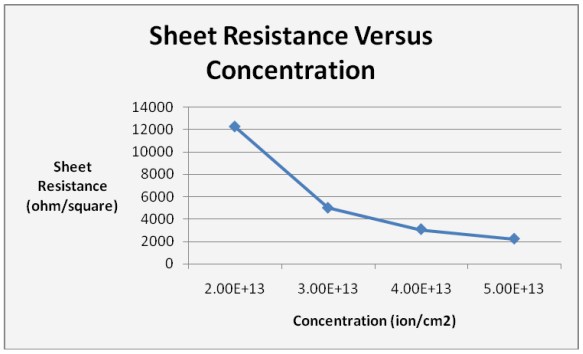

Figure 20: Graph sheet resistance versus concentration

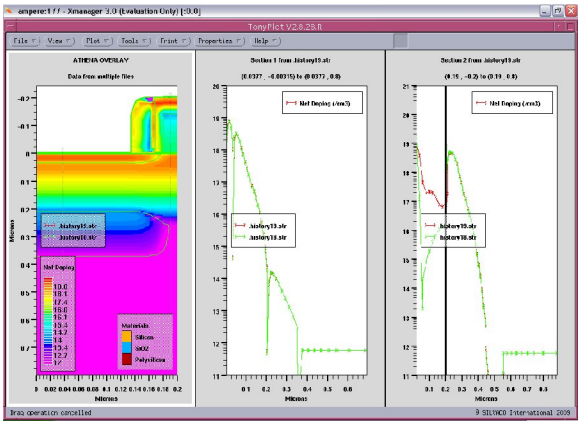

Figure 21: TONYPLOT cutline extracted at gate and source/ drain for concentration of 3e13 ions/cm^2 using Arsenic for Gauss model.

The result for junction depth as shown by Figure 12 and 15 for Dual Pearson model for Phosphorus and Arsenic respectively and Gauss model for Figure 18 and 21 for Phosphorus and Arsenic respectively. The graphs show that with the same energy but different value of concentration has significant effect on junction depth where the increasing of dosage concentration caused the junction depth shifts deeper towards the bottom of substrate.

The dopant that being doped into the polysilicon brings the extra or abundance of ions hence will cause the concentration at the sample extremely high and means that it has excess of ions. This cause the ions at high concentration to diffuse in lower concentration, for this process, the upper gate has high concentration, so the excess ions to diffuse deeper into the structure due to lower concentration. Besides, there is possibilility that during ion implantation process, there will be some dopant atoms were 'out of range' and hit the nearby surface of it should 'attack' that it should be; at the gate surface. This cause the additional of ions at surrounding and with some energy, the ions diffuse deeper into substrate since it has lower concentrations that cause the ions to diffuse.

The polysilicon is naturally N-type, but in this process, again, N-type was doped and one of the reasons was to conform on the conductivity. The pure polysilicon is not good conductor material and it has high resistance so by doping process it could reduce the resistance as shown in Figure 11 and 14 for Dual-Pearson model; Phosphorus and Arsenic respectively, Figure 17 and 20 for Gauss model; Phosphorus and Arsenic respectively, since the dopant will introduce extra free ions that can freely move around, with these free extra ions, in can increase the conductivity of the polysilicon hence reduce the resistance of the sample.

With the decreasing of the resistance of the sample, it shows that the voltage needed to turn on the device, threshold voltage (V_{TH}), from the Table 5, 6, 7 and 8 is decreasing means that only small amount of voltage needed if concentration is kept increasing.

3.3 Defect

The Defect parameters were considered during the doping process and the results corresponding to these defects were shown below with impurity of Phosphorus.

3.3.1 Phosphorus

a) **Point Defect**

Table 9: Result of Point defect by using impurity Phosphorus

Dos (ions/ cm^2)	Energy (KeV)	Point Defect	Junction Depth (um)	V_{TH} (V)	Sheet resistance (ohm/square)
5e13	20	1.0	0.0508434	0.113925	2548.28
5e13	20	1.2	0.0508434	0.113925	2548.28
5e13	20	1.4	0.0508434	0.113925	2548.28
5e13	20	1.6	0.0508434	0.113925	2548.28
5e13	20	1.8	0.0508434	0.113925	2548.28
5e13	20	2.0	0.0508434	0.113925	2548.28

b) **<311> Cluster Defect**

Table 10: Result of Cluster defect by using impurity Phosphorus

Dos (ions/ cm^2)	Energy (KeV)	Min cluster	Max cluster	Cluster factor	Junction Depth (um)
5e13	20	1.0e12	1.5e14	1.2	0.0508434
5e13	20	1.0e13	1.5e15	1.4	0.0508434
5e13	20	1.0e14	1.5e16	1.6	0.0508434
5e13	20	1.0e19	1.5e19	1.8	0.0508434
5e13	20	1.0e19	1.5e19	2.0	0.0508434

c) **Dislocation Loop Defect**

Table 11: Result of Dislocation Loop defect by using impurity Phosphorus

Dos (ions/ cm^2)	Energy (KeV)	Min Loop	Max Loop	Junction Depth (um)	N++ sheet resistance (ohm/square)
5e13	20	1.0e12	1.5e14	0.0508434	2548.28
5e13	20	1.0e13	1.5e15	0.0508434	2548.28
5e13	20	1.0e14	1.5e16	0.0508434	2548.28
5e13	20	1.0e15	1.5e21	0.0508434	2548.28
5e13	20	1.0e16	1.5e21	0.0508434	2548.28
5e13	20	1.0e17	9.9e21	0.0508434	2548.28
5e13	20	1.0e18	9.9e21	0.0508434	2548.28
5e13	20	1.0e19	9.9e21	0.0508434	2548.28

3.3.2 Arsenic

Instead of Phosphorus, the defect parameters were varied by using the impurity of Arsenic and results were shown below.

a) **Point Defect**

Table 12: Result of Point defect by using impurity Arsenic

Dos (ions/ cm^2)	Energy (KeV)	Point Defect	Junction Depth (um)	V_{TH} (V)	Sheet resistance (ohm/square)
5e13	20	1.0	0.0357456	0.278027	2338.05
5e13	20	1.2	0.0357456	0.502172	2338.05
5e13	20	1.4	0.0357456	0.278027	2338.05
5e13	20	1.6	0.0357456	0.502172	2338.05
5e13	20	1.8	0.0357456	0.278027	2338.05
5e13	20	2.0	0.0357456	0.502172	2338.05

b) **<311> Cluster Defect**

Table 13: Result of Cluster defect by using impurity Arsenic

Dos (ions/ cm^2)	Energy (KeV)	Min cluster	Max cluster	Cluster factor	Junction Depth (um)
5e13	20	1.0e12	1.5e14	1.2	0.0357456
5e13	20	1.0e13	1.5e15	1.4	0.0357456
5e13	20	1.0e14	1.5e16	1.6	0.0357456
5e13	20	1.0e19	1.5e19	1.8	0.0357456
5e13	20	1.0e19	1.5e19	2.0	0.0357456

c) **Dislocation Loop Defect**

Table 14: Result of Dislocation Loop defect by using impurity Arsenic

Dos (ions/ cm^2)	Energy (KeV)	Min Loop	Max Loop	Junction Depth (um)	N++ sheet resistance (ohm/square)
5e13	20	1.0e12	1.5e14	0.0357456	2338.05
5e13	20	1.0e13	1.5e15	0.0357456	2338.05
5e13	20	1.0e14	1.5e16	0.0357456	2338.05
5e13	20	1.0e15	1.5e21	0.0357456	2338.05
5e13	20	1.0e16	1.5e21	0.0357456	2338.05
5e13	20	1.0e17	9.9e21	0.0357456	2338.05
5e13	20	1.0e18	9.9e21	0.0357456	2338.05
5e13	20	1.0e19	9.9e21	0.0357456	2338.05

Point Defect
There are many forms of crystal point defects. A defect wherein a silicon atom is missing from one of these sites is known as a 'vacancy' defect. If an atom is located in a non-lattice site within the crystal, then it is said to be an 'interstitial' defect. If the interstitial defect involves a silicon atom at an interstitial site within a silicon crystal, then it is referred to as a 'self-interstitial' defect. Vacancies and self-interstitial defects are classified as intrinsic point defects.

Cluster Defect
This is a grouping of not more than 5 adjacent point defects.

Dislocation Loop Defect
Crystal line defects are also known as 'dislocations', which can be classified as edge dislocation, screw dislocation, or mixed dislocation, which contains both edge and screw dislocation components. An edge dislocation may be described as an extra plane of atoms squeezed into a part of the crystal lattice, resulting in that part of the lattice containing extra atoms and the rest of the lattice containing the correct number of atoms. The part with extra atoms would therefore be under compressive stresses, while the part with the correct number of atoms would be under tensile stresses. The dislocation line of an edge

dislocation is the line connecting all the atoms at the end of the extra plane.
From the results, it shows that even though the parameters of each defect were varied, it give the same result for each type of defects and it shown as in Table 12, 13and 14 which has the same value for junction depth and also for sheet resistance and threshold voltage. This not means that this defect have no effect at all, it might needs another process for these defect to have significant effects.

4.0 CONCLUSION

The polysilicon gate has been doped with the N-type impurity by using the ion implantation process with the parameters of the doping process were varied to study the effect on the junction depth. By using the extracted value of junction depth and TONYPLOT profile, the doping process were done by using two impurities; Phosphorus and Arsenic, for each of the impurities, it were studied with two types of models; Dual-Pearson and Gauss. For the doping process with concentration being varied, the junction depth shows that the increasing of the dosage of concentration cause the junction depth to be shifted deeper into the substrate due to the movement of ions from high concentration to lower concentration towards the bottom. Besides, by adding more concentration, it creates abandon of free electron to move around hence cause the lower resistivity with increasing of dosage concentration. The energy applied during doping process, energized the ions of impurity to penetrate deeper into substrate, therefore with increasing of energy applied, caused the junction depth to be shifted deeper towards the bottom. There are three types of defects to be considered for doping process; point defect, cluster defect and dislocation loop defect, but for this process, it shows no significant different when the parameters of the defect were being varied.

5.0 FUTURE DEVELOPMENT

The future development for this research, effect of polysilicon doping on junction depth, has splendid opportunity to be included for fabricating nano-scale NMOS structure with a precise junction depth. This research can be continued with the other process such as annealing to produce a very good profile of junction depth since it may used to avoid the polysilicon gate depletion in order to reduce the total gate capacitance of MOS devices. This research also might help for the suppression of the reverse short-channel effect (RSCE) in NMOS devices due to junction depth that introduced in doping process.

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