DESIGN OF LOW POWER HIGH SPEED 1-BIT FULL ADDER

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ABSTRACT

Full adder is one of the important elements in microelectronics design. In view of the fact that 1-bit full adder is the building block of most modules, therefore by improving 1-bit of full adder cell will lead to improvement of the whole system. In this paper, a 1-bit full adder cell is implemented by using gate diffusion input (GDI) XOR and XNOR gates architecture technique. This technique is used because of its benefits in reducing the power consumption, delay and the size of digital circuits. The whole simulation for a 0.18μm technology will be carried out by using Silvaco EDA tools.

TABLE OF CONTENT

CHAPTER 1
INTRODUCTION

1.1 Background Study

The demand of portable and complex digital applications has been increased rapidly from the last few decades. This issue has led numerous research efforts to take into account few constraints that are very important with the intention of improving the VLSI systems such as power consumption, performance, area, driving load capability and reliability. [1-10]

Full adder is one of the most critical parts of each processor, which is used in arithmetic logic unit (ALU), digital signal processing (DSP), floating-point unit, image and video processing, and for address generation in case of memory access or cache. In recent years, many researchers are eager to propose several kinds of different logic styles for realizing the 1-bit full adder cell since the addition operation is extensively used in the arithmetic function. Enhancing 1-bit of full adder cell will enhance the overall system because 1-bit adder cell is the building block of all these modules. [1-5]

There are two major approaches in order to improve the full adder cell performance. One is the architecture viewpoint whereby it requires analyzing the longest critical paths in the multi-bit adders and reducing the total critical path delay by shortening the path. The other approach is circuit design viewpoint on the transistor level whereby the designer proposed high performance adder core based on transistor level. [1, 4]