HIGH SPEED 4-BIT FLASH ADC WITH LOW INL AND DNL USING 0.18µm CMOS TECHNOLOGY

This thesis is represented in partial of fulfillment for the award of the

Bachelor of Engineering (Hons.) in Electronic Engineering

UNIVERSITI TEKNOLOGI MARA

(SEPT 2012 – JULY 2013)

AZRIN BIN WASLI (2010658758)
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM SELANGOR
MALAYSIA

ACKNOWLEDGEMENT

In the name of Allah S.W.T, the Most Gracious and the Most Merciful

All praises and glories to Allah who gave me the courage and patience to carry out this project.

In such a great opportunity, I would like to express my acknowledgements and appreciations to those who had contributed and assisted in completing my Final Year Project (FYP).

Foremost, I would like to express my sincere gratitude to my project supervisor, **Miss Ili Shairah Binti Abdul Halim** for the continuous support of my project, for her patience, motivation, enthusiasm and immense knowledge. Her guidance helped me in all the time of research and writing this thesis.

My sincere thanks also go to **Universiti Teknologi MARA (UiTM)** for the facilities provided. To all lecturers and staff in Faculty of Electrical Engineering, very big thanks you to all because of their sincerity and patient. My fellow colleagues should be noted for their endlessly support. I would like to extend my gratitude to everyone who has been helping me directly or indirectly throughout this project.

Last but not least, I would like to thank my family for their concern, encouragement and support throughout my life. They are one of the most valuable gifts in my life. I am very thankful because have been surround with people that always give me support and guidance.

Thank you very much.

ABSTRACT

The purpose of this paper is to design a High Speed 4 -bit Flash Analog-to-Digital Converter (ADC) with low Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). A high speed Flash ADC is obtained by selecting the best topology for the comparator and encoder design. In this paper, the best topology used for the analogue side is the open-loop comparator replacing the conventional comparator. However, some modification is made on the comparator which is by adding hysteresis circuit. The purpose is to lower the non-linearity effect on the output of the ADC. Meanwhile, for the digital side, the best topology used to design the flash ADC is the XOR encoder. The technology used to design this ADC is 0.18µm CMOS technology. The software that is used to design this Flash ADC is Silvaco Electronic Design Automation (EDA) Tools. This includes schematic-drawings, simulations, and overall checking of the circuit. Summarizing the simulation results includes a lower propagation delay comparator design which is 0.2569ns at maximum sampling frequency of 500MHz with analogue input of 1.8V. The simulation of the XOR encoder shows that the topology has the lowest power consumption which is 1.5343mW with a propagation delay of 25.4890ns. The overall DNL for this flash ADC ranging from -0.4LSB ~ 0.3LSB and the INL ranging from -0.6LSB ~ 0.4LSB. Simulation also shows an ADC power consumption of 38.8072mW and a propagation delay of 58.44ns for a 1.8V supply.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Nowadays, in this modernity-growth world, humans are increasingly relying on high-tech gadgets. Hence, demands on the high quality yet simple and user-friendly gadget is becoming a complex challenges for the gadget producers. Since vast majority of signal processing is done digitally, while signal in nature is analogue, synchronization between these two types of signals is highly needed. The main question is how to synchronous between this two signals. This is where data conversion becomes important.

There are two types of signal converter which are Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC). ADC converts analogue signal from surrounding or nature to digital signal form which is '1' and '0' while DAC, vice versa. The converter that is going to be discussed more in this thesis is ADC.

1.2 BACKGROUND OF STUDY

Every devices and gadgets nowadays consist of integrated circuits (ICs) that process data mainly in digital. To convert the analogue signal from the nature into digital that can be processed by the digital signal processors, Analog-to-Digital Converter (ADC) is needed [1]. In a high-rate data transfer