SIMULATION STUDY OF 4-BIT AND 8-BIT KOGGE STONE PARALLEL PREFIX ADDER CIRCUIT CHARACTERISTICS USING SILVACO

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ABSTRACT

This paper describes the design of Radix-2, Radix-3 and Radix-4 of 4-bit and 8-bit Kogge Stone Parallel Prefix Adder (KSPPA) architecture. The objective is to study and investigate the effects of these different radix to the various characteristics of KSPPA in terms of logical depth, number of transistors used, propagation delay, and average power consumption. The simulation study is carried out by Gateway SILVACO EDA Tools software and the design is mapped for a 0.18μm CMOS technology with 1.8V of supply voltage. The result shows that for 4-bit KSPPA, the Radix-4 is the best design while Radix-2 is the worst design, as Radix-4 reduced logical depth by 50%, reduced transistors used as much as 23%, 3% faster, and lower average power consumption by 1.2%. Then for 8-bit KSPPA, Radix-3 is the best design while Radix-2 still the worst design, as Radix-3 reduced logical depth by 50%, reduced transistor used as much as 18%, 9% faster, and lower average power consumption by 6.6%.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

In electronics, an adder is a digital circuit that performs addition of numbers. The most common adders operate on binary numbers. There are two types of adder that are; half adder and full adder. A half adder is a logic circuit that performs one-digit addition. It requires two inputs, A and B and the output produced are the sum S and carry-out Cout [1]. The truth table and circuit for half adder is shows in Table 1.1 and Figure 1.1 respectively. A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers often written as A, B, and C_{in}. The full adder produces a two-bit output sum typically represented with the signals C_{out} and S [1]. A full adder can be implemented simply by joining two half adder by an OR gate. The truth table and circuit for full adder is shows in Table 1.2 and Figure 1.2 respectively.

Table 1.1. Truth table of half adder

Input		**Output**	
A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

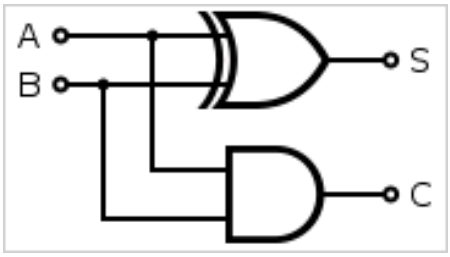

Figure 1.1. Full circuit of half adder [2]