



## **SIMULATION OF BREAKDOWN VOLTAGE ON NMOS TRANSISTOR**

**WAN NUR AMANI BT WAN NORDIN**

**THIS THESIS IS SUBMITTED IN PART FULFILLMENT OF THE  
REQUIREMENT FOR THE DEGREE BACHELOR OF ENGINEERING (HONS.)  
ELECTRONIC**

**FACULTY OF ELECTRICAL ENGINEERING  
UNIVERSITI TEKNOLOGI MALAYSIA**

**JULY 2013**

## **ACKNOWLEDGEMENT**

First, I would like to wish my grateful to Allah S.W.T. for blessing and allowing us to complete this project.

Besides, we would like to thank to my supervisor Mr. Azrif Manut for the valuable guidance and advice. He inspired me greatly to work in this project. His willingness to motivate me contributed tremendously to my project. I also would like to thank him for showing me some example that related to the topic of our project. I also, would like to thank to Mr. Mohd Rofie from MIMOS because gave me plenty of advice knowledge and information about my project.

Also, I would like to take this opportunity to thank to the Fakulti Kejuruteraan Elektrik for offering this subject. It gave us an opportunity to yield own project with the basic that we are learn.

Finally, an honorable mention goes to my families and friends for their understandings and supports on completing this project. Without helps of the particular that mentioned above, I would face many difficulties while doing this project.

## ABSTRACT

The simulation of Breakdown Voltage of an NMOS transistor is investigated using Athena/Devedit/Atlas of SILVACO software. The doping profile is modified, resulting in change of breakdown voltage. The doping profiles of the drain drift region, the p channel region and the length of the drift region play an important role in determining the breakdown properties and on state resistances of these devices. The simple model is used in this simulation for determine the doping profile and drive-in diffusion at the drain that give impact to the breakdown voltage. The dependence of breakdown voltage is studied based on device and process simulation. The possible location of breakdown voltage is at  $n^+$ -p junction. The profile doping is change based on the implant dose due to raising the breakdown, where is implantation dose proportional to implantation time. Current-voltage (I-V) characteristics curves and structure that show the impact gent rate of device were obtained from the simulation. The structure has been simulated using a process simulator and device characteristics were obtained using a device simulator. The breakdown voltage in the range of 8.9V to 9.156V has been obtained from different drain implant dose and drain drive-in time.

***Keywords-component; breakdown voltage; channel length; doping profile; MOSFET;***

## TABLE OF CONTENTS

<b>CHAPTER</b>	<b>DESCRIPTION</b>	<b>PAGE</b>
	<b>DECLARATION</b>	i
	<b>DEDICATION</b>	ii
	<b>ACKNOWLEDGEMENT</b>	iii
	<b>ABSTRACT</b>	iv
	<b>CONTENTS</b>	v
	<b>LIST OF TABLES</b>	vii
	<b>LIST OF FIGURES</b>	viii
	<b>LIST OF ABBREVIATIONS</b>	
	<b>LIST OF APPENDICES</b>	x
<b>1</b>	<b>INTRODUCTION</b>	1
	1.1 BACKGROUND	1
	1.2 PROBLEM STATEMENT	6
	1.3 OBJECTIVE	6
	1.4 SCOPE AND LIMITATION OF THE STUDY	7
	1.5 SIGNIFICANT OF STUDY	7
<b>2</b>	<b>LITERATURE REVIEW</b>	8
	<b>2.1 BREAKDOWN MECHANISM</b>	8
	2.1.1 AVALANCHE BREAKDOWN	8
	2.1.2 SURFACE BREAKDOWN	9
	2.1.3 SNAPBACK BREAKDOWN	10
	2.1.4 GATE OXIDE BREAKDOWN	11
	<b>2.2 PUNCHTHROUGH IN SHORT CHANNEL MOSFET</b>	12
	<b>2.3 BREAKDOWN VOLTAGE OF A FET TRANSISTOR</b>	13

# CHAPTER 1

## INTRODUCTION

### 1.1 BACKGROUND

The standard MOSFET structure consists of a metal gate, a layer insulating oxide and a silicon substrate and the source and drain is general structure that is lightly doped p-type substrate and it usually heavily doped with n-type semiconductor that have been embedded. A metal (or poly-crystalline) gate covers the region between source and drain, but is separated from the semiconductor by the gate oxide. Nowadays, the oxide thicknesses are used is 1.5nm where it is like one fifty-thousandth of the width of human air. In 2007 less than 1nm is necessary and appropriate only 4 atomic layers [1, 2]. In this oxide thickness, quantum mechanical tunneling current pass through the oxide. At these thicknesses, quantum mechanical tunneling becomes restrained. From the MOSFET structure show below, the symbol n+ is used to drop off this heavy doping. Figure 1.1 shows the idealized MOSFET structure and circuit symbol of an n-MOSFET. Besides that, MOSFET is transistor used for amplifying or switching electronic signal. MOSFET divided into four terminal devices with source (S), gate (G), drain (D), and body (B) terminal.

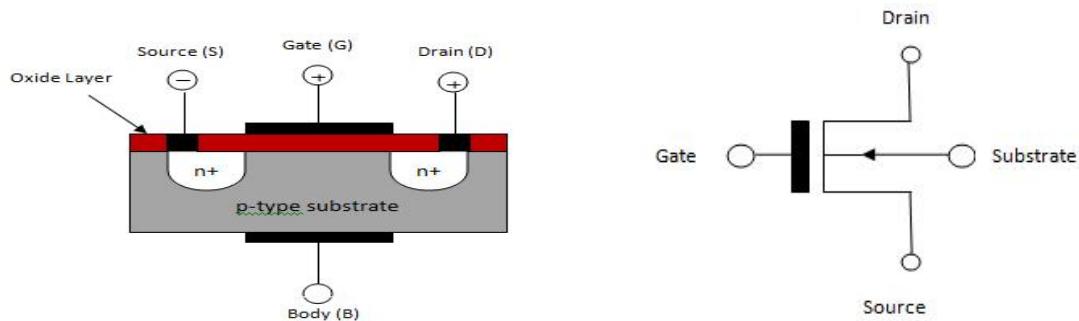


Figure 1.1: Idealized MOSFET structure and circuit symbol of an NMOS