COMPARISON STUDY OF LIGHTLY DOPED DRAIN (LDD) AND DOUBLE DIFFUSED DRAIN (DDD) TO OVERCOME HOT CARRIER EFFECT ON 0.3μm NMOS

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UNIVERSITI TEKNOLOGI MARA
SHAH ALAM, SELANGOR
MALAYSIA

MOHD KHAIRI BIN MUHAMMAD
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM
SELANGOR DARUL EHSAN

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ABSTRACT

The aim of this project is to present the analysis and simulation of the comparison of Light Doped Drain (LDD) and Double Diffuse Drain (DDD) to overcome Hot Carrier Effect on 0.3um NMOS device. The project started with designing the NMOS device using the SILVACO TCAD simulation software. Silvaco TCAD is used to measure substrate current (I_{sub}), gate current (I_{gate}), gate voltage (Vg) at maximum I_{sub} and gate voltage at maximum I_{gate} due to impact ionization that occurred during hot carrier effect. I_{sub} and I_{gate} are directly showed the hot carrier effect in NMOS device.

The investigation is start with the LDD method to overcome the hot carrier effect. The LDD method is designing at Silvaco TCAD first and then analyzes the data needed. In LDD, two investigations are analyzed that are investigation of variation n- concentration and variation of energy implant of n- concentration. After that, the project will continued with the DDD method to overcome the hot carrier effect. In DDD, an investigation is analyzed that is investigation of variation of n- concentration.

The data that collected, I_{sub}, I_{gate} and Vg will be analyzed. From the analysis, it can be conclude that both of the method can be use to overcome the hot carrier in 0.3um NMOS device. Compare with LDD and DDD methods, it was concluded that using LDD is better than DDD in 0.3μm NMOS by 28.25% reduction for I_{sub} and 70.5% reduction for I_{gate}.

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CHAPTER I

INTRODUCTION

1.0 Introduction

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a device used to amplify or switch electronic signals. The MOSFET includes a channel of n-type or p-type semiconductor material and is accordingly called a NMOS or a PMOS [1].

NMOS transistors consist of three terminals. Those are gate, drain or source, and substrate [2]. The drain and source are made from n-type for NMOS. The source and substrate are both grounded and the device will operate, or in other words, a drain current (I_D) will be induced based on voltages applied at the gate (V_G) and drain (V_D) of the transistor. Every NMOS transistor contains a threshold voltage (V_{th}) which is constant and unique for each transistor. In order for the transistor to operate, V_G must be greater than $V_{th.}$ Once this condition has been met, the resulting drain current can be controlled by the voltages supplied at the gate and the drain.

With device feature size being scaling down, hot carriers is become a serious constrain on device scaling and hot carrier reliability is one of the major concern in modern technology [1] [2]. The term hot carriers refers to either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor device. Because of their high kinetic energy, hot carriers can get injected and trapped in areas of the device where they shouldn't be and forming a space charge that causes the device to degrade or become unstable. The term hot carrier effects, therefore, refers to device degradation or instability caused by hot carrier injection [5].

Without consider decreasing the operating voltages in NMOS device, the electrical fields in the devices will increase [3]. Due the electric field increase in the silicon gate and around the drain, the hot carrier becomes a critical problem [2]. The acceleration of the channel carriers causes them to collide with Si lattice atoms, creating dislodged electron-hole pairs in the process. This phenomenon is called as impact ionization, with some of