HOLE MOBILITY ENHANCEMENT OF P-MOSFET USING STRAINED SILICON, SiGe TECHNOLOGY

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ABSTRACT

In this project, the hole mobility enhancement of PMOS are studied using SiGe technology. Silicon Germanium (SiGe) are used to increase drive current or hole mobility in the drain and source region. The performance improvements of devices with a gate length of 0.9 μm, 0.8 μm and 0.7 μm were considered. The first part of this project is reviewed about the effect of using SiGe in PMOS process to calculate the mobility. 100% of mobility enhancement using SiGe was observed compared to conventional PMOS SiGe. The second part covers the characteristics for variation of SiGe thickness. Therefore, using SiGe is an efficient method for improving PMOS device performance.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Normally, the drive current of NMOS is larger compared to PMOSFET. After introduced SiGe, the performance of PMOS becomes faster and shown improvement. The concept of combining silicon (Si) and germanium (Ge) into an alloy for use in transistor has been introduced [1]. Nowadays, new technology of introduced strain in silicon channel of MOSFETS is well accepted [2].

Hole mobility is a parameter which is measure of hole scattering in a semiconductor proportionally factor between hole drift velocity and electric field. In addition, it is toward conductivity and hole concentration in semiconductor, due to its higher effective mass. Hole mobility is typically significantly lower than electron mobility.

Increasing the mobility of the semiconductor will improve drive current and transistor speed. This can be achieved by using SiGe. Silicon germanium (SiGe) substrate had exposed enhancements of hole mobility in strained silicon layers [3]. The hole mobility enhancement depends on the current flow direction and the maximum enhancement factor along the direction.

With the application of strain, the hole effective mass becomes highly anisotropic due to band warping. The energy levels become mixtures of the pure heavy, light and split-off bands. Therefore, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to energy splitting [4]. Theory predicts that the characteristics of hole-type SiGe device can match that of the electrons, an important step for continuing the efficiency of CMOS device.

Strained Silicon concept that utilized elastic relaxation of a buried compressive SiGe layer to induced tensile in the channel and calculate the channel stress for device structure with a different gate length [5]. The channel length is defined as the distance between its