STUDY ON THE EFFECT OF THE POLYSILICON DOPING ON THE JUNCTION DEPTH IN THE 65 NM STRUCTURE

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"THERE'S LIGHT AT THE END OF THE TUNNEL".

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ABSTRACT

An analysis on the effect of the polysilicon doping on the junction depth in the 65 nm structure was conducted in this paper. Several parameters presented in the polysilicon doping process were investigated and the TonyPlot profile for the junction depth was developed to help understanding the polysilicon doping effect which is crucial to produce stable threshold voltage and also how some of these parameters have effect on the n^{++} sheet resistance. For this doping process, it was conducted using ion implantation technique with two type of impurities; phosphorus and arsenic on crystalline material. The cutline to extracting the junction depth at gate and source/drain in TonyPlot was done for investigation in dependence of the polysilicon doping profile. All simulations were done by using SILVACO.

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CHAPTER 1
INTRODUCTION

1.0 BACKGROUND

It is generally recognized that miniaturization is the key to improve performance and functionality of an integrated circuit technology. As CMOS devices are scaled down to nanometer and below, with the increased doping levels and reduction of channel length and gate oxide thickness, junction depth profile is becoming a significant contributor to stability of threshold voltage in CMOS circuits[1].

Different methods of doping procedure has been introduced to improve the thermal diffusion process in order to find the better way in producing the precise distribution of impurities in which a better electrical characteristics of polysilicon films successfully tailored into specific application since for the modern device, the thermal processing must be minimized for suppressing dopant diffusion[2,3]. Ion implantation is another alternative technique of introducing such impurities into polysilicon with a more precise manner and mostly employed to forming shallow junctions. The dopant atom is fired into the polysilicon surface through accelerated ions with specified energies. The latter provides a better lateral registration of doped regions and superior control of dopant concentration, depth and uniformity. Besides, ion implantation also offers better control of the doping process, resulting in higher reproducibility of electrical parameters and also improved yield[4].

The development of polysilicon technology was driven by the use of polysilicon as a gate electrode or as an intermediate conductor in two-level structures for integrated circuits. In CMOS processes particularly, one of the main reasons for using the polysillicon is due to the fact that polysilicon allows the integration of “dual-flavoured” gates: p- and n- type polysilicon for PMOS and NMOS, respectively. Grain sizes and the surface texture of these films are functions of the polysilicon deposition and doping conditions as well as subsequent oxidation and thermal cycle[5]. In CMOS devices, the polysilicon gate must