

**THE EFFECT OF ETCHING PROCESS OF NMOS STRUCTURE
USING SILVACO TCAD TOOLS**

Thesis is presented in partial fulfilment for the award of the
Bachelor of Engineering (Honours) Electrical
UNIVERSITI TEKNOLOGI MARA

NOVEMBER 2008



MOHD SHAHRIR BIN ABD RAHIM
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM
SELANGOR, MALAYSIA

ACKNOWLEDGEMENTS

With the highest praise to Allah which gives the author the energy and spirit to complete this project successfully. The author would like to express sincere appreciation and gratitude to Mr. Uzer Mohd Noor as the respective supervisor and Assoc. Prof. Dr. Mohamad Rusop Mahmood as a co-supervisor for this research.

Special thanks to the lecturers and management of Faculty of Electrical Engineering, Universiti Teknologi MARA especially to Mr. Suhaimi Ahmad for provide tools at Solar Cell Laboratory for this research. My sincere appreciation to the PhD student, Mr. Mohd Zainizan Sahdan and Master students, Mr. Hafiz Mamat and Mr. Khairul Ahmad for giving their hand, criticism and ideas in making this project a success. Without their generosity, this research would not be possible to complete.

Not to forget, I also thank to all my colleagues; Mr. Muhamad Yunus Yahaya, Mr. Ayub Bakri, Miss Suziana Omar, Mr. Muhammad Redzuan Mokhtar, Miss Azmira Ahmad and Miss Ziadora Ibrahim for their encouragement and support.

Last but not least, deepest appreciation to the author's family for the faith instilled as a step in manoeuvrings this life.

Above all, I thank Allah for making this journey possible.

Thank you.

MOHD SHAHRIR BIN ABD RAHIM

Faculty of Electrical Engineering

Universiti Teknologi MARA (UiTM)

40450 Shah Alam

Selangor Darul Ehsan

ABSTRACT

The effect due to the etching process of NMOS structure using Silvaco TCAD tools software was investigated using different etching methods by varying the etch rate and divergence rate. The etching methods are isotropic wet etching method and isotropic RIE etching method where the length of polysilicon gate and threshold voltage were decreased by increasing the etch rate. The chemical RIE etching method provided highly selectivity and directionality gives various divergence rates. The directional RIE etching method gave similarities in term of etch profile, junction depth and threshold voltage characteristic compared to the reference geometrical etching method for any etch rate and divergence rate.

TABLE OF CONTENTS

DECLARATION.....	i
DEDICATION.....	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT.....	iv
TABLE OF CONTENTS	v
LIST OF FIGURES	vii
LIST OF TABLES	ix
ABBREVIATIONS.....	x

CHAPTER 1

INTRODUCTION.....	1
1.1 PROJECT BACKGROUND	2
1.2 OBJECTIVES OF RESEARCH	6
1.3 SIGNIFICANCE OF RESEARCH	6
1.4 SCOPE OF WORK	7
1.5 ORGANIZATION OF THE THESIS	8

CHAPTER 2

LITERATURE REVIEW	9
2.1 OVERVIEW OF NMOS	10
2.2 POLYSILICON GATE	11
2.3 ETCHING METHOD	12
2.4 ETCH PROFILES	13
2.5 JUNCTION DEPTH	15
2.6 THRESHOLD VOLTAGE	16

CHAPTER 3

DESIGN METHODOLOGY	19
3.1 SILVACO TCAD TOOLS	20
3.1.1 Overview of Athena	21
3.1.2 Overview of Atlas	21
3.2 DESIGN METHODOLOGY OF PROCESS AND DEVICE SIMULATION	22
3.2.1 Grid and Substrate	24
3.2.2 Gate Oxide Layer	24
3.2.3 Ion Implantation	25
3.2.4 Polysilicon Gate	25
3.2.5 Deposit Photoresist	25

CHAPTER 1

INTRODUCTION

This project uses Silvaco Technology Computer Aided Design (TCAD) tools software as a fabrication simulation process and device simulation tools. The first chapter of this report will discuss the project background underlying the etching process and the simulation process of N-type Metal Oxide Semiconductor Field Effect Transistor (N-MOSFET) in general. The objectives, significance of research, scope of work and thesis arrangement were also mentioned in this chapter.