A Low Power 0.18µm CMOS Technology Integrating Dual-Slope Analog-to Digital Converter

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***Abstract*— In this paper, a 4-bit integrating dual slope analog-to digital converter (DS-ADC) is designed which consumes low power and simplicity but slow conversion time utilizing a Silvaco Electronic Design Automation (SEDA) tools with an advanced 0.18µm CMOS Technology using 1.8V power supply. This ADC contains three main components of integrator, comparator and control logic at which the integrator is realized with a two-stage operational amplifier (op-amp) that provides sufficient gain, ICMR and power dissipation. Simulation confirms that the proposed ADC architecture shows a power efficiency of 2.47392mW.**

Keywords- Dual Slope ADC, Two stage op-amp, Integrator, Comparator, Control Logic

I. INTRODUCTION

A dual slope integrating ADC (DS-ADC) provides a high accuracy, high resolution, inexpensive, good noise rejection, and ideal for digitizing low bandwidth signal. They are commonly found in slow-speed, low sensitive to passive device variation applications such in digital multimeter, panel meter and even medical instrumentations. DS-ADC integrates an unknown input voltage (V_{in}) for a fixed amount of time (T_{int}), then "de-integrates" (T_{deint}) using a known reference voltage (V_{ref}) for a variable amount of time. Operational amplifier is the key analog component of DS-ADC and the most widely used circuit approach for the implementation of MOS op-amp is the two stage configuration which provides good common mode range, output swing, voltage gain and CMRR in a simple circuit [6-7]. There are many types of analog-to-digital converters which can be classified according to the concept on which they were designed. For example, there are Charge-Coupled ADC, Digital-Ramp ADC, Successive Approximation ADC, Voltage-to-Frequency ADC, Integrating ADC, Delta-Sigma ADC, Flash ADC and some of these converters require the use of digital-to-analog converters (DACs), analog comparators and some logic modules. Integrating ADCs are commonly designed either in single or dual slope by which the single slope approaches is less accurate and make measurement repeatability quite difficult to attain [1-3]. The accuracy of a single slope ADC depends on the resistance and capacitor used. Thus to eliminate the dependency of resistance and capacitor, there is a need of a Dual slope ADC and this ADC requires no DAC as illustrated in Fig. 1 [1-4].

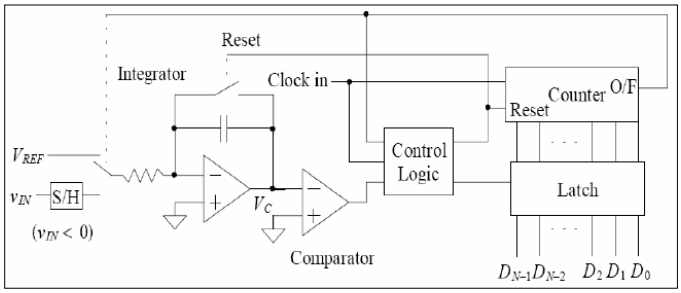


Figure 1. DS-ADC architecture

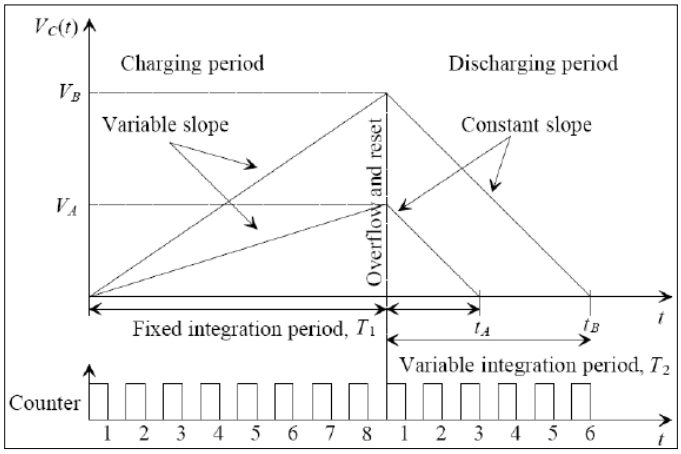


Figure 2. DS-ADC timing analysis

Fig. 2 clarified on the behavior of the DS-ADC. The first integration is of fixed length, dictated by the counter, in which the sample-and-held signal is integrated, resulting in the first slope. After the counter overflows and is reset, the reference voltage is connected to the input of the integrator. Since V_{in} was negative and the reference voltage is positive, the inverting integrator output will begin discharging back down to zero at a constant slope. A counter again measures the amount of time for the integrator to discharge, thus generating the digital output. Notice that the first slope varies according to the value of the input signal, while the second slope, dependent only on V_{ref}, is constant. Similarly, the time required to generate the first slope is constant, since it is limited by the size of the counter. However, the discharging period is variable and results in the digital representation of the input voltage [2].Primary emphasis is also placed on

CMOS amplifiers because of their more widespread use and that they are the key elements of most analog subsystems, particularly in converters which then making the performance of many systems is strongly influenced by op-amp performance [6-7]. The proposed design will lead to a better performance of integrating ADC in terms of its power, error rejection and circuit simplicity in comparison to other ADC architectures and it is specially design in an advanced 0.18µm CMOS technology and a two stage op-amp as a key for increasing system performances. The design is wholly employed by Silvaco EDA Tools beginning from schematic, testbenches, simulation and verification.

II. METHODOLOGY

A. Flow Chart

Fig. 3 reveals the representation of how the different stages in the design process are interconnected and accomplished.

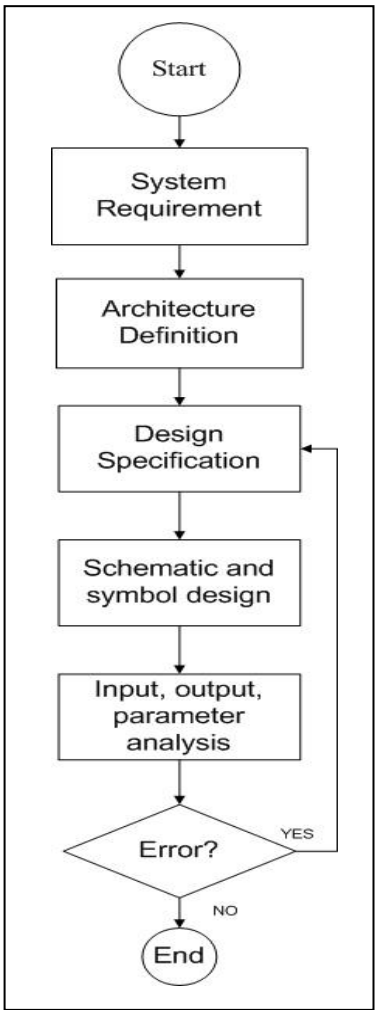


Figure 3. DS-ADC flow chart

B. Block Diagram

Fig. 4 illustrates the each module that integrates the DS-ADC as a whole complete system.

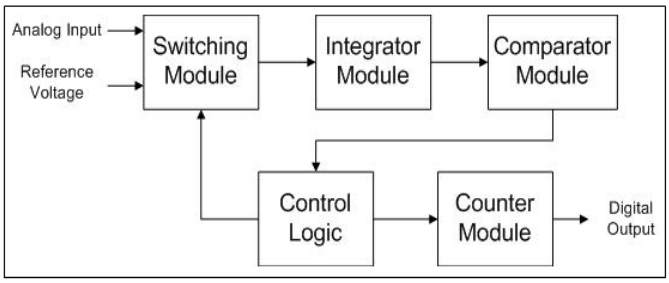


Figure 4. DS-ADC Block Diagram

C. DS-ADC Design

i. Two stage op-amp

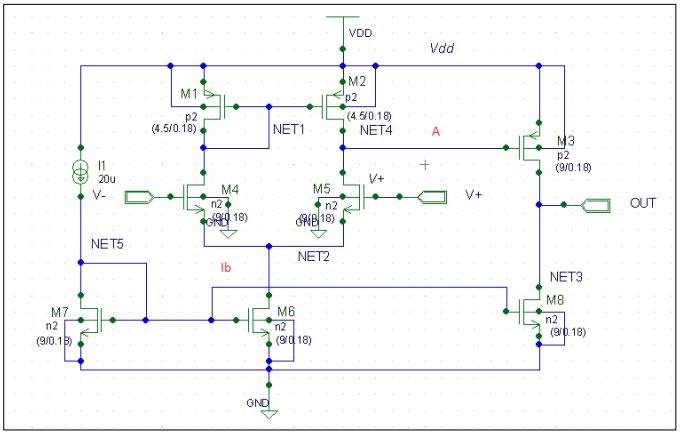


Figure 5. Two stage op-amp

Fig. 5 shows a basic two-stage CMOS op-amp configuration. The current source, I_1 provides biasing for the entire operational amplifier. M4 and M5 form a differential pair and thus the input of the first gain stage of the op amp. The current mirror formed by M7 and M6 supplies the differential pair with bias current, I_b. The input differential pair is actively loaded with the current mirror formed by M1 and M2. Node A forms the output of the first stage of the op amp. The second stage consists of M3 which is a common source amplifier actively loaded with the transistor M8. It should be noted that M8 does not provide biasing for M3, and that M3 is biased from the gate side.

ii. Integrator

Integrator is an application of op-amp that performs the mathematical operation of integration. The output responds to change in the input voltage over time and the integrator op-amp produces a voltage output which is proportional to that of its input voltage with respect to time. The general block diagram is shown in Fig. 6. It uses R and C in feedback fashion and the mathematics for determining the output for integrator is as follow:

$$\frac{dVout}{dt} = \frac{-Vin}{RC} \quad (1)$$

$$\text{or,} \quad V_{out} = \int_0^t \frac{-Vin}{RC}\, dt + C \quad (2)$$

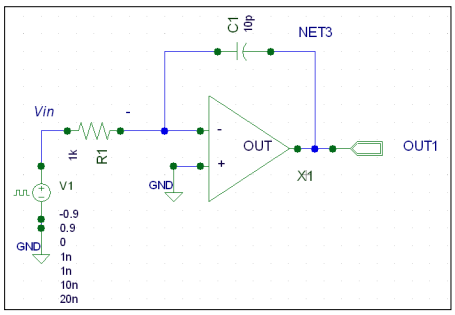


Figure 6. An integrator

iii. *Comparator*

An open loop comparator as in Fig. 7 consists of three stages which are input stage, push-pull inverter and output stage. The advantage of this circuit is that the circuit consumes minimal number of transistor and thus the circuit area is small. It basically compares between the two voltages that are applied on the amplifier terminals; and if the voltage applied on the non-inverting terminal is greater than that applied on the inverting one then the comparator output will be low (V_{OL}) else it will be high (V_{OH}).

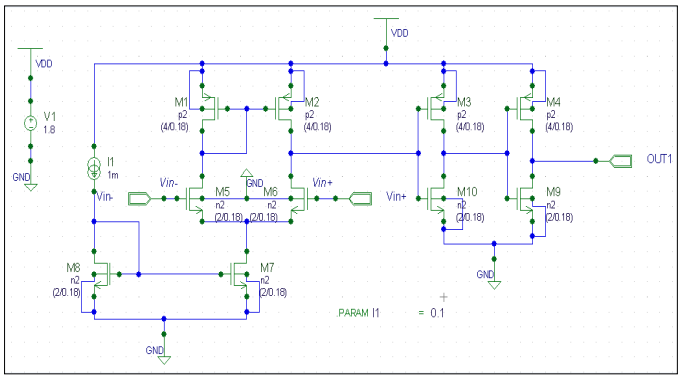


Figure 7. Comparator

iv. *Switching Module*

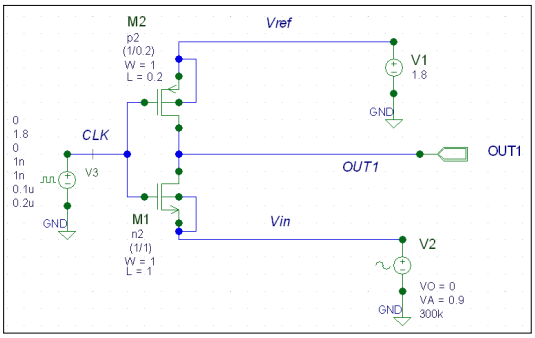


Figure 8. Inverter switch

Fig. 8 indicates the PMOS and NMOS inverter acting as a switch that whenever CLK is high, NMOS will switch on and indicate value of V_{in} at the output. Reciprocally, as CLK goes low, the switch output follows V_{ref} for PMOS switch is taking the role then.

v. *Control Logic*

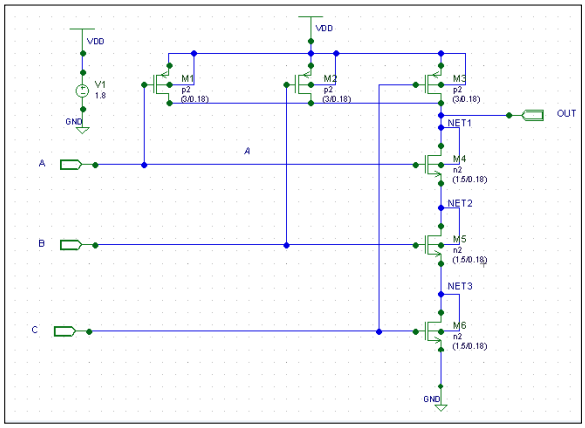


Figure 9. NAND Control logic

vi. *Counter*

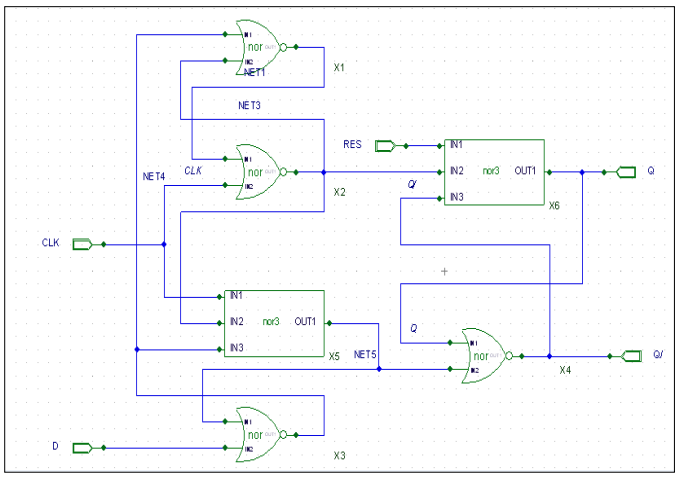


Figure 10. NOR D-flip flop

The digital part consists of control logic and a counter as shown in both Fig. 9 and Fig. 10 by which the control logic is in charge of clearing the counter and is implemented with 3-input NAND logic. A 4-bit counter is realized with the help of 1-bit counter that is design explicitly through a NOR D-flip flop.

vii. Complete System

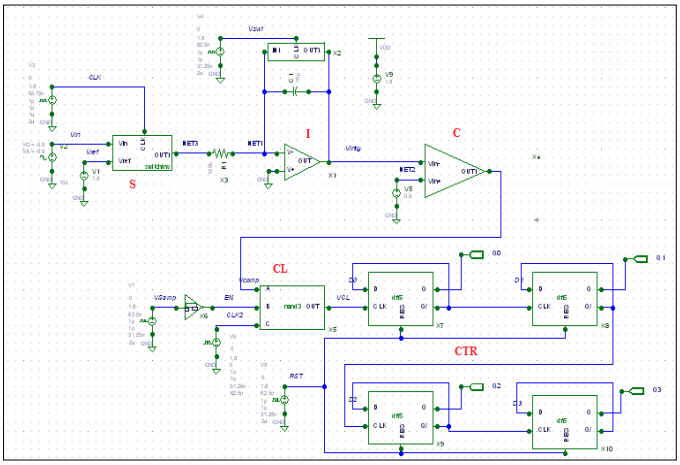


Figure 11. DS-ADC complete system

As shown in above Fig. 11, the whole complete system of DS-ADC is built by combining the modules of switching-S, integrator-I, comparator-C, control logic-CL and counter –CTR. The system is powered by 0.9V analog signal and 1.8V of reference voltage and V_{DD} at 25ºC temperature.

III. Results and Discussion

A. Two Stage Op-amp

Table I pointed out the specification results according to the circuit in Fig. 5.

TABLE I. TWO-STAGE OP-AMP DESIGN SPECIFICATION

Parameter	Specification
Input Offset Voltage	5.4mV
Gain	45.43dB
CMRR	20dB
ICMR	0.6 – 1.72V
Slew Rate	0.09V/µs
Power Dissipation	58µW

B. Integrator

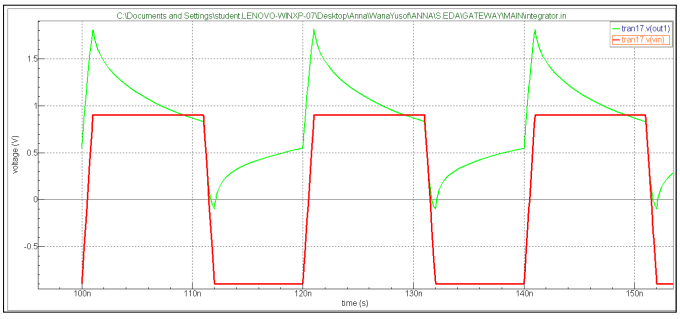


Figure 12. Integrator simulation

Fig. 12 is the transient simulation of an integrator as illustrated in Fig. 6. The negative feedback of the op-amp ensures that the inverting input will be held at 0 volts due to the virtual ground concept. If the input voltage is exactly 0 volt, there will be no current through the resistor, therefore no charging of the capacitor, and therefore the output voltage will not change.

TABLE II. VARIOUS INTEGRATOR VALUES

Resistor, R1 (Ω)	Capacitor, C1 (pF)	V_{charge} (V)	$V_{discharge}$ (V)
100	0.1	1.8	-1.8
100	1	2.0	-2.0
1k	10	1.5	-1.5
10k	10	1.2	-1.2

Table II clarified the different values of RC that make up the integrator and the corresponding output of charging and discharging values. It cannot be guaranteed what voltage will be at the output with respect to ground in this condition, but it can be said that the output voltage will be constant. However, if a constant, positive voltage (0.9V) is applied to the input, the op-amp output will fall (discharging) at a linear rate, in an attempt to produce the changing voltage across the capacitor necessary to maintain the current established by the voltage difference across the resistor. Conversely, a constant, negative voltage (-0.9V) at the input results in a linear, rising voltage (charging) at the output. The output voltage rate-of-change will be proportional to the value of the input voltage.

C. Comparator

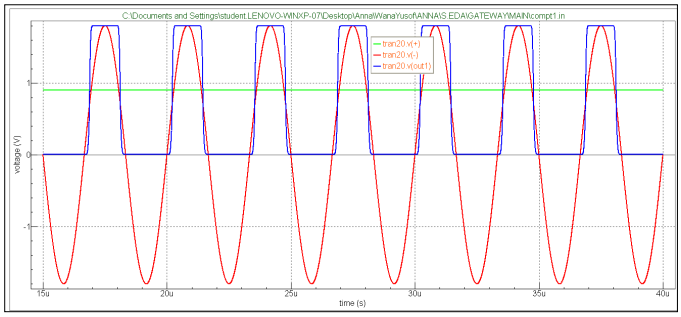
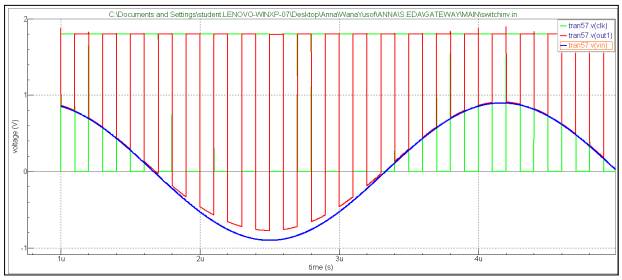


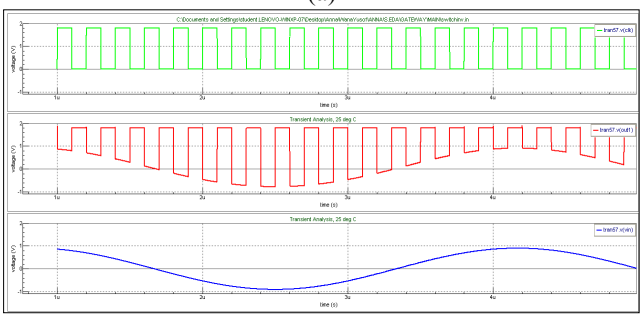
Figure 13. Comparator simulation

As mentioned earlier, a comparator basically compares between the two voltages that are applied on the amplifier terminals. The circuit in Fig. 7 is simulated with 0.9V as a reference voltage (V+) and a sinusoidal 1.8V into the inverting input (V-) that produced a binary output of ‘1’ as long as the inverting input potential is higher than that of reference voltage as described in Fig.13.

D. Switching Module



(a)



(b)

Figure 14. Switching simulations

When the input voltage, V3 as in Fig. 6, is the higher supply rail, the output (referring to Fig.14), V_{out}, goes to V2 (the supply voltage). The NMOS device at the bottom turns on and the PMOS device on top shuts off. When the input goes to low, the output goes to V1 (reference voltage) turning on the PMOS and turning off the NMOS. Table III summarized the operation of the switching circuit in Fig. 8

TABLE III. INVERTER SWITCH

Clock, CLK	Output Voltage, V_{out}
1	V_{in}
0	V_{ref}

E. Control Logic

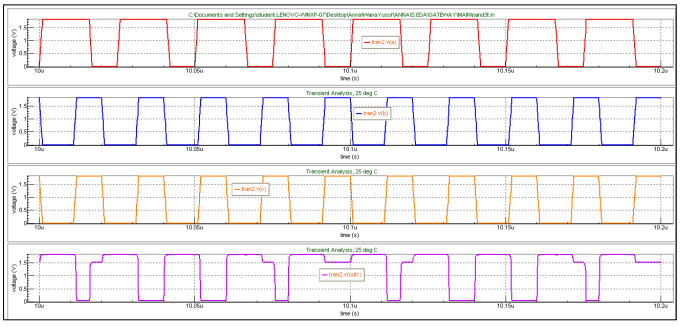
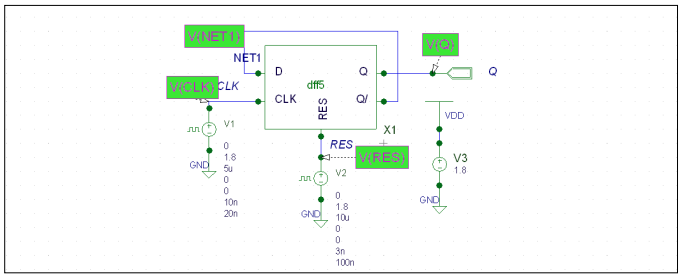


Figure 15. Control logic simulation

Since the control logic module is designed on a simple 3-input NAND gate, the output produced is easily achieved. A high logic of '1' would always true if either input of the gate is '0' whereas logic '0' at the output when all 3-inputs are at high logic as proved in Fig. 13 above.

F. Counter



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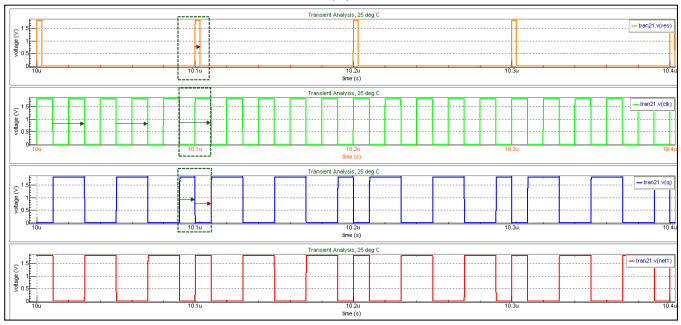

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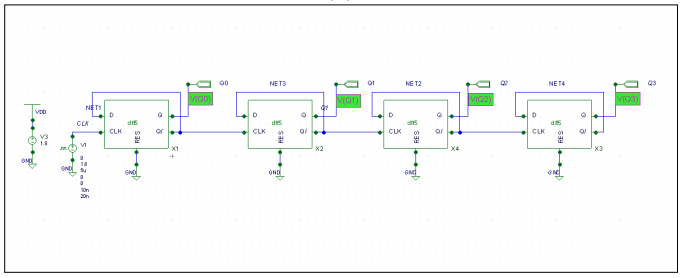
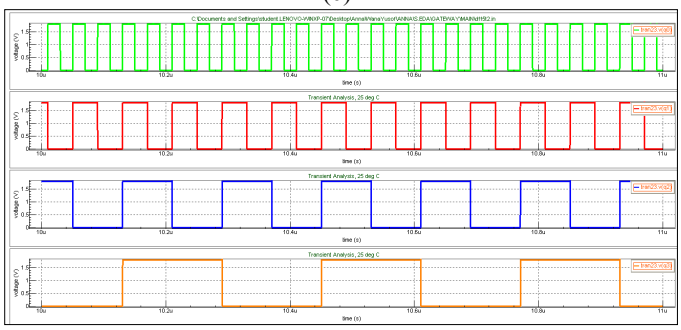


(c)



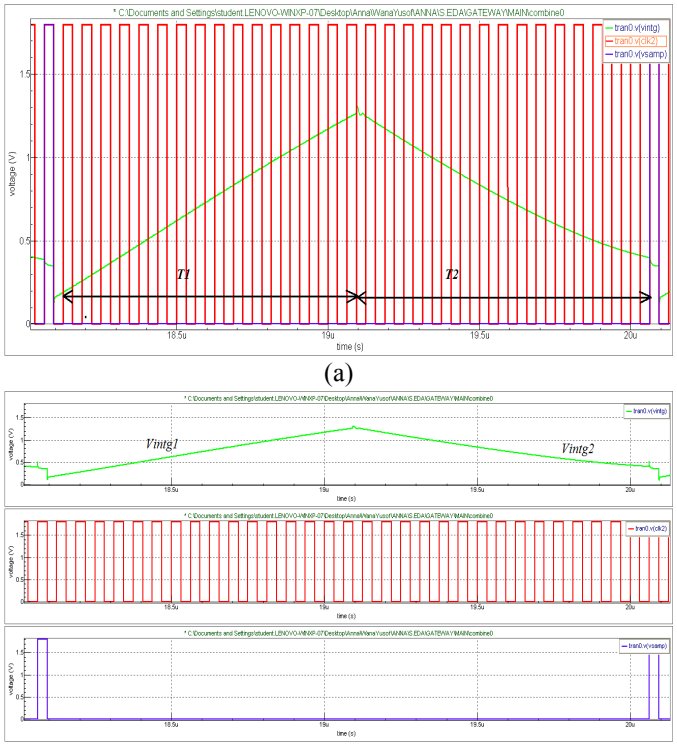
(d)

Figure 16. Counter simulation (a) 1-bit counter (b) 1-bit counter simulation (c) 4-bit ripple counter (d) 4-bit ripple counter simulation

Fig. 16 (a) is the configurations of a single bit counter with 'reset' element functioning as resetting or clearing the output, means a binary '0' will be presented at the Q output, as illustrated in Fig. 16 (b) above. The proposed DS-ADC is a 4-bit system that is realized through a ripple counter stated that

only the first flip-flop is clocked by an external clock and all subsequent flip-flops are clocked by the output of the preceding flip-flop as in both figures of 16 (c) and (d).

G. Complete System



(a)

(b)

Figure 17. Integration slope of DS-ADC

The dual-slope operation differs from the single-slope in that V_{intg} is now compared to ground and two voltages; V_{ref} and V_{in} are both integrated. Initially a negative input is connected to the integrator, ramping V_{intg} until the counter overflows. Since a negative value is being integrated on the inverting input, the integrator output will always positive and greater than zero, so the counter will continue until it overflows, which happens at 2^N clock cycles (= T1). (3) gives a value for V_{intg}. Looking at the slope (V_{intg1}/T1), the dependence on V_{in} is clear and since V_{in} is a variable, so is the slope.

$$V_{intg1} = \frac{-\int_0^{T1}\frac{Vin}{R}\,dt\;T1}{C} = \frac{Vin.T1}{RC} \qquad (3)$$

After overflow switches, V_{ref} is integrated; at the same time, the control logic triggers the reset to clear the counter. The counter now begins checking how many clock cycles are needed to ramp V_{intg} down to zero. (4) gives the value of V_{intg} for this time period, T2. Note, (4) is negative since V_{ref} is on the inverting input; this means that the integrator is now ramping down.

$$V_{intg2} = \frac{1}{C}\int_0^{T2}\frac{Vref}{R}\,dt = \frac{-Vref.T2}{RC} \qquad (4)$$

Again, looking at the slope (V_{intg2}/T2), it is clear that it will be constant since V_{ref} and RC do not change. The value of V_{intg} after T2 will be the sum of V_{intg1} and V_{intg2} and as the illustration shows in Fig. 16 (a) and (b), it should be zero.

$$V_{intg1} + V_{intg2} = 0;$$

$$0 = \frac{Vin.T1}{RC} - \frac{Vref.T2}{RC};$$

$$\frac{Vin.T1}{RC} = \frac{Vref.T2}{RC} \rightarrow \frac{Vin}{Vref} = \frac{T2}{T1} \qquad (5)$$

T2/T1 gives the digital output of the input voltage. (5) is revealing in that there is no dependence on RC. Essentially, errors in the slope of V_{intg} (determined by RC) will cancel out since the same integrator is used to calculate T1 and T2. Also, since the same clock is used to measure these times, errors in the clock such as jitter should also cancel [9]. All these calculation and result are summarized in below Table IV, referring to the complete circuit of Fig. 11.

TABLE IV. INTEGRATION ANALYSIS

Parameter	Value
V_{in} (V2)	-0.9V
V_{ref} (V1)	1.8V
Clock cycles	$2^N = 16$
R1	100kΩ
C1	10pF
V_{intg1}	1.3V
V_{intg2}	-1.3V
T1	305.6 µs
T2	286.5µs

TABLE V. DS-ADC CORRESPONDING OUTPUT

Decimal	Bit	Ideal	Actual
1	0001	0.1125	0.1401
2	0010	0.2250	0.2835
3	0011	0.3375	0.3932
4	0100	0.4500	0.4963
5	0101	0.5625	0.6101
6	0110	0.6750	0.6762
7	0111	0.7875	0.8430
8	1000	0.9000	0.9903
9	1001	1.0125	1.0630
10	1010	1.1250	1.1736
11	1011	1.2375	1.2750
12	1100	1.3500	1.3723
13	1101	1.4625	1.4609
14	1110	1.5750	1.5430
15	1111	1.6875	1.6771

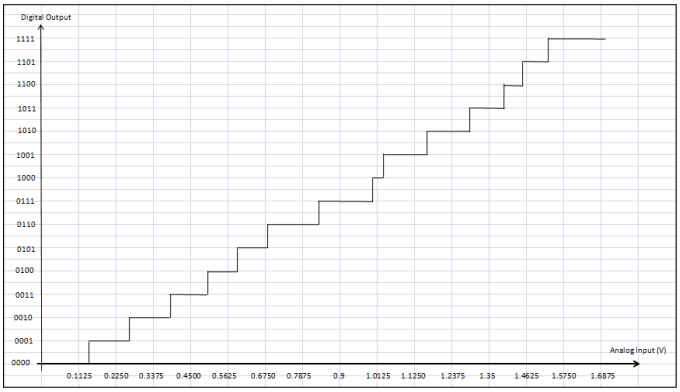


Figure 18. DS-ADC transfer curve

As tabulated in Table V, the least significant bit (LSB) refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. The LSB will always be denoted as D_0. One LSB can be defined as:

$$1LSB = V_{ref}/2^N \quad (6)$$

The value of 1 LSB for this ADC can be calculated using (6) and is the ideal step width (1/16). Therefore, with V_{ref} = 1.8V, 1 LSB = 0.1125V. Based on Fig.18, the digital output 4-bit DS-ADC is plotted versus the analog input, V_{in}. Since the input signal is a continuous signal and the output is discrete, the transfer curve of the ADC resembles that of a staircase. Another fact to observe is that the *2N* quantization levels correspond to the digital output codes 0 to 15. Thus, the maximum output of the ADC will be 1111 (2^N - 1) [2]. The overall characteristics of conversion time, power and others of the DS-ADC design are tabulated in TABLE VI.

TABLE VI. DS-ADC CHARACTERISTICS

Integrating DS-ADC	
Technology	0.18µm
Temperature	25°C
Analog Input, V_{in}	0.9V,10kHz frequency
Reference Voltage, V_{ref}	1.8V
Conversion Time	1.06µs
Power Consumption	2.47392mW

IV. CONCLUSION

A Dual Slope ADC is one valuable ADC in signal processing for its high noise immunity, low cost and low architecture but slow in speed. In this paper, a 4-bit DS-ADC has been designed and simulated in 0.18µm CMOS technology by EDA Tools. The design does not utilize any DC external biasing circuit and only need to apply V_{dd} because it consumes an independent current and voltages sources. The total power consumption of this design is only 2.474mW with 1.06µs conversion time. It is suggested as future work to enhance the DS-ADC transfer curve to be as accurate as the ideal ADC, perhaps by optimize the two stage op-amp and an extra sample-hold circuit.

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