Development of Assembly Check for TL431A

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***Abstract*—TL431A is adjustable voltage regulator which used widely in electronic industry with Vref tolerance 1% at 25C and can operate from -40C until 85C and the output from Vref (2.5V) until 36V made this voltage regulator better than zener diode. By integrate from Final Test to Assembly Check, 100% test coverage at Probe is needed. With high customers demand made TL431A the best candidate as Pilot device to migrate to Assembly Check with test time less 55mS. This paper will explain how and what the tests need to perform to make sure Probe has 100% coverage.**

Keywords: TL431A, Assembly Check, Fuse Trimming, Test System Correlation, Probe

I. Introduction

Final Test is expensive due to poor equipment utilization by many, low volume products, tested on expensive testers and handlers. Assembly Check will move almost all test of Final Test to Probe where the equipment is cheaper, clean, and inherently better utilized. Costs reduction is the key and Assembly Check will still be guaranteed via an electrical check during the device transfers to Tape and Reel.

TL431A was chosen as Pilot device because this device has high customer demand and fully trimming at Probe. With 100% of test coverage at Final Test and 60% at Probe there are some tests perform twice and this will lead to high test costs. To eliminate from performing the tests twice and overlap, Probe and Final Test coverage compared apple to apple and decided to move 5 tests from Final Test to Probe.

The tests that will integrate are Minimum Cathode Current (IK_Min), Cathode Current at 1.35V (IK_1.35V), Regulation to Maximum (Reg_Max), Voltage Cathode to Anode at 36V (VKA_36V) and Voltage Cathode to Anode at 10mA (VKA_10mA). In mean time, Fuse Trimming at Vref needs to be fixing since it affected the Final Test yield.

II. Literature Review

A. Assembly Check

Assembly Check is the project to move almost all of parametric test from Final Test to Probe. Beside to reduce cost of test, this project is to aim to produce quality product by checking Continuity, Critical Parametric and Leakage Test only using VLCT (Very Low Cost Tester) and Tape and Reel Handler. By eliminate Final Test process, Assembly Check is the process where the units are testing during idle time (around 60mS) before the units go to Tape and Reel process.

B. Final Test And Probe

Final Test is the step where the DIE with packaging will perform electrical tests which contain Continuity, Parametric, Trimming, and Leakage tests. Final Test performs with Semiconductor Automatic Test System (ATE) and IC Handler. Probe is the step where DIE without packaging (wafer) will perform electrical tests which contain Continuity, Parametric, Trimming, and Leakage tests. Probe will perform with Semiconductor Automatic Test System (ATE) and Wafer Prober.

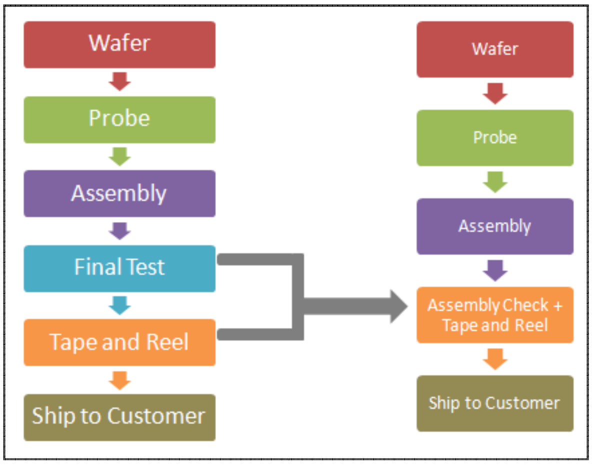


Figure 1. Final Test to Assembly Check

III. Methodology

A. TL431A

TL431A is the device was chosen to run Assembly Check as pilot device in Texas Instruments Mexico. D package was chosen as a benchmark because have high demand and easy to qualify. For preparation to move from Final Test to Assembly Check, all of the parametric tests at Final Test will be offload to Probe. There are 5 critical parametric tests for TL431A which not covered at Probe need to move from Final Test using HSM (High Speed Machine) in Mexico to Probe using ETS-500 (Eagle Test System) in Sherman to drive Assembly Check using VLCT (Very Low Cost Tester) with STI AT368.

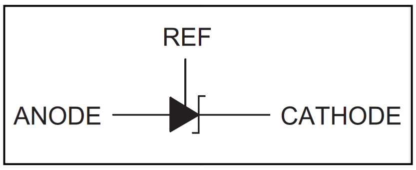


Figure 2. TL431A Symbol [1]

Ideally, from Figure 2, TL431A are contains 3 pins assignment which Anode pin, Cathode Pin and Reference Pin [1].

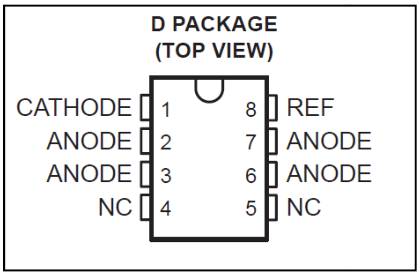


Figure 3. TL431A Pins Assigment [1]

In electronic environment and due customers design and application, from Figure 3, TL431A basiclly is D package and contains 4 of Anode pins, 2 of NC pins, 1 of Cathode pin and 1 of Reference pin [1]. 4 pins of Anode have same function and connected together on lead frame and DIE. Cathode pin and Reference pin connected separately on DIE.

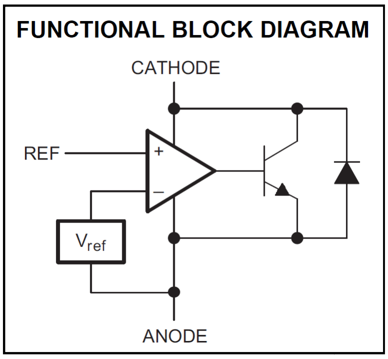


Figure 4. TL431A Block Diagram [1]

From Figure 4, TL431A is a combination between comparator, BJT and diode. Function of comparator is to compare voltage or current between Reference pin and Cathode Pin. Vref are the fuses and BJT is function to amplify the output from comparator and diode function as protection and will allow one way current flows.

B. *Vref Pre*

Vref Pre is a test to measure initial value for Reference Voltage (Vref) before the probe program zaps the 2-bits fuses. 1mA current forced to Cathode pin and Cathode pin with short together with Reference pin. Anode pin set grounded. The measurement will take from Cathode pin to Anode pin. The value from Vref Pre will use to zap 2-bits fuses inside the DIE if initial voltage at Vref Pre not equal with 2.495V.

C. *Vref Fuse Trimming*

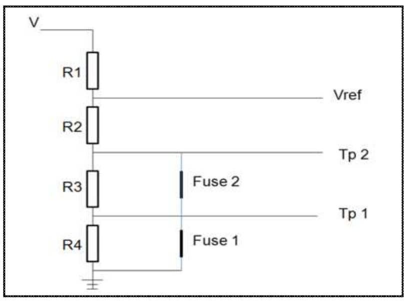


Figure 5. Integrated Fuses Configuration

Figure 5 shows the 2-bits fuses configuration need to zap at Vref and to make sure Vref value closer to 2.95V. Every selection fuse options can be calculate as below:

$$Vref\ (fuse\ 0) = V\ (R2) / (R1 + R2) \quad (1)$$

$$Vref\ (fuse\ 1) = V\ (R2 + R4) / (R1 + R2 + R4) \quad (2)$$

$$Vref\ (fuse\ 2) = V\ (R2 + R3) / (R1 + R2 + R3) \quad (3)$$

$$Vref\ (fuse\ 3) = V\ (R2 + R3 + R4) / (R1 + R2 + R3 + R4) \quad (4)$$

D. *Fuse Selection*

The original Probe programs have 4 options to choose the fuses.

TABLE I. 2-BITS FUSES TABLE

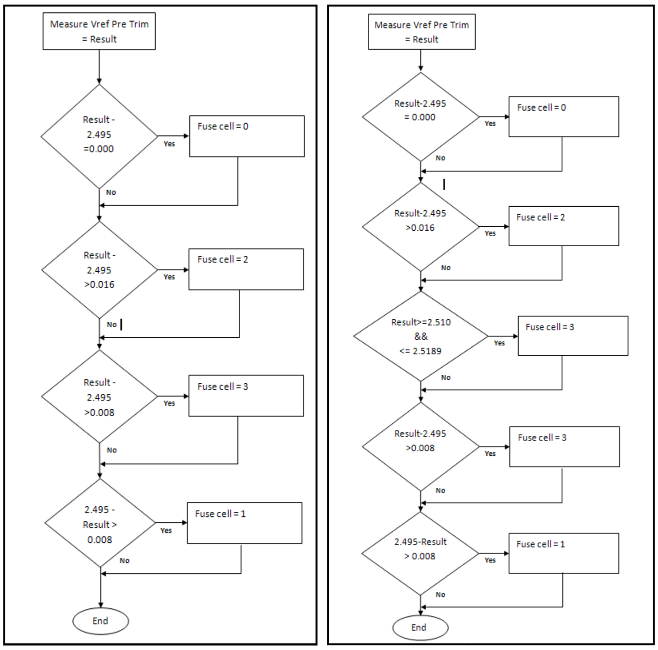
Fuse Cell	Fuse 1	Fuse 2	Voltage (V)
0	0	0	0.000
1	0	1	0.016
2	1	0	-0.032
3	1	1	-0.016

Table I shows 2-bits of fuses that every bit will represent different voltages. Every fuse uniquely represent +0.016 V and -0.032V. In the original program, there some unusual selections fuse where there critical point, the program used to select wrong fuse to zap.

TABLE II. 2-BITS FUSES SELECTION ANAYLSIS TABLE

Pre-Trim (Limit)	V	2.509	2.510	2.511	2.512	2.513	2.514	2.515	2.516	2.517	2.518	2.519
Target Value	V	2.495	2.495	2.495	2.495	2.495	2.495	2.495	2.495	2.495	2.495	2.495
Different Target and Pre-Trim	V	0.014	0.015	0.016	0.017	0.018	0.019	0.020	0.021	0.022	0.023	0.024
Fuse Voltage	V	-0.016	-0.016	-0.016	-0.016	-0.016	-0.016	-0.016	-0.016	-0.016	-0.016	-0.032
New program Fuse Cell		3	3	3	3	3	3	3	3	3	3	2
New Trim Value	V	2.493	2.494	2.495	2.496	2.497	2.498	2.499	2.500	2.501	2.502	2.487
Old Program Fuse Cell		3	3	2	2	2	2	2	2	2	2	2
Fuse Voltage	V	-0.016	-0.016	-0.032	-0.032	-0.032	-0.032	-0.032	-0.032	-0.032	-0.032	-0.032
Old Trim Value	V	2.493	2.494	2.479	2.480	2.481	2.482	2.483	2.484	2.485	2.486	2.487

Table II shows the analysis the Trim target value of 2.95V. The problem came out when Vref Pre reading from 2.510V until 2.518V, the original Probe program will choose to Fuse Cell 2 (-32mV) to zap as show in Figure 10a but when zapping Fuse Cell 3 (-16mV) would have a better choice. This is the root cause of low yield at Final Test. The Final Test limits are from 2.473 until 2.517 V and the consequences from this issue, the Vref at 10mA distribution will shift to upper limits.



(a) (b)

Figure 6. (a) Original Fuses Selection (b) Improvement Fuses Selection

Figure 6(a) shows diagrammatic how the original Probe program decides which fuse will zap to make the value of Vref closer to 2.495V. From the result from Vref Pre measured, the original Probe program will do calculation with condition as per showed above.

To fix the issue, the code in Probe program needs to modify before moving forward to Assembly Check. From Figure 6(b) shows all of the original conditions will remains the same with addition condition to make sure when Vref Pre measured Vref at 2.510 until 2.5189, the probe program will zap Fuse Cell 3.With addition condition below, the missing trim pattern recovered as showed in Figure 11 (b).

E. Vref at 10mA

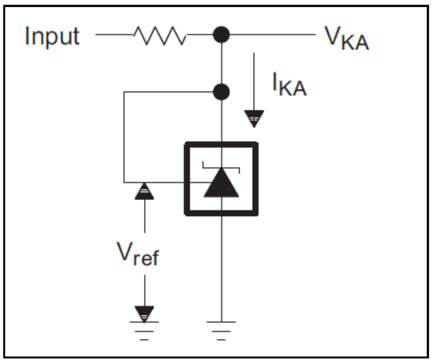


Figure 7. Vref at 10mA circuit configuration[1]

Vref at 10mA is the post measurement to measure voltage after the fuses zapped at Trim pad. This test purposely to measure voltage at Reference at the correct condition applied with target value at 2.495V. With circuit configuration from Figure 7, current at 10mA forced at Cathode while Anode pin set grounded. Reference and Cathode pins will set short together. The voltage Vref at 10mA measured from Cathode to Anode.

F. IK_Min and IK_1.35V

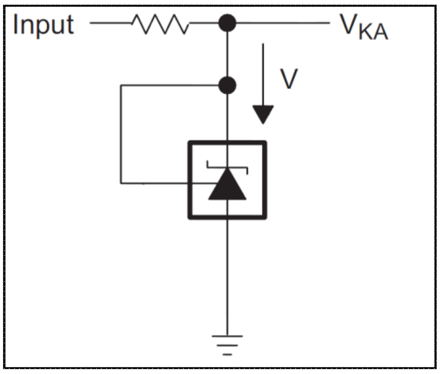


Figure 8. IK_Min and IK_1.35V circuit configuration[1]

Minimum Cathode Current (IK_Min) test is test to measure minimum current flow at Cathode pin. This test will perform when 2.45 V will supply to Cathode pin and Cathode pin and Reference pin. Anode pin will supply 0 V or grounded. The current will measure at Cathode pin and will clamp at 100uA.

Cathode Current at 1.35V (IK_1.35V) test is the test to measure current at Cathode pin when Cathode pin was forced 1.35V. Reference pin and Cathode pin connected together and Anode pin forced 0V or grounded. Cathode Current will measure at Cathode pin.

G. Reg_Max, VKA_10mA and VKA_36V

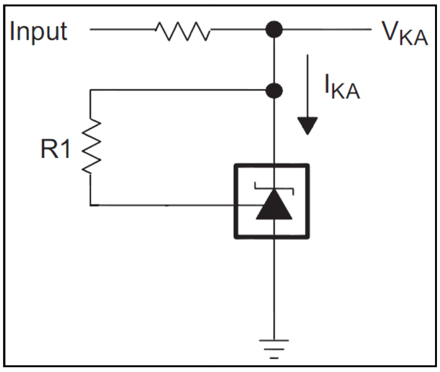


Figure 9. Reg_Max, VKA_10mA and VKA_36V circuit configuration.

Regulation to Maximum (Reg_Max) test is the test to validate maximum rating for TL431A. Current 11.001mA will force at Cathode pin and Reference pin will for force -3.451mA. The Anode will force 0V or remain grounded. 10Kohm resistor will connect between Cathode pin (Pin 1) and Reference pin. The voltage will measure from Cathode pin and Anode pin.

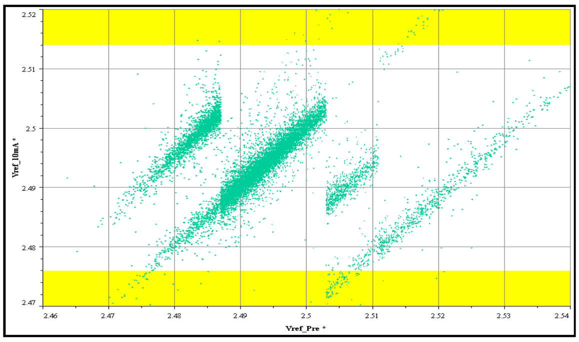
Voltage Cathode to Anode at 36V (VKA_36V) test is the test performs when Cathode pin forced 13.35mA and Reference pin forced -3.35mA. Anode pin forced 0V or remain grounded. 10KOhm connected between Cathode pin and Reference pin. The voltage will measure from Cathode pin and Anode pin.

Voltage Cathode to Anode at 10mA (VKA_10mA) test is the test to measure voltage from Cathode pin to Anode pin. Cathode pin will force 10.75mA and Reference pin will pull out -720uA. 10KOhm connected between Cathode pin and Reference pin. The measurement takes from Cathode pin to Anode pin.

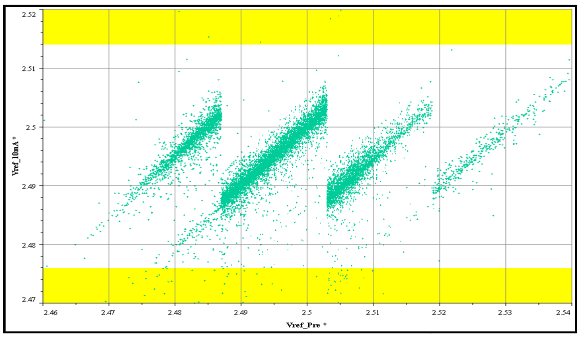
IV. RESULT AND ANALYSIS

A. *Vref 10mA vs Vref Pre*

Figure 10 shows Vref 10mA versus Vref Pre where there are missing pattern at (-0.032V +0.016V) where the pattern mist-trim at after 2.51V (a). The missing Trim pattern fixed when run with new Probe solution (b).



(a)



(b)

Figure 10. (a) Vref 10mA vs Vref Pre Trim pattern missing (b) Vref 10mA vs Vref Pre trim pattern recovered.

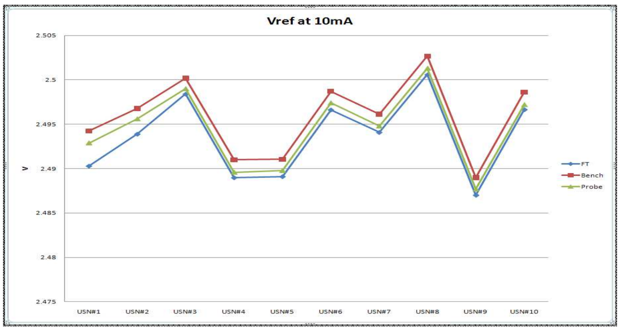
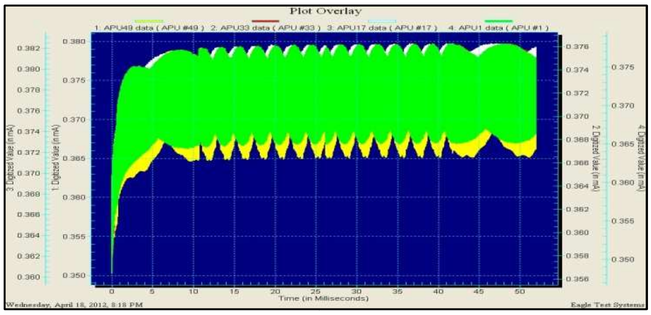


Figure 11. Vref 10mA Correlation Chart

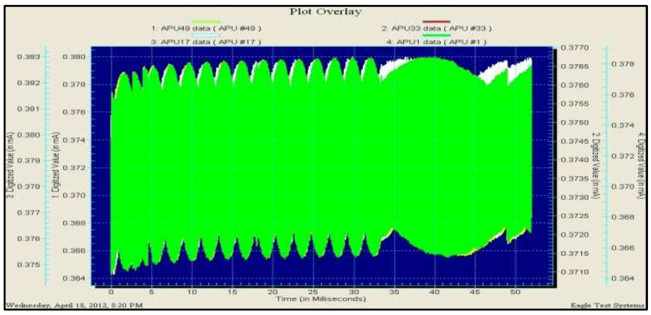
Figure 11 shows the correlation using 10 units of TL431A tested on Probe, Final Test and Bench Lab. The chart shows that the Probe measurements are between Bench Lab and Probe. However some of the units show the Probe measurement more close to Final Test.

B. *IK_Min and IK_1.35V*

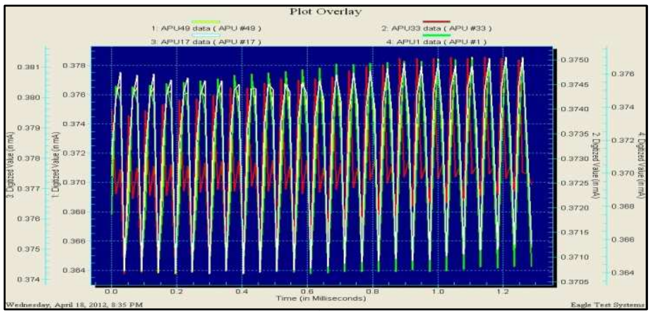
Figure 12 shows measurement of Minimum Cathode Current test (IK_Min) using Probe program with 4096 measurement points (a), Minimum Cathode Current test (IK_Min) with 4096 measurement points when applied 5mS settling time (b) and Minimum Cathode Current test (IK_Min) measurement when applied 5mS settling time and 100 measurement points (c).



(a)



(b)



(c)

Figure 12. (a) IK_min with 4096 measurement point without settling time. (b) IK_Min with 5mS settling time and 4096 measurement points. (c) IK_Min with 5mS settling time and sampled measurement points.

Figure 13 below shows that Minimum Cathode Current (IK_Min) correlation studies between Final Test, Probe and Lab Bench using 10 units of TL431A. The Correlation studies show that Probe measurement closer to Bench Lab measurement.

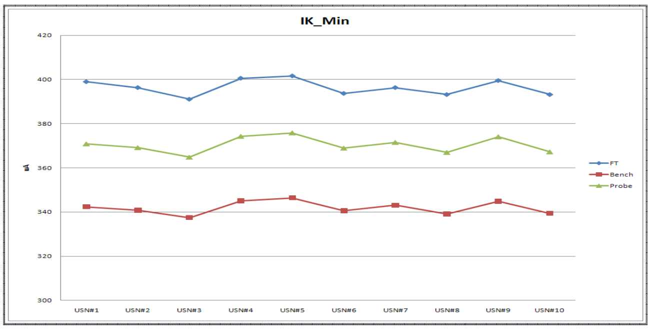
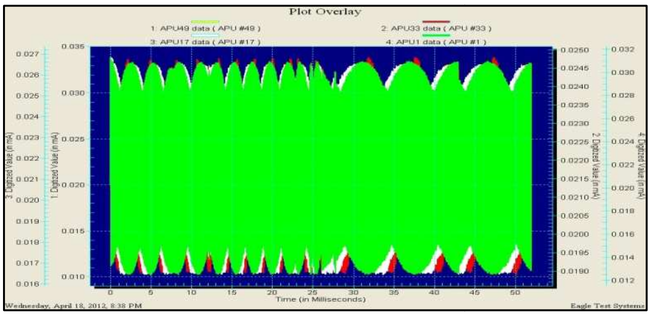
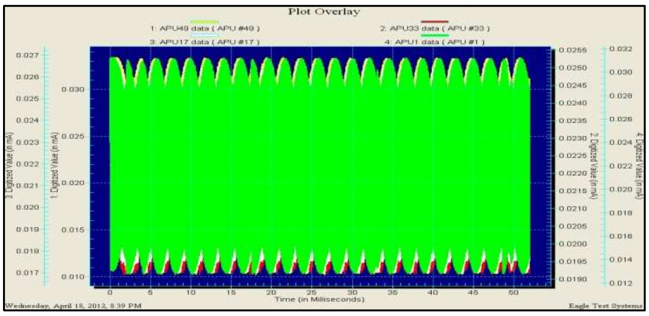


Figure 13. IK_Min Correlation

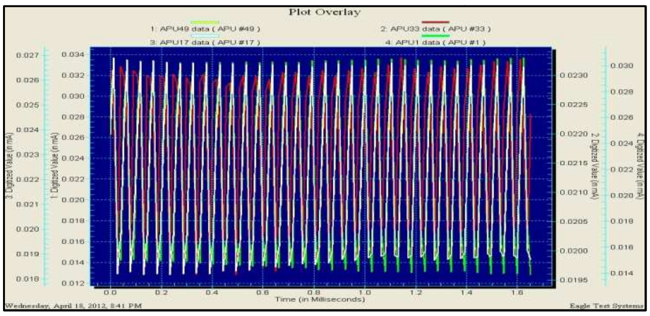
Figure 14 shows Cathode Current at 1.35V test (IK_1.35V) waveform with 4096 measurement point (a). Cathode Current at 1.35V (IK_1.35V) with 4096 measurement point and 5mS settling time (b). Cathode Current at 1.35V test (IK_1.35V) with 5mS settling time and 100 measurement points (c). This test has minimal settling time it is perform after IK_Min test with test condition almost similar.



(a)



(b)



(c)

Figure 14. (a) IK_1.35V with 4096 measurement point without settling time. (b) IK_1.35V with 5mS settling time measurement. (c) IK_1.35V with 5mS settling time and sampled measurement

Figure 15 below shows Cathode Current at 1.35V test (IK_1.35V) correlation study between Final Test, Probe and Lab Bench measurements using 10 units of TL431A. The correlation chart shows that Probe measurements are closer to Bench Lab measurements.

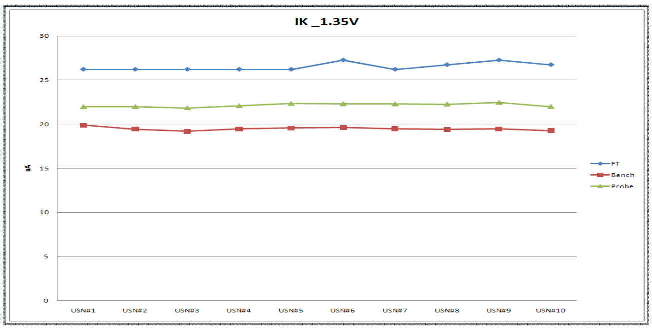
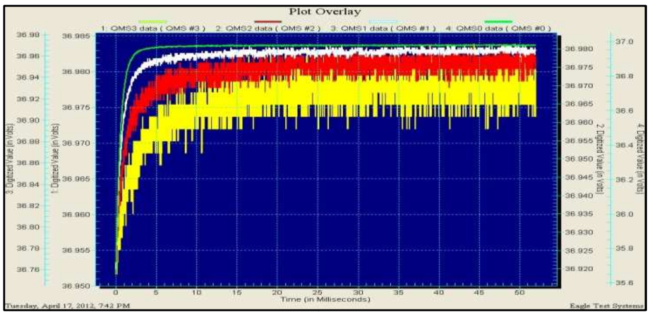


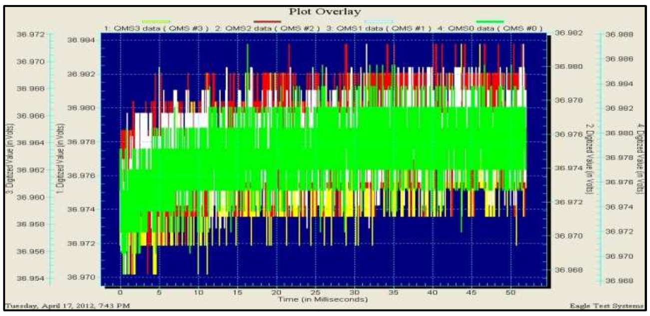
Figure 15. IK_1.35V Correlation

C. *Reg_Max, VKA_36V and VKA_10mA*

Figure 16 below shows Regulation to Maximum test (Reg_Max) waveforms with 4096 measurement points (a). Regulation to Maximum test (Reg_Max) with 5mS settling time and 4096 measurement points (b). Regulation to Maximum test (Reg_Max) waveforms with 5mS settling time and 100 measurement points.



(a)



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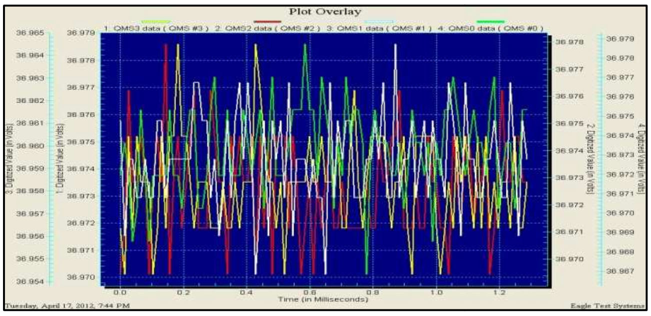


(c)

Figure 16. (a) Reg_Max test with 4096 measurement point without settling time. (b) Reg_Max with 10mS settling time measurement. (c) Reg_Max with 10mS settling time and sampled measurement

Figure 17 below shows Regulation to Maximum (Reg_Max) correlation studies between Final Test, Probe and Lab Bench measurement using 10 units of TL431A. From the correlation chart shows that Probe measurement overlap and correlated with Bench Lab measurement.

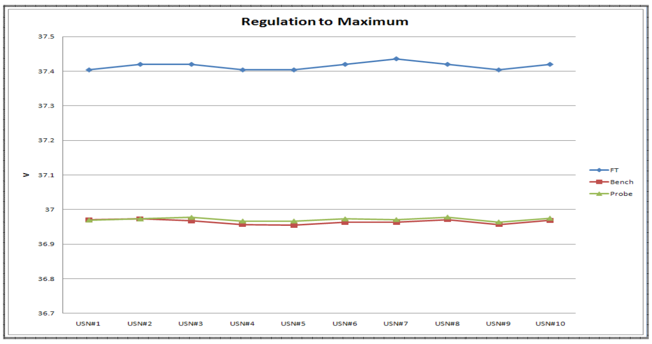
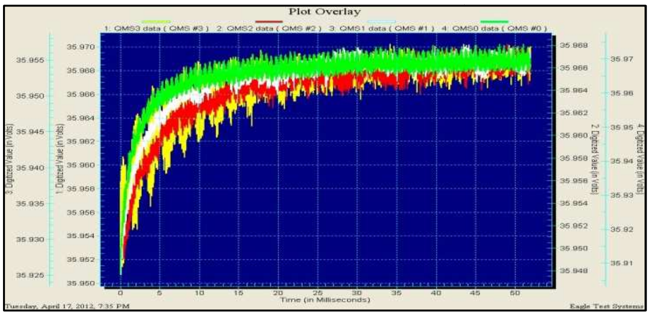
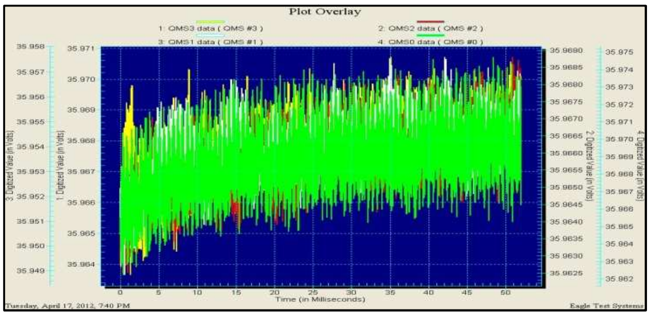


Figure 17. Example of a figure caption. (figure caption)

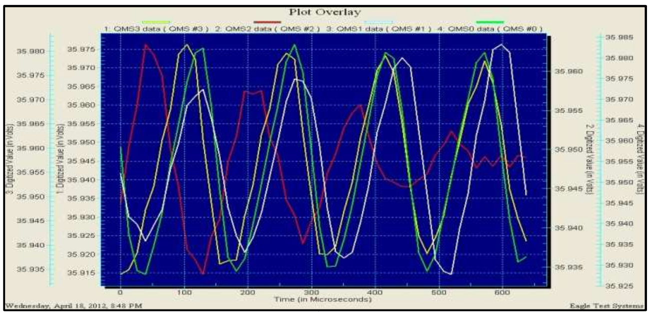
Figure 18 below shows Cathode-Anode at 36V (VKA_36V) waveform with 4096 measurement point and without settling time(a). Cathode-Anode at 36V (VKA_36V) with 15mS settling time measurement (b). Cathode-Anode at 36V test (VKA_36V) waveforms with 15mS settling time and 100 measurement point.



(a)



(b)



(c)

Figure 18. (a) VKA_36V test with with 4096 measurement points without settling time. (b) VKA_36V with 15mS settling time measurement. (c) VKA_36V with 15mS settling time and sampled measurement

Cathode-Anode at 36V (VKA_36V) correlation studies between Final Test, Probe and Lab Bench using 10 units of TL431A. The chart in Figure 19 shows that Probe readed closer and correlated to Bench Lab measurement if compare to Final Test measurement.

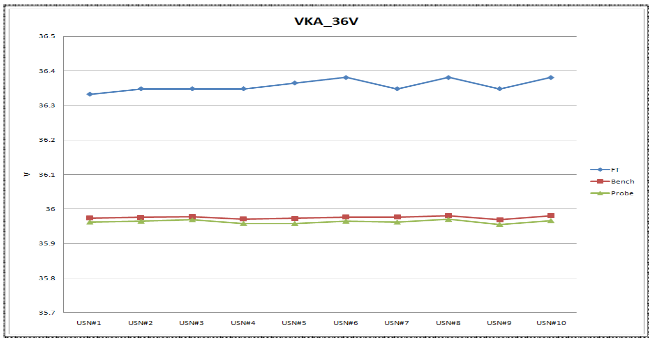
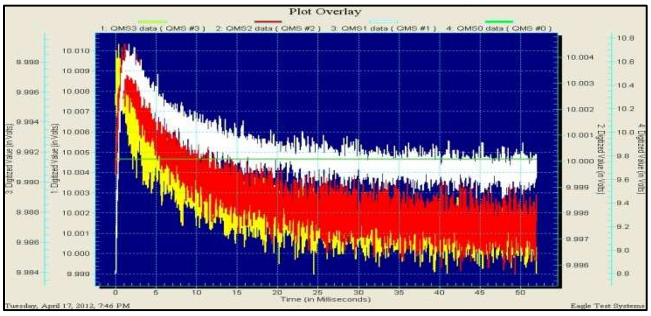
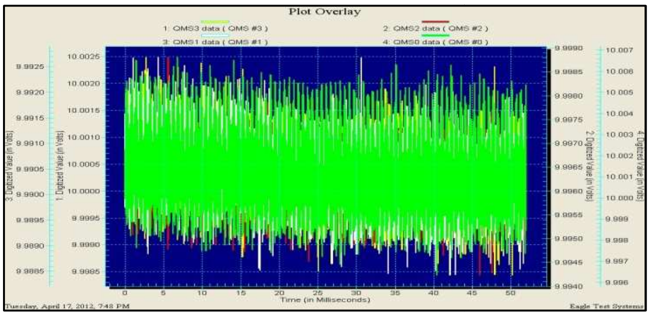


Figure 19. VKA_36V Correlation

Figure 20 shows Voltage Cathode-Anode at 10mA (VKA_10mA) waveforms with full scale measurement (a), Cathode to Anode at 10mA test (VKA_10mA) waveforms with 10mS settling time and 4096 measurement points (b) and Cathode to Anode at 10mA test (VKA_10mA) waveforms with 10mS settling time and 100 measurement points (c).



(a)



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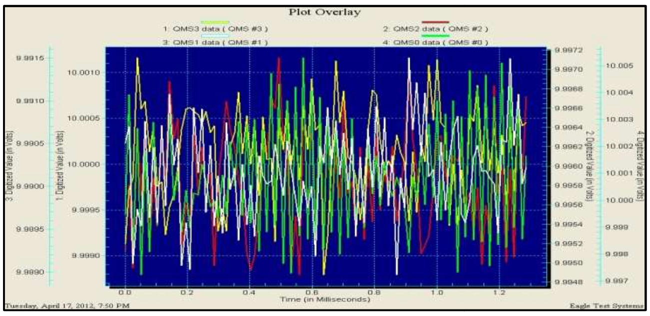


(c)

Figure 20. (a) VKA_10mA test with with 4096 measurement points without settling time, (b) VKA_10mA with 10mS settling time measurement, (c) VKA_10mA with 10mS settling time and sampled measurement.

Figure 21 shows Cathode-Anode at 10mA correlation between Final Test, Probe and Bench Lab using 10 units of TL431A. The correlation observed when the Probe and Bench Lab reading compared.

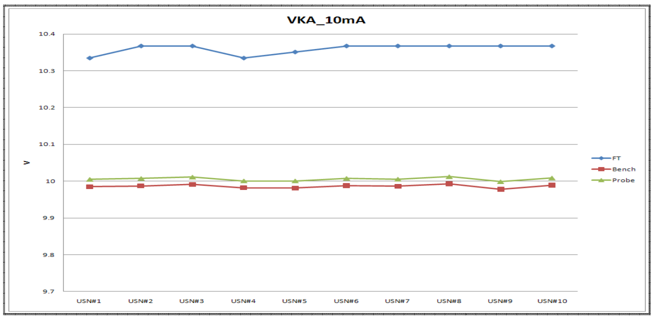
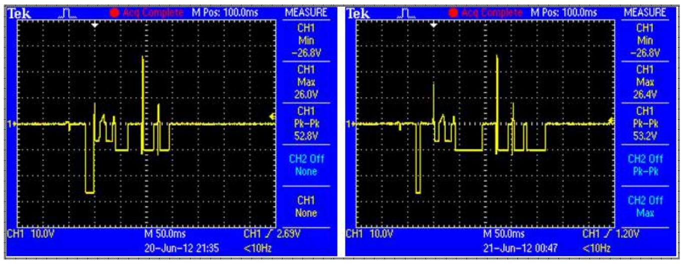


Figure 21. VKA_10mA Correlation

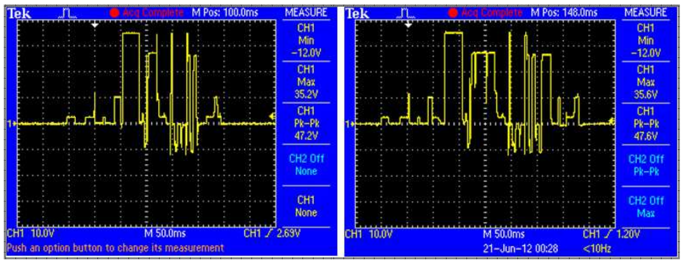
D. *Spike Check*

Spike Check has performed to make sure all resource turn On/Off properly using oscilloscope. All of active pins such Anode, Cathode and Reference pin have to perform spike check to prevent from EOS (Electronic Overstress) during testing. Figure 23, 24 and 25 show the comparison spike check using old Probe solution (a) and new Probe solution (b) need to be done to make sure all min/max voltage within specification.



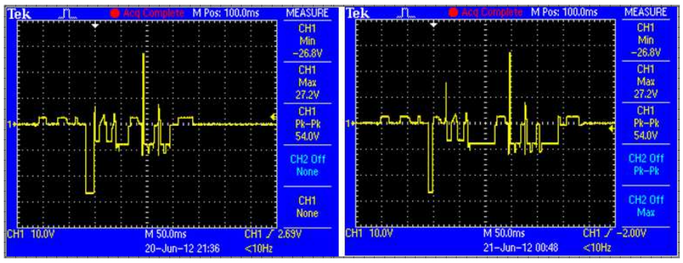
(a) (b)

Figure 22. (a) Anode Pin with original Probe solution. (b) Anode Pin with new Probe solution.



(a) (b)

Figure 23. (a) Cathode Pin with original Probe solution. (b) Cathode pin with new Probe solution.



(a) (b)

Figure 24. (a) Reference Pin with original Probe solution. (b) Reference pin with new Probe solution.

IV. Disscussion and Conclusion

By adding 5 tests at Probe and re-correct for Trimming routine for Vref at 10mA, the yield at Probe expected to drop 1% and Assembly Check for TL431A will expect to produce zero underkill and less than 0.5% overkill during qualification and buy-off. The Assembly Check yield will expect to be more than 99% and the test time is expecting less than 55mS.

In conclusion, to prepare TL431A to move from Final Test to Assembly Check project, test time at Probe significantly increased from 679mS to 788mS. It is a low impact if compare the cost and time that will save after Assembly Check project released.

In future, by releasing Assembly Check for TL431A, this project will be a benchmark for other devices like TLV431A family, TL432A family and LM431 family to moving forward to Assembly Check approach and not just limited to D package.

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