IMPROVISATION OF GABOR FILTER DESIGN USING VERILOG HDL

Thesis presented in partial fulfillment for the award of the Bachelor in Electrical Engineering (Hons) UNIVERSITI TEKNOLOGI MARA

SHAMSUL ANUAR BIN HJ MOHAMED
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
40450 Shah Alam, Malaysia
JULY-NOVEMBER 2009

ACKNOWLEDGEMENT

In the name of god, most beneficent, most merciful, All the praised and thanks to Allah most almighty, lord of the universe and peace be open to His messenger Muhammad, the last of the prophets. We are very gratitude to the Almighty God for the strengths, wisdom, patience, motivation, creativity and ability bestowed upon no to complete this project. This project could not have emerged in its present without the helpful suggestions and combine work made by many people during its preparation. There are many people who have done their part to shape the excellent result.

I, **SHAMUSL ANUAR BIN HJ MOHAMED, (2005387569)** wish to take the opportunity to say thank for the commitment of all people that involve accomplishing this project. My sincerest appreciation must be extended to En. Mohd Faizul Bin Md Idros, the supervisor for the final year project for his commitment and comment. He also explains briefly on the arrangement of the project. Besides, he also gives guidelines, idea and feedback for all steps from start until the end of the project. In addition he also advised me on the characteristic that should be included in my project and about the marking scheme for me to prepare and meet the requirements.

My sincere appreciations to my family for giving me the encouragement and morale support. They also provide me financial support that I need most upon to complete this report. I would like to thank DR Azilah Binti Saparon and En. Karimi Abdul Halim for their helps and advices. I also like to thank my friend Rosshidi Hezrimi for his help and assistance. Thank to fellow faculty members and students. Also, I like to thanks to all members for their comment and helps.

ABSTRACT

This paper presents the improvisation of Gabor Filter design using Verilog HDL. This paper details important enhancement made to the Digital Gabor filter to minimize the sizing problem and the coding style that synthesizable. The intention is to study, analyze, simplify and improvise the design synthesis efficiency and accuracy while maintaining the same functionality. The main characteristic of the proposed approach was to replace the parallel multiplication-accumulation unit (MAC) to a serial multiplication-accumulation unit where the convolution matrix takes place. This significant change helps to reduce the sizing problem without jeopardizing the functionality of the Digital Gabor Filter. The result provides area efficiency architecture for the effective design.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND STUDY

Fingerprint enhancement using Gabor filter is one of highly computational complexity in fingerprint verification process. Gabor filter have a complex valued convolution kernel and a data format with complex values is used. So implementing Gabor filter is very significant in fingerprint verification process. Designing Gabor filter will help enhancing the quality of fingerprint image[1]. In fingerprint recognition, Gabor filter optimally capture both local orientation and frequency information from a fingerprint image. By tuning a Gabor filter to specific frequency and direction, the local frequency and orientation information can be obtained. Thus, they are suited for extracting texture information from images[1].

The Gabor filter is design in an FPGA flow[3]. In FPGA design, speed, size and the power element are the most important elements. In the industry, these three elements act as a guideline in designing a complex circuit. Often designers use a fixed optimization strategy to try and meet the timing. If the speed is chosen to be improved, it will compromise either the size or the power consumption. Theoretically, parallel connection is faster than the series design in FPGA design. However in the industries, sometimes the series connection can provide faster result and can reduce design space consumption. The Gabor filter design Improvisation can help not just reducing the size but might also increase the speed of the filter. Hence, the design optimization is very significant in the designing process[9].

1.2 OBJECTIVE

Objective of this work was to reduce the sizing problem in the Gabor filter design by replacing the parallel design *MAC* to a serial design *MAC*. The convolution matrix took place at the multiplication-accumulation unit (*MAC*) of the digital filter design