DESIGN A SINGLE STAGE FOLDED CASCODE AMPLIFIER WITH GAIN BOOSTER FOR SAMPLE AND HOLD STAGE OF PIPELINED ADC

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ABSTRACT

This thesis presents the full custom design of an operational transconductance amplifier (OTA) for the sample and hold (SHA) stage of a 10-bit 50-MS/s pipelined analog-to-digital converter (ADC) implemented in a MIMOS 0.35μm Complementary Metal Oxide Semiconductor (CMOS) process. Full custom design is implemented in which the design start by determining the specification followed by netlist entry. The simulation is done to verify the specification purpose. The layout of the OTA is constructed after all the parameters are finalized. The last stage of the full custom design is post layout simulation to see the effect of parasitic capacitances to the performance of the design.

The OTA chosen for this design is folded cascode with gain booster. This topology comprises of operational amplifier, biasing circuit and common-mode feedback circuit. This architecture is capable to achieve the high DC gain without sacrificing the output voltage swing as well as the high frequency performances. Based on research, the appropriate sizing (W/L) also contribute to the achievement of the requirement for the pipelined ADC. It is demonstrated through the design analysis and HSPICE simulation that such a structure realizes the best trade-off between power, speed and gain.

The use of gain booster has improved the characteristic of the OTA. The simulation results show that the proposed OTA achieves DC gain of 88.05dB, unity gain bandwidth of 430.03MHz and 84.06 degree of phase margin in the normal condition. Further research also shows the OTA also exhibits a high speed manner, the settling time to 2^{-11} accuracy is 8.26ns. The OTA also achieves 62.13 dB SNR at the sampling rate of 50MHz with the input frequency of 24MHz. Power consumption is 9.68 mW from a single 3V supply. By simulation, it is proved that the OTA is well-suited for the high speed and low power requirement of the pipelined ADC.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Speed and accuracy are two of the most important properties of analog circuits such as switch-capacitor filters, sigma-delta converters, sample and hold amplifier and pipeline ADC; however, designing high performance analog circuits is becoming increasing challenging with persistent trend towards reduced voltage supply. The main bottleneck in the analog circuit design is the operational amplifier. Speed and accuracy are determined by the settling behavior of operational amplifiers. Fast settling requires a high unity-gain frequency and a single-pole settling behavior of the op amp, whereas accurate settling requires a high dc gain. In a low voltage circuit, the realisation of the CMOS operational amplifier that combines high DC gain with high unity gain bandwidth has proven to be a difficult problem. The high-gain requirement has leads to multistage designs with long-channel devices biased at low current levels, whereas the high unity-gain frequency requirement calls for a single-stage design with short channel devices biased at high bias current levels [1].

Cascading is a most useful technique to achieve DC requirement of the amplifier without degrading its high frequency performance. But cascading is not possible in low voltage circuits owing to output voltage swing consideration. The result is a dc gain which is proportional to the square of the intrinsic MOS transistor gain $g_m r_o$. In modern processes with short-channel devices and an effective gate-driving voltage of several hundreds of millivolts, the intrinsic MOS transistor gain $g_m r_o$, is about 20-25 dB, resulting in a dc gain of the cascode version of about 40-50 dB [1]. However, this value is not enough in most analog application.