Simulation of 65nm Vertical Double Gate NMOS Using Silvaco TCAD Tools

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Abstract **- This paper has demonstrated structure design and simulating electrical characteristic of Vertical Double Gate n-channel MOSFET (NMOS) using Silvaco TCAD Tools. Objectives of this study are to design 65nm Vertical NMOS, meet the specification provided by International Technology Roadmap Semiconductor (ITRS) and to study the effect threshold voltage by varying body channel doping and oxide thickness. The investigation of Vertical NMOS characteristic is done through structure design and simulation electrical characteristic using ATLAS tools Silvaco. The extracted values are compared to the ITRS specification. At gate length, L_g=65nm, channel body doping concentration of 1.5×10^{18} cm^{-3} and oxide thickness, T_{ox}=2.2 nm, this design have a drive current of 450µA/µm, low off-state leakage at 18.14nA/µm and subthreshold swing, SubVt of 76mV/decade. From I_d versus V_{gs} characteristic curve, threshold voltage is 0.19V at V_{ds}=0.1V.**

I. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is increasingly used in areas as diverse as mainframe computers and power electronics. The MOSFET's long standing advantages over other types of devices are its mature fabrication technology, its successful scaling characteristics and the combination of complementary the N and P-channel MOSFETs yielding CMOS circuits. MOSFET scaling has been significantly propelled by the rapid advancement of lithographic techniques enabling the definition of smaller features from about 10mm in the 1960's to less than 0.1 micron meter today. During the early years of transistor scaling, Gordon Moore (in 1965) predicted that the number of transistors per square inch on integrated circuits would double every 18 months which has become known as Moore's law [1].

The key technical challenge for continued transistor scaling following Moore's law in the future is scaling the planar MOSFET below a gate length of approximately several tens nanometers (nm). However, there are significant challenges that must be overcome such as lithography, channel doping fluctuation, short channel effects and hot carrier effect. One of the possible alternative to traditional planar MOSFET structure that being explored is Vertical channel Double Gate MOSFET [2].

Since the channel length has no dependence on the critical lithography in vertical MOSFETs, they have received much attention in sub100-nm memory and conventional logic applications [1]. These easily scalable and high-density vertical transistors are well suited for low-voltage and low-power applications.

Objectives of this study includes to design 65nm Vertical NMOS, meet the specification provided by International Technology Roadmap Semiconductor (ITRS) and to study the effect threshold voltage by varying body channel doping and oxide thickness. Fig 1 below show the flow chart progress to achieved the objectives.

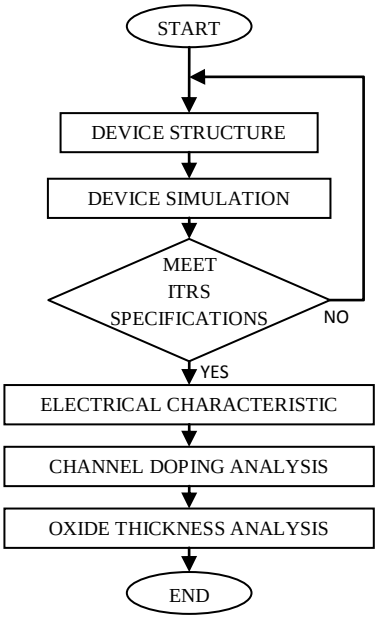

Fig. 1. Flow of study to achieve objectives

Many important semiconductor technologies have been derived from processes invented decades ago. The planar process which utilized on oxide layer formed on a semiconductor surface was originally developed by Jean Horni [3] in 1960. This MOSFET fabrication technology has dramatically control over the last three decades. Starting with a ten-micron gate length PMOS process with an aluminium gate

and a single metallization layer around 1970, the technology has moved to n channel, polysicide gate MOSFET with MOSFET channel length scales down to sub-micron dimensions. Over the past four decades, the channel length of MOS transistors has halved at intervals of approximately every eighteen months, which has led to a virtuous circle of increasing packing density (more complex electronic products), increasing performance (higher clock frequencies) and decreasing costs per unit silicon area [3]. However, to continue this progress, the downscaling of the MOSFET is facing a growing list of technical problems. To continue on this path, research is underway at some research labs to investigate an alternative method of fabricating short-channel MOS transistors. A number of variations in the MOSFET's design have been reported including the FinFET, Tri-Gate and Vertical MOSFET [4].

II. METHODOLOGY

The device structure of Vertical Double Gate NMOS is simulated using ATLAS tools. The process flow of device structure is shown in Fig. 2.

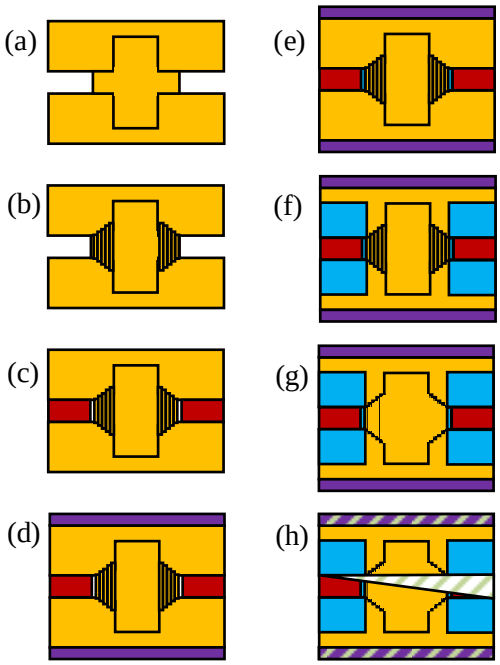

Fig. 2. Device structure of 65nm Vertical Double Gate NMOS using ATLAS

Process of modeling device structures start with mesh definition. In defining mesh, a critical region at gate oxide is designed with finer mesh. Region of source, drain, gates, spacer and gate oxide are defined by coordinates and material used as shown in Fig 3. To make a contact on semiconductor, electrode statement is use for source, drain and gates.

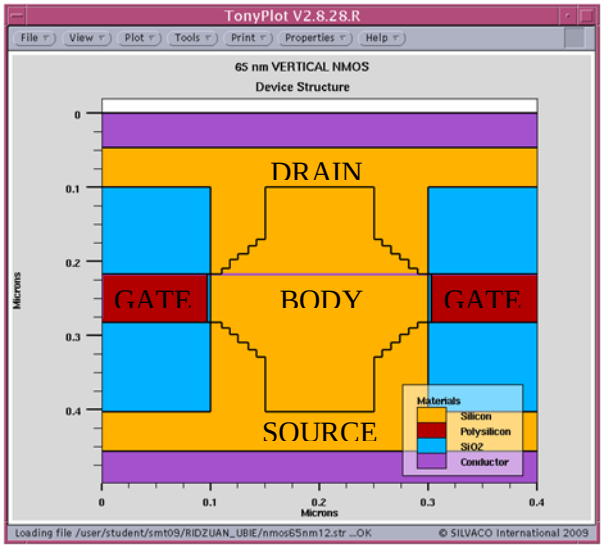

Fig. 3. Region definition in design a structure of 65nm Vertical NMOS.

Electrodes for gates that are associated with the same electrode name are treated as being electrically connected [5] as in Fig. 4.

Device doping is performed using uniform form where drain and source have uniform n-type doping density of 1e20 cm^{-3}. Both left and right gate uniform doping density is 1e21 cm^{-3} n-type. Doping for channel body is applied with p-type at 1.5e18 cm^{-3}. The model used is combination of Lombardi (CVT) and Shockley-Read-Hall (SRH). Model of CVT is good for non-planar devices and SRH is used to fix the minority carrier lifetime [5].

The INTERFACE qf=3e10 statement specifies that all interfaces between semiconductors and insulators have a fixed charge of $3.10^{10} cm^{-2}$. For solution and iteration, fully coupled (Newton) method is used when the system of equations is strongly coupled and has quadratic convergence.

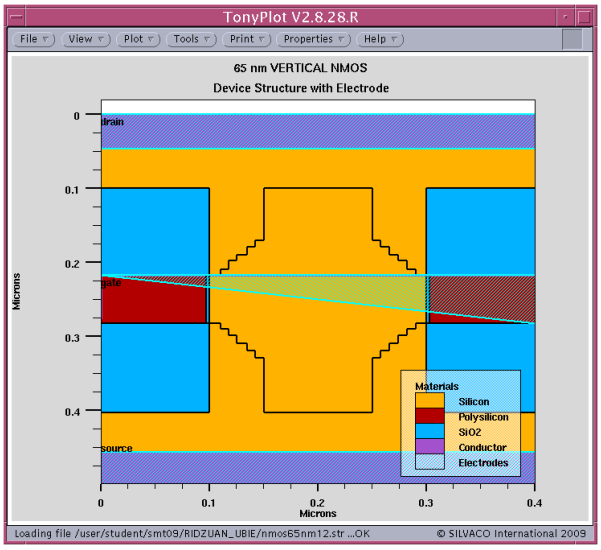

Fig. 4. Electrode of both gates are electrically connected

Graph for I_d versus V_{gs} characteristic is obtained at V_{ds}=0.1V and gate voltage is ramped from 0 V to 1.2V with a step of 0.1V. From the obtained graph, the value of threshold voltage, subthreshold swing, drive current and leakage current is extracted. With a log graph for subthreshold characteristic, the characteristic for subthreshold swing, drive current and leakage current can be seen more clearly. The output characteristic is obtained with applying gate voltage of 0.6, 0.8, 1.0 and 1.2V. Drain voltage is ramped from 0V to 1.2V with a step of 0.1V.

In study on body doping effect analysis, the concentration of body doping, N_a is varied from 1.0e18cm^{-3} to 2.0e18cm^{-3}. For oxide thickness effect, gate oxide thickness is tested at 2.0nm, 2.2nm, and 2.5nm. The analysis is done by observing the effect on Current-Voltage Characteristic, Subthreshold Characteristic and Output Characteristic.

III. Result and Discussion

A. *65nm Vertical NMOS*

By completed the device structure design, ITRS specification is met at structure with length gate, L_g=65nm, oxide thickness, T_{ox}=2.2nm and body doping concentration at N_a=1.5e18cm^{-3}.

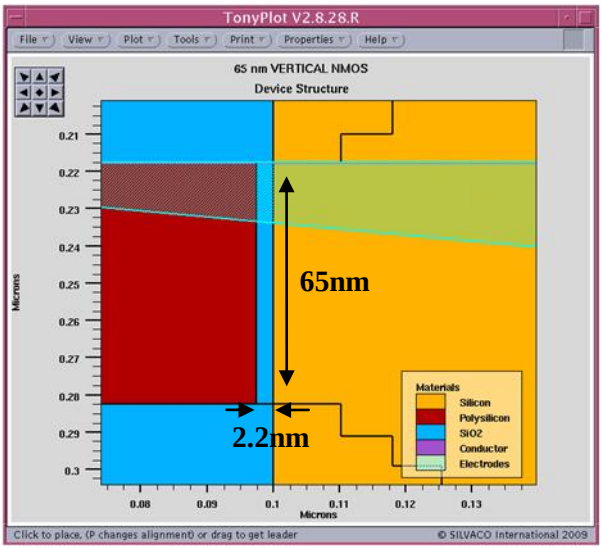

Fig. 5. Vertical channel with length gate, Lg=65nm and oxide thickness, Tox=2.2nm.

As shown in Fig. 6, current-voltage characteristic curve produced at length gate 65nm, oxide thickness 2.2nm and body doping, N_a=1.5e18cm^{-3}. At V_{ds}=0.1V, the threshold voltage extracted for 65nm Vertical NMOS is 0.19V.

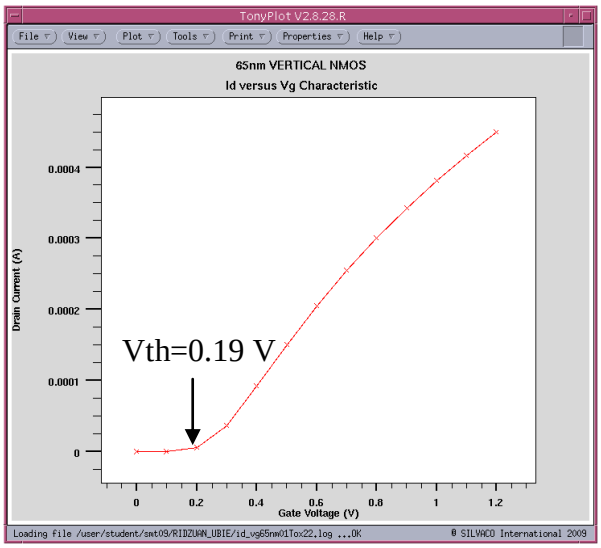

Fig. 6. Id versus Vgs characteristic of 65nm Vertical NMOS at Vds=0.1V

Fig. 7 shows the subthreshold characteristic curve. The graph indicates a drive current at 450 µA/µm, leakage current of 18.138 nA/µm and subthreshold swing, $SubV_t$ of 76 mV/µm.

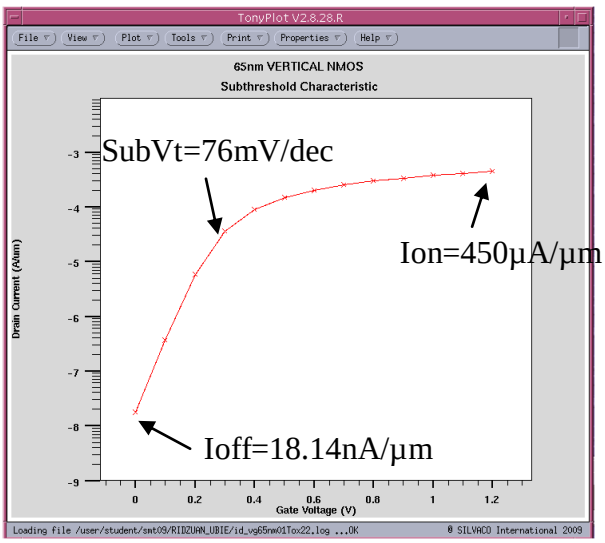

Fig. 7. Subthreshold characteristic of 65nm Vertical NMOS at Vds=0.1V

I_d-V_{ds} curve in Fig. 8 shown the output characteristic of 65nm Vertical NMOS. When no V_{ds} is applied, electrons I the channel do not drift. When V_{ds}>0 is applied, the electrons flow from source to drain. At very small values of V_{ds}, I_d varies linearly with V_{ds}. For V_{ds} at larger values, current levels off and saturates. this can be explain using pinch-off point concept. At $V_{ds} > V_{dsat}$, the pinch-off point of the channel moves toward the source. This will limit current flowing in the channel.

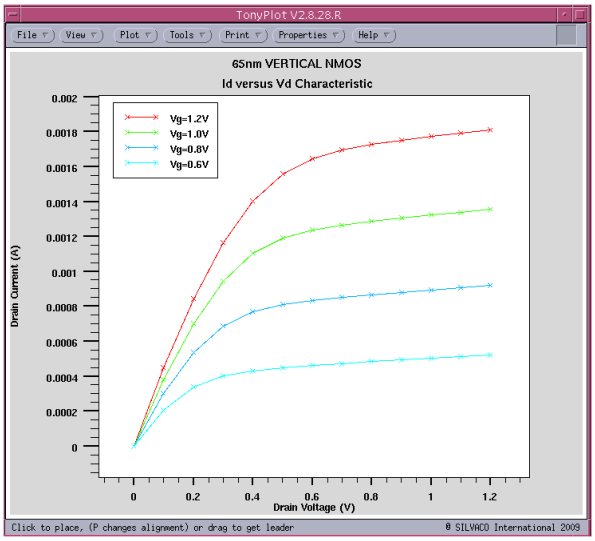

Fig. 8. Id versus Vd characteristics with Vgs at 0.6, 0.8, 1.0 and 1.2V

B. *Doping Effect Analysis*

By simulation, Id versus Vgs characteristic curve is obtained as in Fig. 9. The doping concentration is adjusting at 1.0e18cm^{-3}, 1.5e18cm^{-3} and 2.0e18cm^{-3}. As a result, low threshold voltage values can be achieved by using lower body doping concentration. The threshold voltage extracted is from 0.108V until 0.261V. With the channel doping increasing, the Fermi potential increase, also channel depletion charge increasing, it takes to deplete the whole channel. That's the cause that the threshold voltage goes up with the channel doping increasing [6].

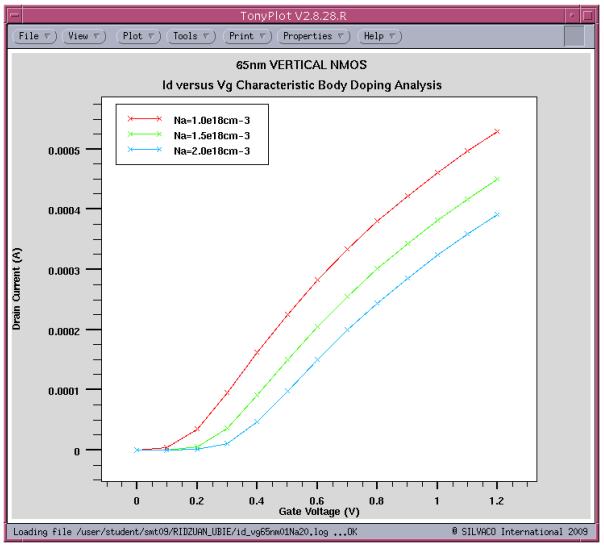

Fig. 9. Id versus Vgs characteristic of 65nm Vertical NMOS at Vds=0.1V with different body channel doping.

Same as threshold voltage in varying body doping, subthreshold swing became higher with a high doping concentration. The range of SubVt is from 73mV/dec to 79mV/dec where doping in 10^{18} cm^{-3} gives a best swing range for NMOS transistor [7]. In investigating the leakage current effect, by increasing body doping concentration, it will lower the leakage current as shown in Fig. 10. These effects arise due to the fact that at higher doping, surface mobility is decreased and better gate electrostatic potential observed within the device which makes the leakage current controllable [8].

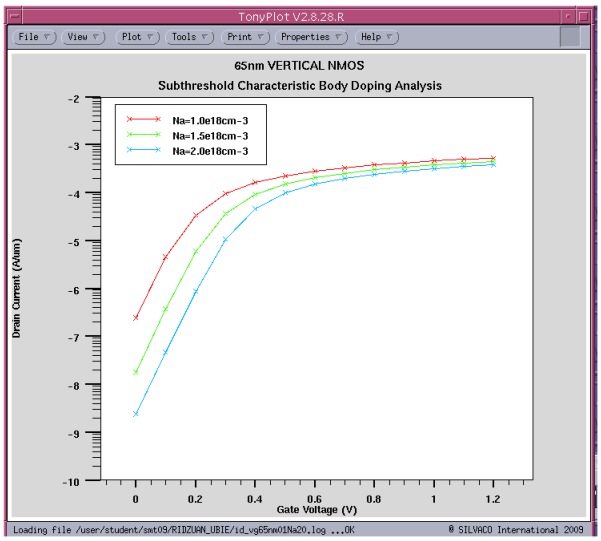

Fig. 10. Subthreshold characteristic of 65nm Vertical NMOS at Vds=0.1V with different body channel doping.

Fig. 11 illustrates the Id-Vds characteristics at the different channel body doping. This graph shows that low channel body doping capable to induce high drive current.

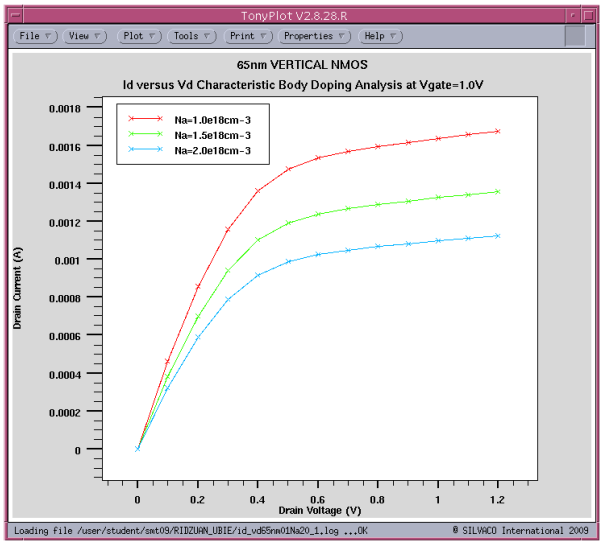

Fig. 11. Id versus Vds characteristic of 65nm Vertical NMOS at Vgs=0.1V with different body channel doping.

C. *Oxide Thickness Effect Analysis*

Oxide thickness is varied at 2.0nm, 2.2nm and 2.5nm, the effect of threshold voltage corresponding to oxide thickness is shown as Fig. 12. From the graph, threshold voltage is

increased when oxide thickness is increased. This means that with the gate oxide thickness increasing, the gate capacitance decreases, and the gate have less control to the channel. In order to invert the channel, the threshold voltage will increase to compensate it [6].

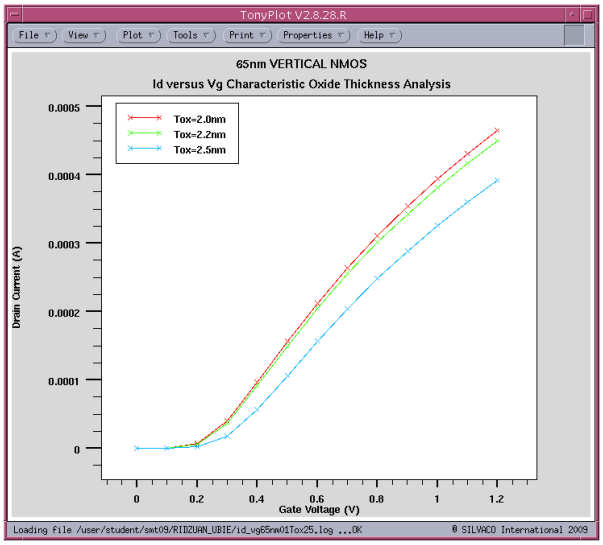

Fig. 12. Id versus Vgs characteristic of 65nm Vertical NMOS at Vds=0.1V with different oxide thickness.

Fig. 13 shows a subthreshold characteristic effect due to different oxide thickness. From the results, subthreshold swing is increased from 76mV/dec to 77mV/dec when varying oxide thickness from 2.0nm to 2.5nm. Leakage current gives a different effect when varying oxide thickness. As thinner the gate oxide is, the higher the leakage current becomes.

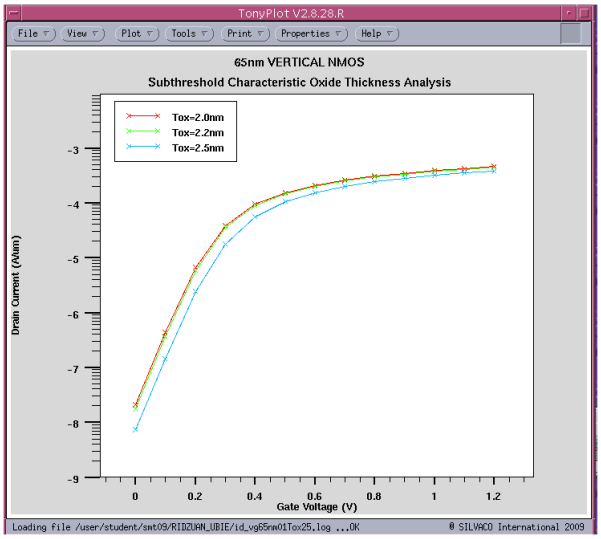

Fig. 13. Subthreshold characteristic of 65nm Vertical NMOS at Vds=0.1V with different body channel doping.

As shown in Fig. 14, the Id-Vds characteristic shows the effect of drive current by varying oxide thickness. From the graph obtained, thin oxide thickness is induces more drive current compare with the thick one.

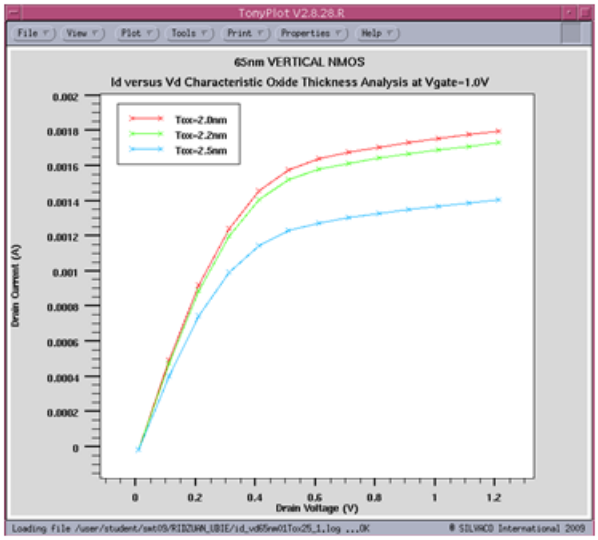

Fig. 14. Id versus Vds characteristic of 65nm Vertical NMOS at Vds=0.1V with different oxide thickness

IV. Conclusion

In conclusion, the structure of 65nm Vertical NMOS is done by using ATLAS TCAD tools. The ITRS specification is met for length gate, L_g=65nm at oxide thickness, T_{ox}=2.2nm and body doping concentration, N_a=1.5e18cm^{-3}. By using Newton as iteration method, electrical characteristics are obtained. The threshold voltage extracted at V_{ds}=0.1V is 0.19V, subthreshold swing, SubV_t of 76mV/decade, drive current at 450µA/µm and low off-state leakage at 18.14nA/µm. From doping effect analysis, it is found that threshold voltage will increase as body doping increase. Leakage current is inversely proportional to body doping concentration. In oxide thickness effect analysis, threshold voltage is low for thin oxide thickness. In term of leakage current, thin oxide thickness will cause a higher leakage current.

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REFERENCES

[1] G. E. Moore, "Progress in Digital Integrated Electronics", in *IEDM Tech. Dig.*, 1975, pp 11-13.

[2] E. Gili, V.D. Kunz, C.H. de Groot, T. Uchino, P. Ashburn, D.C. Donaghy, S. Hall, Y. Wang, P.L.F. Hemmen, "Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance", in *Solid-State Electronics* vol. 48 (2004) pp 511–519.

[3] Hong Xiao, "Introduction to Semiconductor manufacturing Technology", Prentice Hall, 2001.

[4] B. Doyle, R. Arghavani, D. Barlage, S. Datta, S. Doczy, J. Kavalieros, A. Murthy, and R. Chau, "Transistor elements for 30 nm physical gate lengths and beyond," in *Intel Technology Journal*, Volume 6, Issue 6, 2002. pp 42-54.

[5] "DEVICE SIMULATION SOFTWARE", in *ATLAS User's Manual*, Silvaco International, Volume 1, 1998

[6] Xiangli Li, Stephen A. Parke, Bogdan M. Wilamowski, "Threshold Voltage Control for Deep Sub-micrometer Fully Depleted SOI MOSFET", *IEEE Transactions on Electron Devices*, Vol. 51, No. 1, 2004, pp 106-112.

[7] Ima Sulaiman, "*Characterization of Planar and Vertical N-Channel MOSFET in Nanometer Regime"*, 2007

[8] Ismail Saad, Razali Ismail, "Design *and Simulation of 50nm Vertical Double Gate MOSFET (VDGM)*", *IEEE Transactions on Electron Devices*, 2006.

[9] *"International Technology Roadmap for Semiconductor (ITRS)",* Emerging Research Device, http://public.itrs.net, 1999.