ANALYSIS AND DESIGN OF MATCHED-IMPEDANCE WIDE-BAND AMPLIFIERS WITH MULTIPLE FEEDBACK LOOPS USING 0.35µm TSMC COMPLIMENTARY METAL OXIDE SEMICONDUCTOR TECHNOLOGY

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ABSTRACT

The realization of matched impedance wide band amplifiers simulated using **0.35µm CMOS** technology is reported. The technique of multiple feedback loops was used to archive terminal impedance matching and wide bandwidth. The experimental results showed that a small signal gain of **12.7dB** a **3-dB** bandwidth of **1.7GHz** with in band input or output return loss less than **10dB** were obtained. These values agreed well with those predicted from the analytic expressions that have derived for voltage gain, transimpedance gain, bandwidth, and input and output impedances. A general method for the determination of frequency responses of input/output return losses (or S_{11}, S_{22}) from the poles of voltage gain was proposed. The intrinsic overdamped characteristic of this amplifier was proved and emitter capacitive peaking was used to overcome this problem. The tradeoff between the input impedance matching and bandwidth was also found.

1.0 INTRODUCTION

Wide-band amplifiers are used in variety of modern electronic system such as microwave or lightwave communication, instrumentation and wireless system. Among the many versions of wide-band amplifiers, the Kukielka circuit configuration is the one of the popular circuits. Recently, CMOS technology has attracted much attention because it is potentially a low cost process. Multiple feedback loops were used to archive terminal impedance matching and wide bandwidth simultaneously. Capacitive peaking technique was also used to overcome the intrinsic overdamped frequency response of the Kukielka amplifiers and thus enhance the bandwidth. It is well known that the frequency response of voltage gain of a circuit can be determined from the poles and zeros of the voltage-gain transfer function. While knowing the voltage gain is enough in traditional analog circuit design, additional information on the input and output return losses is indispensable in microwave radio frequency (RF) circuit design because input/output impedance matching is important. In addition, the reverse isolation (or reverse voltage gain) of a circuit has to be found to ensure circuit stability. Usually, the conventional analog circuit design starts from the calculation of the voltage-gain transfer function. One of the systematic approaches to derive the denominator of a transfer function efficiently is to write down the simultaneous equations by node or mesh analysis and then find the determinant of the simultaneous equations.

2.0 CIRCUIT DESIGN

The schematic circuit of the Kukielka wide-band amplifier is shown in Figure 1. The input stage consists of a single transistor M1 driving the output stage consisting of a transistor M2 with local shunt (R_{f2}) and series (R_{S2}) feedback. There is also an overall shunt-series feedback loop composed of resistors R_{S2} and R_{f2}. Local shunt feedback around M2 gives low impedance at the collector node of M2 for the output terminal impedance matching. Then, global shunt feedback is applied around this voltage amplifier via R_{f1} to achieve the input matching condition. To verify the proposed theory, a Kukeilka configuration amplifier with multiple feedback loops simulated with a **0.35µm** CMOS process was designed and analyzed.

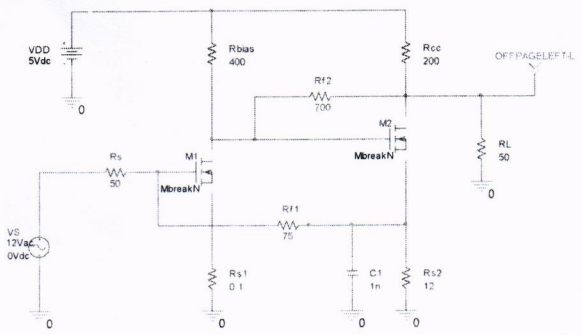

Figure 1: Schematic Diagram

2.1 Circuit Architecture and the Expressions of Its S-Parameters.

The input stage consists of a single NMOS M1, which drives the output stage, composed of an NMOS M2 with local shunt ($\mathbf{R_{f2}}$) and series ($\mathbf{R_{S2}}$) feedback. There is also an overall shunt-series feedback loop composed of resistors ($\mathbf{R_{S2}}$) and ($\mathbf{R_{f1}}$). Capacitance $\mathbf{C_{S2}}$ is added in parallel to $\mathbf{R_{S2}}$ to introduce peaking, which compensates for the overdamped characteristics of this configuration and hence enhances the bandwidth. Clearly, this amplifier can be approximated by a two-pole system with open loop poles ω_{p1} of ω_{p2}. $\mathbf{C_{g1}}$ and $\mathbf{C_{g2}}$ are the total gate capacitances of M1 and M2, R_{sub1} and R_{sub2} are the equivalent substrate resistances of M1 and M2, g_{m1} and g_{m2} are the intrinsic transconductances of M1 and M2, $\mathbf{g_{mb1}}$ and $\mathbf{g_{mb2}}$ are the transconductances of M1 and M2 due to the body effect:

$$G'_{m1} \equiv \frac{g_{m1}}{[1 + (g_{m1} + g_{mb1})R_{S1}]}$$

And

$$G'_{m2} \equiv \frac{g_{m2}}{[1 + (g_{m2} + g_{mb2})R_{S2}]}$$

are the effective transconductances of M1 and M2, and ω_{T1} and ω_{T2} are the cutoff frequencies of M1 and M2. The closed-loop poles of the voltage-gain transfer function and all four S-parameters of the amplifier are given by

$$\omega_{pn1}, \omega_{pn2} = -\frac{1}{2}(\omega_{p1} + \omega_{p2}) \pm \frac{1}{2}\sqrt{(\omega_{p1} + \omega_{p2})^2 - 4(1+T)\omega_{p1}\omega_{p2}}$$

where T is the loop gain, which will be derived later. In the following, first, the expressions of voltage and current gains and input and output impedances at dc frequency will be derived. Then, the expressions of the frequency responses of the amplifier's S-parameters will be described.

2.2 Voltage, Current Gain and Loop Gain

In order to estimate the wideband amplifier performance, the current and voltage gain, the open loop gain and feedback factor need to be calculated. Figure 2 is the equivalent circuit of the circuit shown in Figure 1 excluding the global shunt-series feedback.

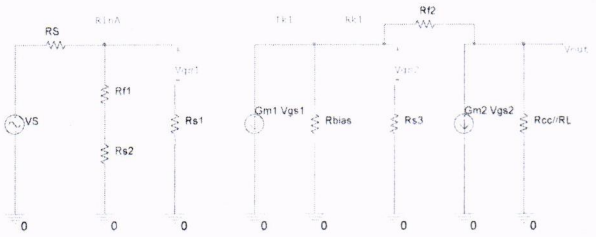

Figure 2: The Small Signal Equivalent Circuit

The voltage gain A_V without global feedback is given by

$$A_V = \frac{V_{out}}{V_{in}} \approx G_{m1}R_{k1}G_{m2}(R_{f2} \parallel R_{CC} \parallel R_L) \approx G_{m1}R_{f2} \quad (assume\ that\ R_{bias} \gg R_{K1})$$

The whole voltage gain of Figure 1 with global shunt-series feedback is given by

$$A_{VSF} = \frac{V_{in}}{V_S} \times \frac{V_{out}}{V_{in}} = \frac{R_{in}}{R_{in} + R_S} \times A_V$$

where $\mathbf{R_{in}}$ is the input resistance of the wideband amplifier with global feedback. If $\mathbf{R_{in}}$ is matched to $\mathbf{R_S}$, then

$$A_{VSF} = \frac{1}{2}A_V \approx \frac{1}{2}G_{m1}R_{f2}$$

The current gain is given by

$$A_I = \frac{I_{out}}{I_{in}} = -(R_{f1} + R_{S2}) \times G_{m1} G_{m2} \times \frac{R_{f2} + (R_{CC} \parallel R_L)}{1 + G_{m2}(R_{CC} \parallel R_L)}$$

Note that the shunt-series feedback theory does not provide the method of deriving the close loop voltage gain, but provides the whole current gain (with feedback) by the modification factor **(1+Aβ)**, so the $\mathbf{A_{VSF}}$ relies on the calculating result of $\mathbf{R_{in}}$. On the other word the loop gain and feedback factor must be obtained. The feedback factor is given by

$$\beta_I = -R_{S2}/(R_{f1} + R_{S2})$$

The total current gain is given by

$$A_{IS} = \frac{I_{in}}{I_S} \times \frac{I_{out}}{I_{in}} = \frac{R_S}{R_S + R_{f1} + R_{S2}} \times A_I$$

Hence the loop gain T of this shunt-series feedback amplifier can be represent as

$$\begin{aligned} T = A_{IS} \times \beta_I &= A_I \frac{R_S}{R_S + R_{f1} + R_{S2}} \beta_1 \\ &= A_I \beta_I \frac{1}{1 + \dfrac{R_{f1} + R_{S2}}{R_S}} \\ &= \frac{A_I \beta_I}{1 + \dfrac{1}{R_S}\left[\dfrac{R_{f1} + R_{S2}}{1 - A_I \beta_I}(1 + A_I \beta_I)\right]} \\ &= \frac{A_I \beta_I}{1 + \dfrac{R_{in}}{R_S}(1 + A_I \beta_I)} \end{aligned}$$

2.3 Position of Poles

The Kukielka topology has two dominant poles. The open loop transfer function of the amplifier (in the absence of global shunt-series feedback) can be written as

$$A_S = \frac{A_0}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$$

According to the open circuit time constant theory, we can write the two approximate open loop poles as

$$\omega_{p1} \approx \frac{g_{m1}}{\dfrac{C_{g2} g_{m1}}{1 - g_{m1} R_{S1}} \times [R_S \parallel (R_{f1} + R_{S2}) + R_{S1}]} \approx \frac{\omega_{T1}}{G_{m1}(R_S + R_{S1})}$$

$$\omega_{p2} \approx \frac{g_{m2}}{\dfrac{C_{g2} g_{m1}}{1 + R_S R_{S1}} \times \left(\dfrac{R_{f2} + (R_{CC} \parallel R_L)}{1 + G_{m2} \times (R_{CC} \parallel R_L)}\right)} \approx \frac{\omega_{T2}}{R_{f2}} \times (R_{CC} \parallel R_L)$$

Thus the close loop transfer function can be written as

$$A_{f(S)} = \frac{A_{(S)}}{1 + A_{(S)} \beta}$$

The close loop poles of any two poles system can be obtained by the following characteristic equations

$$S^2 + S\frac{\omega_0}{Q} + \omega_0^2 = 0$$

$$S = -\frac{1}{2}(\omega_{p1} + \omega_{p2}) \pm \frac{1}{2}\sqrt{(\omega_{p1} + \omega_{p2})^2 - 4(1 + A_0 \beta)\omega_{p1}\omega_{p2}}$$

2.4 Input and Output Resistances

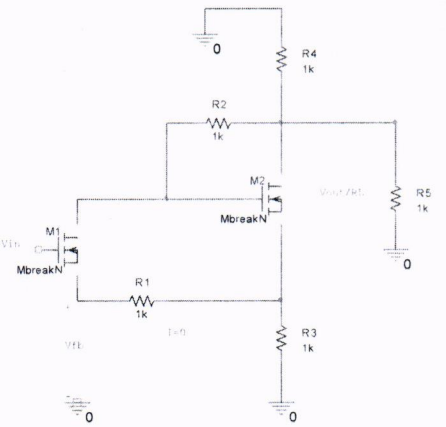

Figure 3: Output Schematic

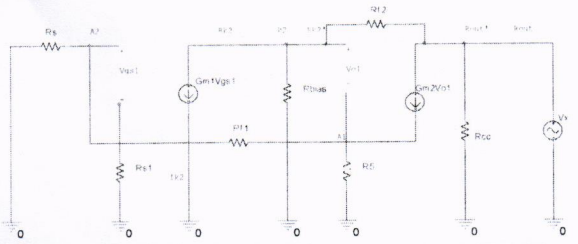

Figure 4: The Equivalent Circuit to Measure Output Resistance

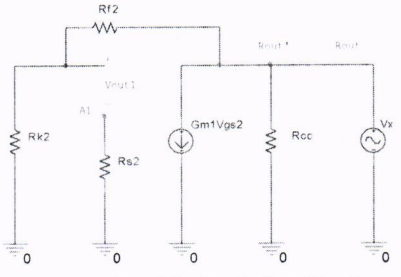

Figure 5: Simplified Equivalent Circuit

By inspecting the input resistance $\mathbf{R_{inA}}$ is $\mathbf{R_{f1} + R_{f2}}$. From the shunt series feedback theory, the input resistance seen to the right hand side of the resistance ($\mathbf{R_S}$) with the global feed back is given by

$$R_{in} = \frac{R_{f1} + R_{S2}}{1 - A_I\beta_I} = \frac{R_{f1} + R_{S2}}{1 + G_{m1} \times G_{m1} \times R_{S2} \times \dfrac{R_{f2} + (R_{CC} \parallel R_L)}{1 + G_{m2}(R_{CC} \parallel R_L)}} \approx \frac{R_{f1} + R_{S2}}{1 + G_{m2} R_{f2} \dfrac{R_{S2}}{R_L}} = \frac{R_{f1} + R_{S2}}{1 + A_V\beta_V}$$

The circuit in Figure 4 can be simplified to the one shown in Figure 5. From this circuit, the impedance $\mathbf{R'_{out}}$ can be shown to be $(R_{f2} + R_{k2} / 1 + G_{m2} R_{k2})$. Therefore, the output impedance under the assumption that $\mathbf{R_{cc}}$ and $\mathbf{R_{bias}}$ are very large and $\mathbf{R_{out}=R_S}$ (equal $\mathbf{50\Omega}$) is given by

$$R_{out} = R'_{out} \parallel R_{cc} = \left(\frac{R_{f2} + R_{k2}}{1 + G_{m2} R_{k2}}\right) \parallel R_{cc} = \frac{A_V R_{S2} + \left(\dfrac{1}{G_{m2}}\right)\left(2 + A_V \dfrac{R_{S2}}{R_L}\right)}{\dfrac{A_V R_{S2}}{R_{f2}} + 2 + A_V \dfrac{R_{S2}}{R_L}}$$

2.5 Frequency Response

Once the two poles and dc or midband gain are known, the frequency response of $\mathbf{S_{21}=2\times}$(voltage gain) can be determined. However, the traditional theory on frequency response does not provide a general way to determine the frequency responses of input and output return losses, i.e., $|S_{11}|$ and $|S_{22}|$. Here, the determination of the frequency responses of input and output return losses from the poles of voltage gain is proposed. $\mathbf{S_{11}}$ and $\mathbf{S_{22}}$ are given by:

$$S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} = \frac{R_{in} + R_S}{R_{in} + R_S} \times \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$$

$$S_{22} = \frac{Z_{out} - R_L}{Z_{out} + R_L} = \frac{R_{out} + R_L}{R_{out} + R_L} \times \frac{\left(1 + \dfrac{s}{\omega_{z3}}\right)\left(1 + \dfrac{s}{\omega_{z4}}\right)}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$$

2.6 Transimpedance Gain

The open loaded transimpedance gain can be calculated by

$$Z_{21} = \frac{A_I}{1 - A_I\beta_I}(R_{f2} \parallel R_{cc}) \frac{1}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)}$$

Where P1' and P2' are the two poles with $\mathbf{R_S}=\infty$ and $\mathbf{R_L}=\infty$. In the 50Ω loaded system, the transimpedance gain can be shown to be

$$Z_T = \frac{S_{21}}{1 - S_{11}} \times 50$$

2.7 Design Equation

Under the assumptions that $G_{m1} R_L \gg 1$, $R_{s1} \ll R_s$, and $\omega_{T1} = \omega_{T2}$. The condition $\omega_{p1} = \omega_{p2}$ can be reduced to

$$R_{f2} = G_{m1} R_S (R_{cc} \parallel R_L)$$

than

$$R_{f2} = \sqrt{2 A_{VSF} R_S (R_L \parallel R_{cc})}$$

$$R_{S1} = \frac{R_S \times (R_{cc} \parallel R_L)}{R_{f2}} - \frac{1}{g_{m1}}$$

In which g_{m1} is dependent on the size of bias of M1, which is decided according to the acceptable power consumption and noise figure. According to equation before, $\mathbf{R_{fl}}$ is given by

$$R_{f1} \approx (1 + A_I\beta_I)R_S = (1 + A_V\beta_V)R_S$$

The β_V (or $\mathbf{R_{S2}}$) must be determined in order to find the value of $\mathbf{R_{fl}}$ is desirable in the requirement of a low noise figure, which means that a large $A_I\beta_I$ or $A_V\beta_V$ is favored. $\mathbf{R_{S2}}$ can be decided by the output matching condition. By setting $\mathbf{R_{out}}$ to $\mathbf{R_L}$, the following equation is obtained.

$$R_{out} = \frac{A_V\beta_V R_L + \left(\frac{1}{G_{m2}}\right)(2 + A_V\beta_V)}{\frac{A_V\beta_V R_L}{R_{f2}} + (2 + A_V\beta_V)}$$

Based on the equation above, the value of $\mathbf{R_{S2}}$, in general, can be obtained.

$$R_{S2} = \frac{R_L\left(\frac{A_V\beta_V R_L}{R_{f2}} + 2\right)}{2 + A_V\beta_V} - \frac{1}{g_{m2}}$$

$\mathbf{R_{cc}}$ is determined by the dc bias point, which should be around **1/3** of the supply voltage. The bandwidth can be estimated to be $\mathbf{1.414\omega_{p1}}$ or $\mathbf{1.414\omega_{p2}}$, assuming maximum flat condition.

3.0 METHODOLOGY

The CMOS circuit design process consists of defining circuit inputs and outputs, hand calculations, circuit simulations, layout of the circuit, simulations, and reevaluation of the circuit inputs and outputs.

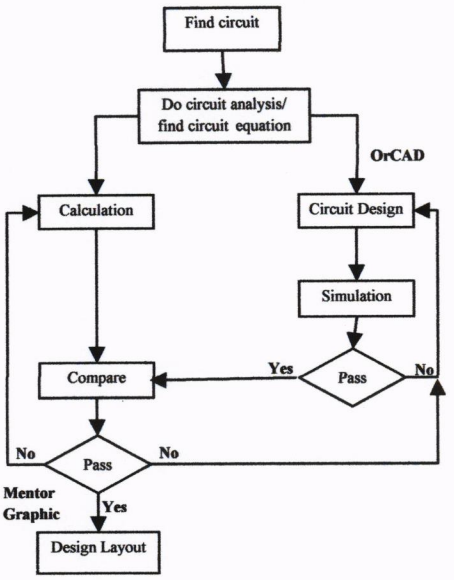

Figure 6: Work Flow

4.0 RESULTS AND DISCUSSION

The resistors have the following values: R_{bias} = 650Ω, R_{cc} = 150Ω, R_{fl} = 80Ω, Rf2 = 650Ω, $R_{s1} \approx 0\Omega$, $R_{s2} \approx 12\ \Omega$, C_{g1} = 2.5.5 fF, C_{g2} = 162.4 fF. Input Reflection Ratio, S_{21}= 17.7 *dB*, Input Return Loss, S_{11} = -8.9 *dB* Isolation, S12 = -25.3 *dB*, Output Return Loss, S22 = -6 *dB*, Bandwidth = 1.7 *GHz*, Power = 1.5 *mW*.

This circuit was simulated using 0.35µm technology and the size of M1 and M2 are both 0.35µm x 20µm. The total power dissipation is only 1.16 mW.

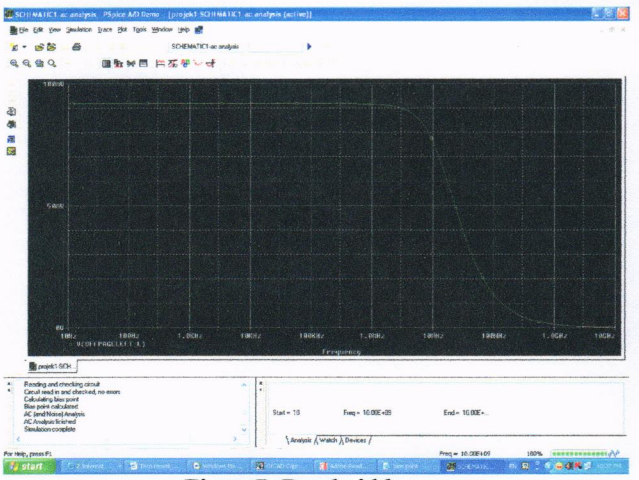

Figure7: Bandwidth

A general method for the determination of the frequency responses of input and output return losses from the poles of voltage gain was also presented. The simulation results showed that small signal gain of 10.5dB and a 3-dB bandwidth of 1.7GHz with in band input and output return losses less than –7dB were obtained. The calculated values of small signal gain, bandwidth, input/output resistance, and frequency responses agreed well with those from experimental results. Thus the verification of proposed equations was demonstrated.

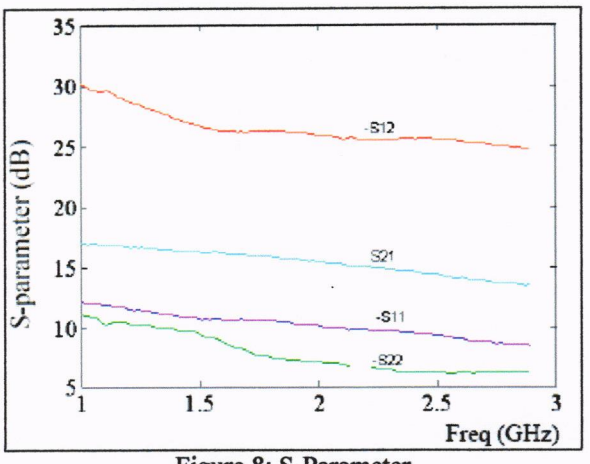

Figure 8: S-Parameter

The result shows:
Input Reflection Ratio, S_{21}=18.3 *dB*
Input Return Loss, S_{11}= -8 *dB*
Isolation, S_{12}= -23.5 *dB*
Output Return Loss, S_{22}= -6.7 *dB*
Bandwidth= 2.1 *GHz*

The layout of the finished circuit is shown in Figure 9.

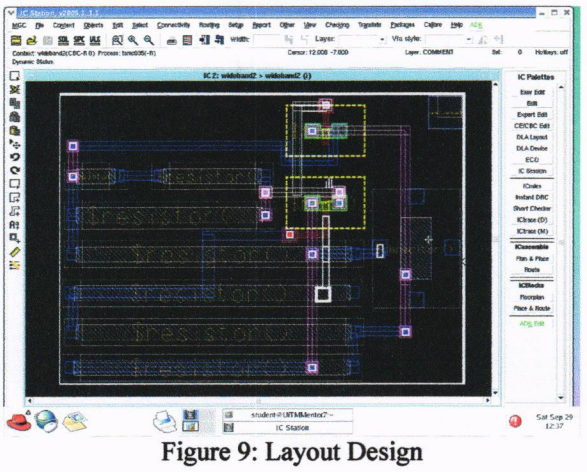
Figure 9: Layout Design

	Predicted	Calculation	Simulation
Input Reflection Ratio,S21	18.7 *dB*	17.7 *dB*	18.3 *dB*
Input Return Loss,S11	-8 *dB*	-8.9 *dB*	-8 *dB*
Isolation,S12	25 *dB*	-25.3 *dB*	-23.5 *dB*
Output Return Loss,S22	-7 *dB*	-6 *dB*	-6.7 *dB*
Bandwidth	2.0 *GHz*	1.7 *GHz*	2.1 *GHz*
Power	1.5 *mW*	1.5 *mW*	1.16 *mW*

Table 1: Result Comparison

The measured S_{21} exhibited a flat response with a 3-dB bandwidth of 1.7*GHz* and in band return loss $|S_{11}|$ and $|S_{22}|$ were smaller than –7*dB*. The predicted S_{21} at low frequency by the method we proposed is 18.7*dB*, in good agreement with the simulated S_{21} 18.3*dB*. The measured result is about 0.5 *dB* lower than the prediction, which is possibly due to substrate loss that is not modeled. The simulated $|S_{11}|$ and $|S_{22}|$ also agreed well with the measured values as shown in Figure 7, respectively. Also shown are the calculated values of frequency responses from our theory for S_{21}, S_{11}, S_{22}, Z_{21}, and Z_T. Reasonably good agreement with the experimental results is found. The predicted bandwidth is 2.0*GHz*, which is comparable to the simulated result of 2.1*GHz* but higher than the measured result of 1.7 *GHz*. The discrepancy may be due the parasitic substrate capacitances.

5.0 CONCLUSION

1 The realization of matched impedance wide band amplifier designed by 0.35 **µm TSMC** complementary metal oxide semiconductor technology is reported. The technique of multiple feedback loops was used in the amplifier for terminal impedance matching and wideband simultaneously. The simulated result small signal gain, bandwidth, input and output resistance, and frequency response

of s-parameters agreed well with the predicted and measured results. The methodology for the calculation of S-parameters from the denominator or poles of the voltage-gain transfer function is presented. First, S_{11} and S_{22} can be obtained with R_S in the expression of the denominator or poles of the voltage-gain transfer function Second, the input impedance can be obtained by isolating R_S from the other terms in the expression of the denominator while the output impedance can be obtained by isolating R_L from the other terms. Third, S_{11} can be determined by finding the zeros and dc (or mid-band) gain of the "reverse circuit." The theory has been applied to three circuits and the results of S-parameters and input/output impedance derived from present method are the same as those obtained from direct calculations. In addition, a wideband amplifier with multiple feedback loops simulated using **0.35µm CMOS** technology was used to verify the proposed theory. The simulated results are consistent with those predicted from the analytic expressions of S–parameters determined from the poles of the voltage-gain transfer function. These results show that our proposed method is very applicable to amplifier for example RF IC design.

6.0 FUTURE IMPROVEMENTS

The wide band amplifier can be improving on their electrical characteristic. There are also can be improve on the frequency response, gain and reduce the noise effect. The improvement can be implementing by using the latest technology such as the shortest length of technology of FET. Another way is by using of different material such as GaAs replace the silicon oxide.

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