A Study of 4-bit Pipeline Flash Analog to Digital Converter Using 0.18um CMOS Technology

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Abstract - **In this paper, effect of pipelining in 4 bit flash ADC is investigated. By adding latch staging in decoder circuit, it can improve the accuracy and meta-stability error of output signal of the flash ADC. Two stages comparator that has high speed, high level accuracy and non-compensation is used. The output of comparator is generated in form of thermometer code will be converted to binary code in decoder stage. Effect of load capacitor to the comparator stage also will be analyzed. Small value of capacitor will lead to short time transition of state, mostly because of charge and discharge of the capacitor. LTSPICE is used to design the circuit and simulate the flash ADC circuit to produce waveform of flash ADC. Based on the waveform generated, the meta-stability error of the output waveform will be analyzed. The proposed pipeline flash ADC will produce less meta-stability error than conventional pipeline flash ADC. The binary code of the conversion of input analog signal also will be analyze and tabulate.**

Keywords **- ADC, flash ADC, pipeline, comparator, decoder, meta-stability error, capacitor, latch, circuit, binary code**

I. INTRODUCTION

Nowadays, the growth of analog and digital circuitry was very rapidly increasing[1]. Flash ADC are the key in many applications including the read channels of magnetic and optical data storage systems, high data rate digital communications, high speed instruments, wideband radar and optical communications. Flash ADC is suitable for applications that requiring very large bandwidths[2]. However, these converters consume large power consumption, have relatively low resolution and can be quite expensive. Function of the flash ADC is to convert analog input voltage signal to binary code output signal. By using flash ADC, the conversion of the analog signal is fastest compared to other converters[3].

Comparator circuit is very important and also the key in circuit of flash ADC architecture and strongly influences the performance of flash ADC. High degree of the comparator accuracy is essential for good ADC performance. The comparator is a device which compares two currents or voltages and produces the digital output based on the comparison. Many applications such as analog to digital converter, memory sensing circuits, and chip transceivers are widely use the comparator. In past years, most researches try to come out with comparator that has low power consumption, simple thermal management and high efficiency. The growth of portable devices has made the power consumption issues crucial for the researcher in order to create a comparator that uses less power consumption.

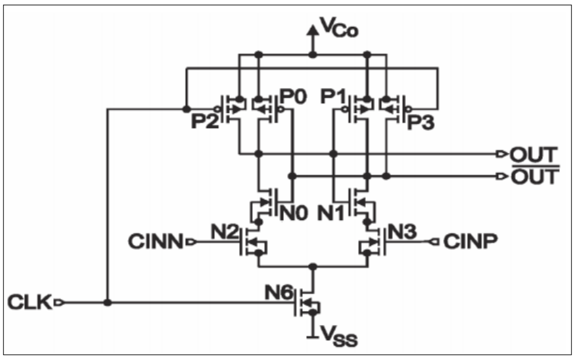

Fig.1: Conventional comparator circuit

Figure 1 is the circuit of conventional flash ADC[4]. This comparator circuit is latch-type comparator with the high impedance input, rail to rail output swing and no static power consumption. This circuit has advantages in reducing noise and the mismatch error. However, it suffers of high sufficient power supply, which is caused by many stacked transistors in circuit design. Many researchers try to come with a design of comparator that has less power consumption, high accuracy and stability, and also the size is small. The two stage comparator is the suitable and fastest in converting analog signal to output signal. But is also consumes high power in order to function in high resolution and accuracy level.

Meta-stability in electronics is the ability of a digital circuit to obtain metastable state for a given time or input[5][6]. In metastable state, there are a state of the circuit may be unable to settle into a stable '0' or '1' logic level within the time required for proper circuit operation. As the result, meta-stability error will occur and affect the accuracy of the flash ADC circuit. By adding latch at comparator stage and converting thermometer code to gray code, it can reduce the meta-stability error[7].

In this paper, 4-bit pipeline flash ADC is design that has less meta-stability error. Adding latch staging can improve the accuracy and reduce meta-stability error of the flash ADC circuit. By reducing the meta-stability error, the circuit is able to settle into a stable '0' or '1' logic level for a given time. Implementation in high frequency applications needs high level of accuracy and stability of waveform of output. The result should show that this design can be use in high frequency applications base on the accuracy level and the stability of the output voltage.

II. METHODOLOGY

Flash ADC is made by cascading high-speed comparators. Figure 2 show the conventional flash ADC block diagram[8]. For an N-bit converter, the circuit needs $\mathbf{2^N - 1}$ number of comparator. By increasing the number of bits of the converter, the accuracy level and resolution also can be increase. For every increase in digital bits, number of comparator gets doubles. A resistive-divider known as resistor ladder with $\mathbf{2^N}$ number of resistors generates $\mathbf{2^N - 1}$ of the references voltages[9]. The function of comparator is to compare the analog input voltage and the reference voltage that generated by resistor ladder. Each comparator produces a 1 when its analog input voltage is higher than the reference voltages applied to it. Otherwise, the comparator output is 0.

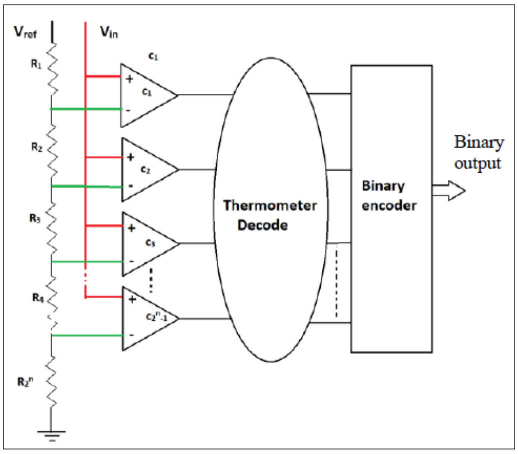

Fig.2: Conventional flash ADC block diagram

The output of comparator stage is in form of code, known as thermometer code[5][10]. This name used because the design is similar to mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above the temperature. First, the thermometer code is converted to gray code. This is due to detect and corrected the bubble error in thermometer code[11]. Gray code then converted to 4-bit binary code using XOR gate.

Figure 3 is the architecture of the proposed pipeline flash ADC. The different between conventional and the proposed pipeline flash ADC is the addition of latch staging at the comparator stage and decoder stage. This will be explained later in the section B, decoder circuit. The input of this architecture is analog input voltage and reference voltage. $Vref$ is connected to resistor ladder to produce 15 different $Vref$. The 15 different $Vref$ is compare with analog input voltage, Vin by 15 different comparator stages. In comparator stage, comparator is connected to first latch stage to produce thermometer code. Thermometer code then converted to gray code. Gray code must go through the second latch staging before converted to binary code. The binary code also needs to go through the third latch staging before become the output of the flash ADC.

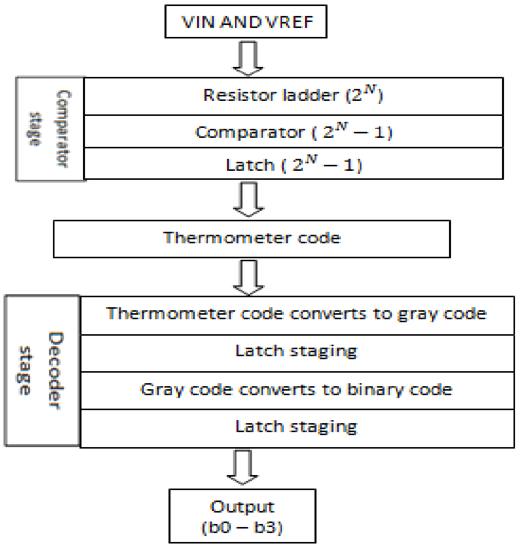

Fig.3: Architecture of proposed 4 bits flash ADC

A. *Design of Comparator Stage*

Figure 4 shows the circuit of the comparator. Two stages comparator is used in this research. The comparator is the combination of basic differential amplifier stage and the inverter. This comparator has high gain and good signal swing compare to differential amplifier base comparator. The inverter will give the full swing output. Because of two stages comparator is an op-amp with non-compensation, it can be use in open loop mode.

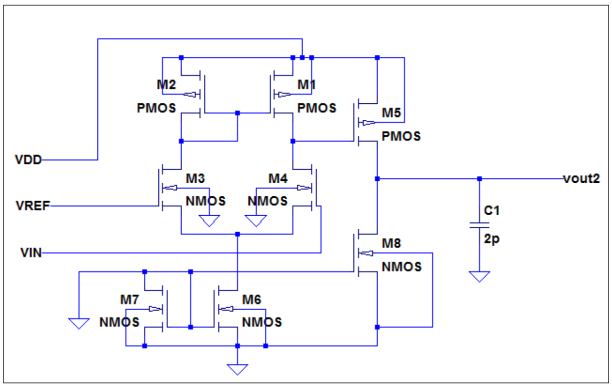

Fig.4: two stage comparator

The comparator output is connected to load capacitance to reduce the noise at input voltage and remove the ripples from power supplies. This load capacitance can store energy or electrical charges. Moreover, capacitor also can be used to resist any change of voltage across due to capability to store a charge and gives the output voltages waveform smoother. Increasing the value of load capacitor will affect the rise time and fall time of output waveform. This is due to charging and discharge process of the load capacitor. This effect was analyzed in section III, result and discussion.

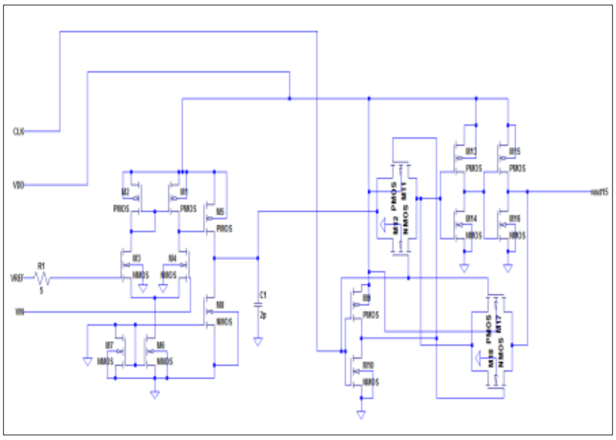

Fig.5: Circuit of comparator and latch

The first staging of latch is at comparator stage. Every comparator is connected with latch to reduce meta-stability error in comparator output signal as in Figure 5. By increasing the time of regeneration of signal, the latch will stabilizing the signal and reducing the meta-stability error in comparator stage. The low state of output signal will approximately equal to 0V and the high state is equal to VDD.

B. *Design of Decoder Stage*

To design the decoder, a gate-based decoder is preferred compared to ROM-based decoder. The schematic of conventional gate based decoder is shown in figure 6. Based on the Figure 6, it consists of AND, NAND, NOT, XOR gates and latch. In first stage, the thermometer code is converted to gray code. By this conversion, any bubble error from thermometer code will be detected. The correction of the bubble errors in thermometer code is done by converting thermometer code to gray code. Second stage is to convert gray code to digital binary code using XOR gates.

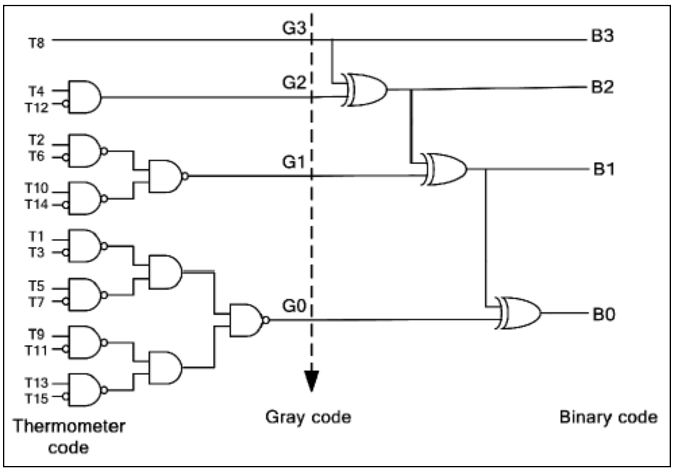

Fig.6: Schematic of pipeline decoder

For pipeline flash ADC decoder shown in Figure 7, latch staging is implemented at the gray code and binary code. Gray code need to go through the latch staging before converted to binary code and binary code need to go through latch staging to produce stable, accurate binary code. By adding the latch, meta-stability error of each code can be reduce due to clock transition of the latch. Adding the latch also can reduce the critical data path delay of this decoder. This can make the decoder can operates faster than conventional flash ADC decoder.

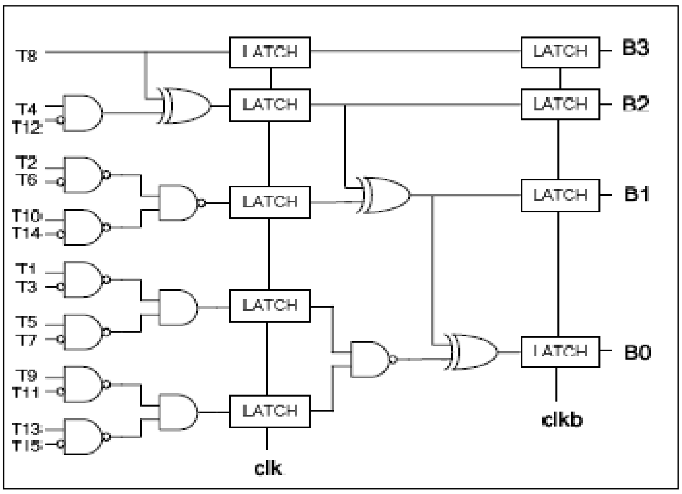

Fig.7: Schematic of pipeline decoder

Figure 8 is the proposed decoder pipeline circuit designed by using LTSPICE software. The input of decoder is the thermometer code that generated by comparator stage and the output is 4-bit digital binary code. It has two stage of latch, at the gray code and binary code. Thermometer code is converted to gray code by using NAND and AND gate. The gray code is converted to binary code by using XOR gate.

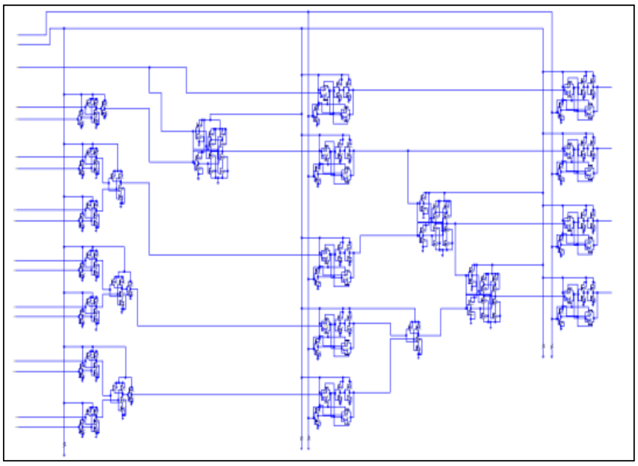

Fig.8: Circuit of pipeline decoder circuit

C. Schematic of Proposed Pipeline ADC

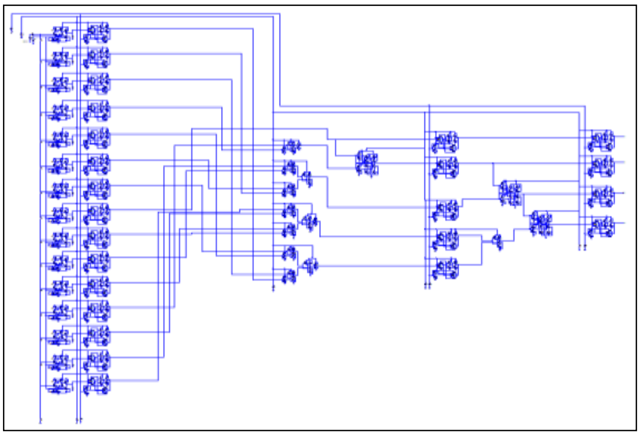

Fig.9: circuit of pipeline flash ADC

By combining comparator circuit and pipeline decoder circuit, the proposed 4-bit pipeline flash ADC is established. This circuit will convert analog input voltage to 4-bit binary code. By using LTSPICE software, the circuit was designed based on the parameter of 0.18um CMOS technology. Figure 9 show the proposed 4-bit pipeline flash ADC. It has 15 stage of comparator. The input of comparator is reference voltage and analog input voltage. It has 3 stage of latch, one at the comparator stage and other two is at decoder stage. This latch stages is functions to stabilize and reduce the meta-stability at the thermometer code, gray code and binary code.

III. RESULT AND DISCUSSION

To simulate the pipeline flash ADC circuit, some specification needs to be considered. We are using 0.18um CMOS technology. Supply voltage, Vdd is equal to 1.8V for the CMOS transistor to operate in saturation region. Reference voltage is 1.8V. Analog input voltage must be in sine waveform, so the input analog voltage is set to a sine wave waveform. Input analog voltage has frequency of 100MHz. the DC offset voltage is 0V and the amplitude of the sine wave is 1.8V. For the resistor ladder, we are using 5ohm resistor to produce difference reference voltage in every comparator.

For transient analysis simulation, the clock is set as pulse waveform. the initial voltage is 0V, on voltage is 1.8V, time delay is 0.5second, rise time and fall time is 0.1second, on time is 0.25second, time of period is 0.5second and the number of cycles is 40. The stop time for transient analysis simulation is 20second.Table 1 shows the summarization of parameter that need to be considered in simulation process.

TABLE 1: specification to simulate ADC

Component	**parameter**	**Value**
CMOS	technology	0.18um
Vin (analog sine wave voltage)	Frequency	100MHz
	Amplitude	1.8V
	Offset voltage	0V
	phase	0°
Vdd	DC value	1.8V
$Vref$	DC value	1.8V
resistor	R value	5 ohm
CLK (pulse wave)	V (initial)	0V
	V(on)	1.8V
	Delay time	0.5s
	Rise and fall time	0.1s
	Period time	0.5s
	On time	0.25s

A. Comparator Stages Analysis

Comparator stage is simulated to generate thermometer code by DC sweep analysis simulation. The analog input voltage was swept from 0V to 1.8V. Figure 10 shows the input voltage and reference voltage generated by resistor ladder. Every resistor value at the resistor ladder is 5ohm.It generated15 reference voltage has range between 112.5mV to 1.675V. Each comparator will compare each reference voltage with sweep value of input voltage. All values of each reference voltage as in Table 2.

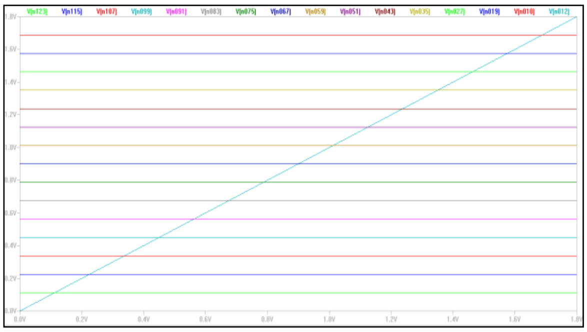

Fig.10: input voltage and reference voltage

The output comparator stage waveform is shown in Figure 11. The output waveforms are in the form of thermometer code. Comparator waveform will start at low state. The comparator output waveforms start changing from low to high when Vin is greater than $Vref$. Otherwise, the output waveforms stay at low state. The thermometer code of the comparison of Vin and $Vref$. at comparator stage was tabulated in table 2.

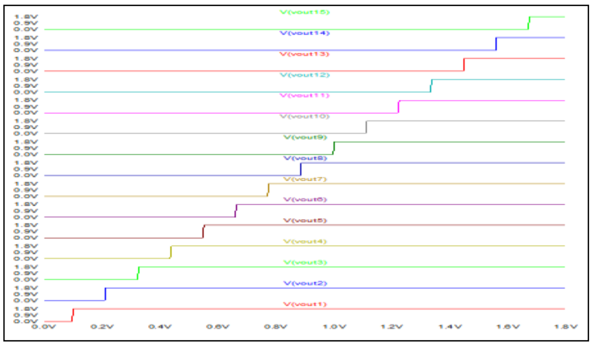

Fig.11: output comparator stage

B. 4-bit Pipeline Flash ADC Analysis

Proposed 4-bit pipeline flash ADC is simulated to generate the binary code waveform base on the conversion of gray code to binary code.

1) Dc sweep Analysis Simulation

DC sweep analysis simulation for pipeline flash ADC was same as the simulation for comparator stage. Figure 12 is the output binary code waveform that produced by converting thermometer code to binary code. This waveform was generated by DC sweep analysis simulation. The lowest significant bit (LSB) is the waveform of V(b0). The most significant bit (MSB) is the waveform of V(b3). Table 3 is the result of binary code produced by the simulation of 4 bits pipeline flash ADC.

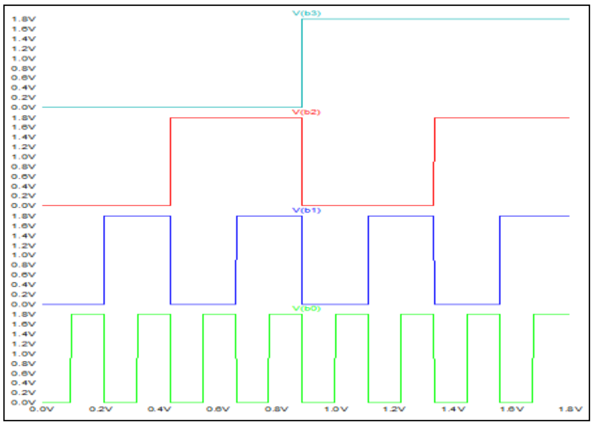

Fig.12: DC sweep analysis simulation waveform of Pipeline flash ADC

TABLE 2: Thermometer code

Reference voltage	Thermometer code													
	t15	t14	t13	t12	t11	t10	t9	t8	t7	t6	t5	t4	t3	t2	t1
0.00mV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
112.5mV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
225.0 mV	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
337.5 mV	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
450.0 mV	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
562.5 mV	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
675.0 mV	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
787.5 mV	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
900.0mV	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1.013V	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1.125V	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1.238V	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1.350V	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1.463V	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1.575V	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1.675V	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TABLE 3: Output binary code

VOLTAGE	OUTPUT BINARY CODE			
	B3	B2	B1	B0
0.0000V	0	0	0	0
0.9329V	0	0	0	1
0.2058V	0	0	1	0
0.3197V	0	0	1	1
0.4322V	0	1	0	0
0.5447V	0	1	0	1
0.6585V	0	1	1	0
0.7697V	0	1	1	1
0.8835V	1	0	0	0
0.9947V	1	0	0	1
1.1085V	1	0	1	0
1.2197V	1	0	1	1
1.3335V	1	1	0	0
1.4447V	1	1	0	1
1.5557V	1	1	1	0
1.6679V	1	1	1	1

C. *Meta-stability Analysis*

To analyze the meta-stability error, the circuit is simulated by DC sweep analysis simulation. First analysis is at the comparator stage and second analysis is the different of meta-stability between proposed pipeline flash ADC and the conventional flash ADC.

1) *Comparator Stage Meta-stability Analysis*

Meta-stability error is the error of comparator stage to achieved stable low state or high state. This error can be reduced by adding latch stage to comparator stage. The decreases of meta-stability error can be seen in Figure 13. The output comparator stage has low state voltage value 474.105mV. After adding latch circuit, the low output voltage value is decreases to 1.07537nV that is approximately 0V.

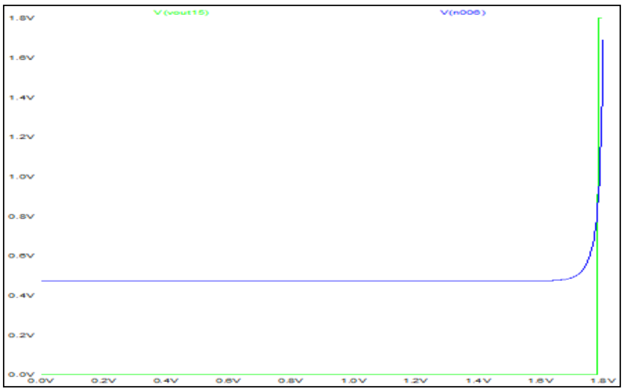

Fig.13: Meta-stability analysis

2) *Meta-stability Different Between Conventional and Pipeline Flash ADC*

Conventional flash ADC and proposed flash ADC is simulated to see the improvement of meta-stability error between those two architectures. The meta-stability error of those two architectures can be seen in the low state voltage and high state voltage of the output waveform. The low and high state output voltage was tabulated in Table 4 and 5.

TABLE 4: Conventional flash ADC

Output signal	Low state voltage	High state voltage
B3	504.56mV	1.8V
B2	4.3201nV	1.784V
B1	4.4981nV	1.8V
B0	2.1914nV	1.8V

Low and high state output voltage of conventional flash ADC is show in Table 4. The low state output voltage is not consistent. High state output voltage same for B3, B1 and B0 but different for B2. The meta-stability error occurred for the conventional flash ADC.

TABLE 5: Proposed pipeline flash ADC

Output signal	Low state voltage	High state voltage
B3	920.188pV	1.8V
B2	920.188pV	1.8V
B1	920.188pV	1.8V
B0	920.188pV	1.8V

For the proposed pipeline flash ADC, the low and high state output was tabulated in Table 5. We can see that the low state output voltage is consistent 920.188pV. The values also approximately equal to 0V. For high state, the value is equal to VDD, 1.8V and the value is consistent for all output signals.

D. *Effect of Load Capacitor Analysis*

Comparator circuit is simulate and analyze to show the function of comparator , the effect of load capacitor and effect of different value of load capacitor to the output of comparator[4]. Those analyses were done by transient analysis. The rise time and fall time will be effected by the load capacitor due to charging and discharging of the load capacitor. This will be explain in part 1 and 2.

1) *Effect of Load Capacitor.*

Figure 14 shows the output waveform of a comparator. The sine wave is the input analog voltage, red waveform is reference voltage and the green waveform is the output voltage. Based on this simulation, the output is high when the analog input voltage is greater than reference voltage. For the changes from high state to low state, the fall time is increases due the load capacitor discharging the charge. For low state, the voltage is 626.141mV. For 0.18um CMOS technology, approximately 0.6V is the VTH of each transistor. To on the transistor, input voltage must be higher than VTH. For the high state, the voltage is equal to VDD, 1.8V.

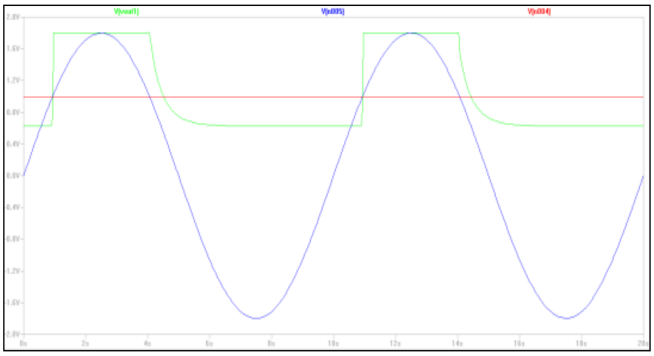

Fig.14: Output waveform of comparator

2) *Effect of Different Value of Load Capacitor*

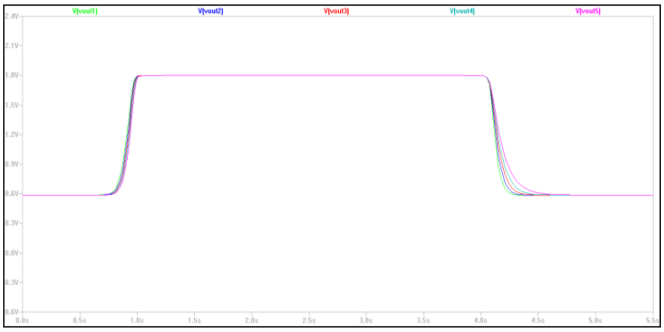

Fig.15: Different load capacitor value

Figure 15 show the simulation waveform of effect of different value of load capacitor. To analyze the effect, transient analysis simulation was done. The value of load capacitor was set. The value is 2pF, 6pF, 10pF, 16pF and 20pF and connected to the output terminal of comparator. The waveform shows that the small value capacitor produced fastest output waveform.

TABLE 6: Rise time and fall time

Load Capacitor(pF)	Output	Rise time(s)	Fall time(s)
2	Vout1	0.2436	0.2954
6	Vout2	0.2588	0.3044
10	Vout3	0.2588	0.3957
14	Vout4	0.2892	0.4718
20	Vout5	0.3196	0.6698

Table 6 show the load capacitor value and the output rise time and fall time. Small value of load capacitor has short time to charge and discharge but for the large value, it take more time to charging and discharging. Large value of load capacitor takes more time in rise time and fall time. For small value, its takes short time for rise time and fall time. But if the value is too small, the capacitor cannot filter the noise and distortion of the output voltage.

IV. CONCLUSION AND FUTURE RESEARCH

As a conclusion, this project somehow has achieved the objective where to design pipeline flash ADC using 0.18um CMOS technology and has successfully generates waveforms of flash ADC. The comparator stage generates the thermometer code based on the comparison of input voltage and reference voltage. In decoder stage, the thermometer code successfully converted to binary code based on waveform from simulation of pipeline flash ADC. For meta-stability error at flash ADC, it had been reduced by implemented the three latch staging to the thermometer code, gray code and binary code. The effect of load capacitor also had been analyzed. The small value of load capacitor gave short time of rise time and fall time of waveform due to charging and discharging process.

For future research, research can be improves in finding the power consumption pipeline circuit. Issues of power consumption were very critical to the designer to produces low power consumption flash ADC that can be use in portable devices. The different of length and width of transistor also can be as future research. This circuit should be design using Silvaco EDA software that is more advantages than LTSPICE software.

V. ACKNOWLEDGEMENT

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VI. REFERENCES

[1] E. Säll, M. Vesterbacka, and K. O. Andersson, “A STUDY OF DIGITAL DECODERS IN FLASH ANALOG-TO-DIGITAL CONVERTERS.”

[2] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, “A 4-Bit 5GS / s Flash A / D Converter in 0 . 18μm CMOS,” pp. 6138–6141, 2005.

[3] P. Heydari and R. Mohanavelu, “Design of ultrahigh-speed low-voltage CMOS CML buffers and latches,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 10, pp. 1081–1093, Oct. 2004.

[4] R. Mohd, "Design and Analysis of Low Power and High SpeedDynamic Latch Comparator in 0.18 µm CMOS Process," *International Journal of Information and Electronics Engineering*, vol. 2, no. 6, pp. 0–3, 2012.

[5] A. Detail, "Understanding Flash ADCs," pp. 1–7, 2001.

[6] S.- Linköping, "METASTABILITY DETERMINES THE NOISE IN FAST AND ACCURATE A / D CONVERTERS Jan-Erik Eklund and Christer Svensson," no. d.

[7] S. Shubhanand and A. G. Rao, "Design and Simulation of a High Speed CMOS Comparator," vol. 6, no. 1, pp. 75–80, 2013.

[8] C. Engineering, "Design and implementation of 4-bit flash ADC using folding technique in cadence tool," vol. 1, no. 4, pp. 238–241, 2012.

[9] W. Kester, "TUTORIAL MT-020," pp. 1–15.

[10] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0 . 18 m CMOS pipelined encoder for a 5 GS / s 4-bit flash analogue-to-digital converter Encodeur pipeline en technologie CMOS 0 , 18 m pour un convertisseur analogique- num erique flash 4 bits (5 GS / s)," vol. 30, no. 4, 2005.

[11] C. C. Lee, "Improving Accuracy and Energy Efficiency of Pipeline Analog to Digital Converters by," 2010.