CHARACTERIZATION OF MULTILEVEL INTERCONNECT CAPACITANCE FOR 0.35μm CMOS TECHNOLOGY

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ABSTRACT

This thesis presents a methodology for an interconnect capacitance characterization for 0.35µm CMOS technology with three-level metals. The purpose of this work is to generate a capacitance table for the new MIMOS 0.35µm CMOS process and compare with the previous back end process. The generated table is based on simulation results from Raphael field solver simulation tools. Parasitic capacitance database is created and capacitance rules file are generated for parasitic extraction using layout parameter extraction (LPE) tools, Calibre xRC. The methodology starts with plate capacitor measurement, followed by field solver simulation, and finally data verification. This methodology proves sufficiently accurate enough in technology library characterization for MIMOS 0.35µm CMOS process. The comparison of the process shows that the interconnect capacitance from the new process increased due to the smaller design rules implemented.

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CHAPTER 1

INTRODUCTION

In order to construct a Very Large Scale Integration (VLSI) circuits, it is necessary to fabricate many active devices on a single wafer. Initially, each of the devices must be isolated from the others, but later in the fabrication process specific devices must be interconnected in order to realize the desired circuit function [1]. Nowadays, in the VLSI circuits, the density of the circuit steadily increases as the transistor gate length downscaled with each new generation. Therefore, it will condense the circuit with millions of logic gates and several kilometers of wire. Interconnect is a process of wiring the devices on the wafer during the back-end process, as it becomes multilevel and more complex, it will greatly affect the performance of the circuits [2]. Thus, multilevel interconnect plays an important role in the VLSI circuits. Under this circumstances, accurate characterization and simulation of the multilevel interconnect are crucial to predict the performance of the circuit. For this research effort, the research work is implemented in Malaysian Institute of Microelectronic System (MIMOS) Berhad.

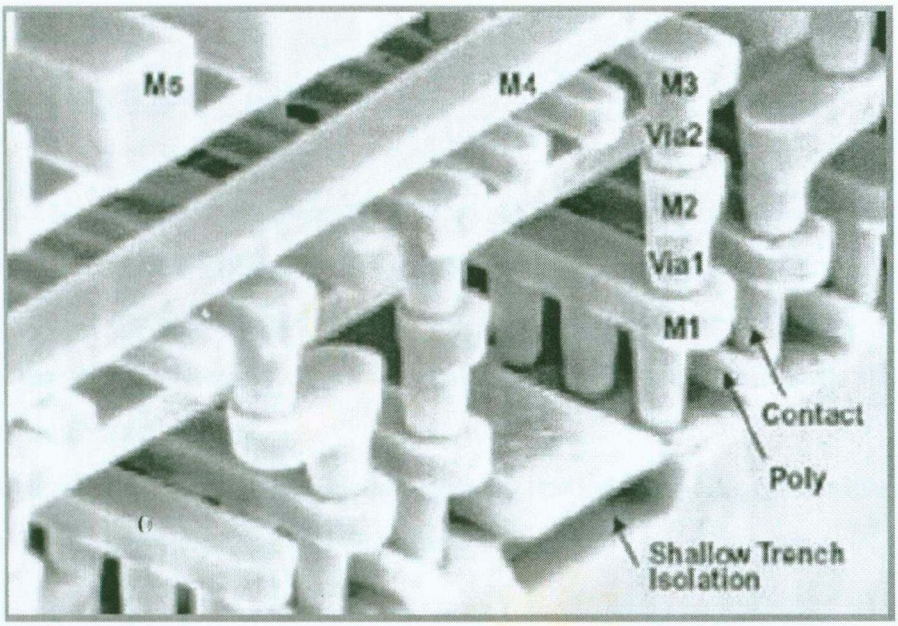

Figure 1.1: Cross section views of multilevel interconnect.