NMOS GATE LENGTH SCALING FOR 0.13μm USING SILVACO TCAD TOOLS

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ABSTRACT

This project is about down sizing the size of gate length of NMOS (n-channel MOSFET). The NMOS gate length is reduced from 0.18μm to 0.13μm. In order to reduce the size, the design process is based on the scaling factor rules. This process is done by using appropriate doping profile and oxide thickness according to the channel length in order to improve the device performance. This process is design for 0.13μm NMOS transistor with L_{gate} = 0.131μm and L_{eff} = 0.00765μm. The threshold voltage, V_T obtained was -0.1V and the drain current of 107μA/μm was obtained at V_D=V_G=2.5V. The design device is characterized for on-state and off-state performance. Electrical parameter extraction is done to develop this process which can be used in future circuit designs.

Silvaco TCAD Tools is used to simulate the process and analyze the electrical characteristics curve of the scaled NMOS. The study is about the results that will indicate the characteristics and effects of the reduction of gate length that brings to the impact of devices. The design process and design simulation is carried out using Silvaco's simulator tools Athena and Atlas.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

For the past 30 years, transistor scaling has been the primary factor for driving CMOS performance improvement. Approaching the fundamental limits of transistor scaling drives the industry and research community to actively search for alternative materials and new device architectures to boost the performance. A large part of the success of the CMOS transistor is due to the fact that it can be scaled to increasingly smaller size. As CMOS integrated circuit technology advances, the main focus of scaling the MOSFET is with respect to scaling the gate length. The advantages of scaling the gate length include an increase in the drain current, a decrease in gate area of the minimum sized transistor, both of which lead to improve circuit speed and thirdly an increase in the density of devices per chip.

Adjusting a fabrication process and the bias voltages to allow proper operation of reduced-sized devices is one of the constant pursuits of fabrication process engineering. The adjustment in achieving the small dimensions depends on the aspects of a given process should be optimized for applications.

In this design, a silicon N-type MOSFET gate length has been reduced from 0.18μm to 0.13μm through a combination of gate oxide and thickness and junction depth scaling. There are several approaches to device scaling. One of the approaches for maintaining the long-channel behaviour is to simply reduce all dimensions and voltages by scaling factor, κ. This approach is known as constant-field scaling. Besides that, the performance characteristic such as the curves of V_D, V_{GSs} V_T and I_D will be discussed to maintain the trend of performance improvement. In performing the fabrication simulation process, the TCAD