

**COMPARISON STUDY OF LIGHTLY DOPED DRAIN (LDD) AND  
DOUBLE DIFFUSED DRAIN (DDD) TO OVERCOME  
THE HOT CARRIER EFFECT ON 90nm CMOS DEVICE**

This thesis is presented in partial fulfillment for the award of the  
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**UNIVERSITI TEKNOLOGI MARA**

**SHAH ALAM, SELANGOR**

**MALAYSIA**



**MOHD HAFIZI BIN SURANI  
FACULTY OF ELECTRICAL ENGINEERING  
UNIVERSITI TEKNOLOGI MARA  
40450 SHAH ALAM  
SELANGOR DARUL EHSAN**

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## ABSTRACT

The aim of this project is to present the analysis and simulation of the comparison of Lightly Doped Drain (LDD) and Double Diffused Drain (DDD) to overcome Hot Carrier Effect on 90nm CMOS device. From the previous research, it showed that LDD method is better compared to DDD method to overcome hot carrier effect on 0.3um NMOS. This continuous project is to make a comparison between LDD and DDD method for 90nm CMOS device. Silvaco TCAD is a tools that being used to do data analysis such as substrate current ( $I_{sub}$ ), gate current ( $I_{gate}$ ), and gate voltage ( $V_g$ ). The comparison will be make in order to know which method is the best to overcome hot carrier effect on 90nm CMOS device.

The investigation is start with the LDD method to overcome the hot carrier effect. The LDD method is designing at Silvaco TCAD first and then analyzes the data needed. In LDD, two investigation are analyzed, that are specifically focusing on the concentration dose and implant energy, which on the  $n^-$  region for NMOS and  $p^-$  region for PMOS of the LDD structure. These investigations will produce the measurement of  $I_{sub}$  and  $I_{gate}$ , where directly related to the hot carrier effect. In DDD structure,  $I_{sub}$  and  $I_{gate}$  were measured only by varying the  $n^-$  and  $p^-$  concentration dose on NMOS and PMOS device respectively.

The data collected,  $I_{sub}$ ,  $I_{gate}$  and  $V_g$  will be analyzed. From the analysis, it can be conclude that both of the method can be use to overcome the hot carrier effect on 90nm CMOS device. As a result, LDD structure is better to the overcome hot carrier effect on 90nm NMOS device, which  $I_{sub}$  and  $I_{gate}$  were reduced to 48.12 % and 79.67 % respectively, while on 90nm PMOS device, DDD structure is better which  $I_{sub}$  and  $I_{gate}$  were reduce to 88.17 % and 65.83 % respectively.

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# CHAPTER I

## INTRODUCTION

### 1.0 Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a device used to amplify or switch electronic signals. The MOSFET includes a channel of n-type or p-type semiconductor material and is accordingly called NMOS and PMOS [1].

The complementary metal-oxide-semiconductor (CMOS) includes of both channel. CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Figure 1.1 shows the example of cross section area of two transistors in a CMOS device. CMOS is also sometimes referred to as complementary-symmetry metal-oxide-semiconductor (COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions [10].

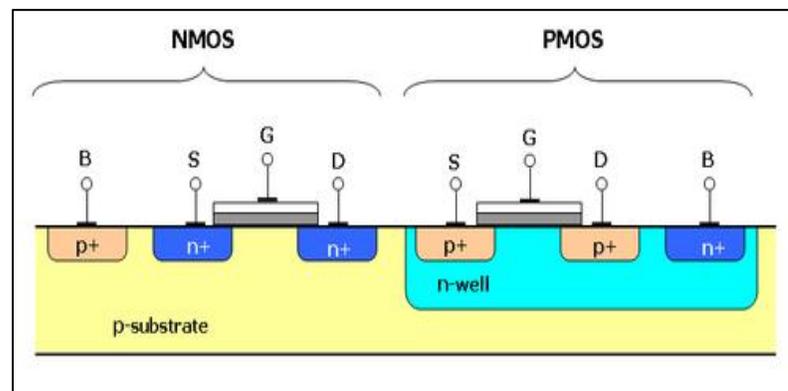


Figure 1.1: Cross section of two transistors in a CMOS device.