CIRCUIT PERFORMANCE ANALYSIS OF THREE- STAGE CMOS RING OSCILLATOR

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ABSTRACT

This report describes the simulation and measurement of the circuit performance analysis for a three-stage CMOS ring oscillator, to investigate the DC operating point. The MOSFET measurement is done using 372 Semiconductor Workbench to obtain the transfer curve and output curve for n-channel enhancement transistor ICs: IRLZ14, IRLD110, IRF730 and 2N7000. The three stages CMOS ring oscillator is simulated by PSPICE (Orcad Schematic Capture) and Tanner software.

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INTRODUCTION

1.1 INTRODUCTION

Nowadays, there are many modern and advanced software's being developed. One of the software is TANNER .From this software, it can simulate the three-stage CMOS ring oscillator using TANNER and SPICE. This project is intended to investigate the three-stage CMOS ring oscillator performance.

Recently, interest in ring oscillator has been growing Due to their versatile nature, ring oscillators have become a general purpose building block in many areas of integrated circuit design. Additionally, ring oscillators have both digital and analogue features which make them useful for data conversion tasks such as phase and pulse width modulation [1].

In this report, the circuit performance analysis of three-stage CMOS ring oscillator has been investigated. Figure 1 shows, a three-stage ring oscillator circuit where, the output node of the third inverter is connected to the input node of the first inverter.

The only DC operating point, at which the input and output voltages of all inverters which are equal to the logic threshold V_{th}, is inherently unstable in the sense that any disturbance in node voltage would make the circuit drift away from the DC operating point. In fact, a closed loop cascade connection of any odd number of inverter will display a stable behaviour [2]. The scope of this project has been limited to DC current and voltage performance.