SIMULATION OF DOUBLE STACK DIELECTRIC MOS CAPACITOR

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ABSTRACT

This paper reports the study about the relationship of Capacitance-Voltage (C-V) characteristics in MOS structure devices characterization. All these things are completely related with the experimental of double stack dielectric MOS capacitor in range of 35nm, 65nm and 95nm Silicon Oxide thickness neither calculated nor simulated capacitance. This project has been done by absolutely using TCAD Silvaco software. Athena and Atlas tools modules are most important simulators used that had been calibrated and manipulated in this experiment in order to fabricate the better MOS Capacitor with the fabricated industry standard sample from wafer Fabrication Lab. For this study, three operating modes under negative and positive bias such as the accumulation, depletion and inversion also have been put to prove the capacitance value obtained. Besides that, few parameters that have been considered and pay more attention which are the dielectric permittivity, thickness of dielectric, and MOS structure's area in this experiment to relate both of the calculated value and simulation output of the total capacitance from fabricated sample.

Keywords — Capacitance-Voltage Characteristics (C-V Curve); Metal–Oxide–Semiconductor (MOS) Capacitor; dielectric thickness, dielectric permittivity; area.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

The acronym MOS stands for metal–oxide–semiconductor. An MOS capacitor (Figure 1) is made of a semiconductor body or substrate, an insulator film, such as SiO2, and a metal electrode called a gate. The oxide film can be as thin as 1.5 nm. One nanometer is equal to 10 Å, or the size of a few oxide molecules.

MOS gate oxides thickness in logic, dynamic memory and non-volatile memory has been scaled to enhance the performance. Within the next few years gate dielectric thickness will be scaled to below 20 Å. This is approaching the fundamental limit for proper circuit operation. Supply voltage has not scaled proportionately according to the classical scaling theory. Degradation and breakdown is caused due to electrical stress. Therefore lifetime and reliability of such ultrathin dielectric films may be a show stopper in the evolution of the current technology.

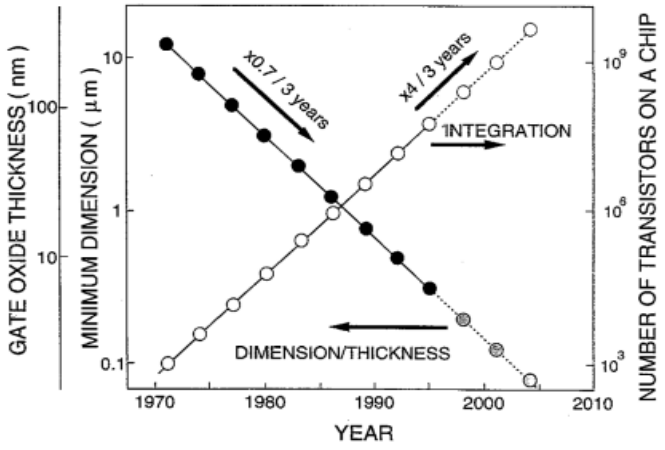

Figure 1.1: Thin Dielectrics for MOS Gate [13]