

**DESIGN OF LOW VOLTAGE LOW POWER AND FAST SETTLING  
OPERATIONAL TRANSCONDUCTANCE  
AMPLIFIER (OTA) USING 0.25 $\mu$ m TECHNOLOGY**

By

**MOHD RAZIFF BIN KUSNIN**  
Faculty of Electrical Engineering  
UNIVERSITI TEKNOLOGI MARA  
40450 Shah Alam, Selangor Darul Ehsan  
Malaysia

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This project is approved by:

Dr Azilah Saparon  
Project Supervisor

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## ABSTRACT

This thesis presents a fully differential operational transconductance amplifier (OTA) for very low voltage and fast settling application implemented in TSMC 0.25 $\mu$ m Complementary Metal Oxide Semiconductor (CMOS) process technology. The design employs full custom design approach in which the design starts with design specification determination followed by simulation for characterization purpose and validation. The layout design for the OTA is achieved along with the post layout simulation and layout verification. The layout is designed based on TSMC 0.25 $\mu$ m CMOS process technology and design rules. The performance analysis and the layout design of the OTA are done by using Mentor Graphics software.

The OTA consists of three main circuits; hybrid class A/AB OTA, common mode feedback (CMFB) and biasing circuit. The two stage OTA is proposed to satisfy the high dc gain requirement for high speed application. The performance analyses are compared to three different temperatures which are 70 degrees (worst-case), 25 degrees (typical-case) and 0 degree (best-case).

Simulation results show DC gain of 69.16dB, phase margin of 61.84 degrees, unity gain bandwidth of 173.69MHz, settling time of 11ns and power consumption of 5.95mW. By simulation, it is proved that the two stage class A/AB OTA produced a high gain, high speed and low power consumption.

# **TABLE OF CONTENTS**

|                                                                  | <b>PAGE</b> |
|------------------------------------------------------------------|-------------|
| DECLARATION                                                      | II          |
| ACKNOWLEDGEMENT                                                  | III         |
| ABSTRACT                                                         | IV          |
| TABLE OF CONTENTS                                                | V           |
| LIST OF FIGURES                                                  | IX          |
| LIST OF TABLES                                                   | XI          |
| ABBREVIATIONS                                                    | XII         |
| <br><b>CHAPTER 1</b>                                             |             |
| <b>INTRODUCTION</b>                                              |             |
| 1.1. Introduction                                                | 1           |
| 1.2. Project Specification                                       | 2           |
| 1.3. Objectives                                                  | 3           |
| 1.4. Scope of Work                                               | 3           |
| 1.5. Organization of the Thesis                                  | 4           |
| <br><b>CHAPTER 2</b>                                             |             |
| <b>LITERATURE REVIEW</b>                                         | 5           |
| 2.1. Operational Amplifier                                       | 5           |
| 2.1.1. Basic Operation                                           | 5           |
| 2.1.2. The Ideal Op-amp                                          | 6           |
| 2.2. Operational Transconductance Amplifier (OTA)                | 7           |
| 2.2.1. Principal Differences From Standard Operational Amplifier | 7           |
| 2.2.2. Basic Operation                                           | 8           |
| 2.2.3. Non-Ideal Characteristics                                 | 9           |
| 2.2.4. Subsequent Improvements                                   | 9           |

# CHAPTER 1

## INTRODUCTION

### 1.1 INTRODUCTION

An Operational Transconductance Amplifier (OTA) is used extensively in most analog and mixed signal mode devices such as sigma-delta [1], pipelined ADC [2] as well as switched capacitor [3]. The trend toward lower operating supply voltages and lower power consumption in mixed signal integrated circuit (IC) has three strong motivations:

- Portable equipment capable of operating with minimum number of battery cells to reduce volume and weight.
- Voltage limitations resulted from smaller feature sizes of modern IC technologies.
- Longer operating periods without battery recharging or replacement.

Design of high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. Two stage OTA is used to satisfy the high dc gain requirement for high speed application.

In OTA, settling time and dc gain are direct reflections of speed and accuracy. The criteria of speed and accuracy are determined by the settling behavior of the OTA. The fast settling mainly depends on the unity gain bandwidth (UGB) while high settling accuracy is due to high dc gain of the OTA. The realization of a CMOS operational amplifier that combines high dc gain with high unity gain bandwidth has been a difficult problem especially in low voltage circuits.

The high dc gain requirement leads to multistage designs or cascoding of transistors with long channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for single stage design with short channel devices biased