DESIGN OF SAR ADC CONTROL LOGIC USING VERILOG HDL

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In the name of Allah

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ABSTRACT

This paper presents the design of successive approximation register analog to digital converter (SAR ADC) control logic using Verilog Hardware Description Language (Verilog HDL) coding. This control logic design methodology is based on Xilinx ISE 8.1i Field Programmable Gate Array (FPGA) design flow from design entry until implementation process. The behavioral coding of SAR ADC control logic was written in Verilog HDL design entry by using Finite Sate Machine (FSM). It was synthesis to get the schematic, check syntax and we can be known the maximum of the clock that can be used. This 10-bit SAR ADC control logic was designed to operate at frequency of 33.3 MHz and the sampling rate is 3.33MSample/s. It was simulated by using Modelsim III 6.0d simulator. The SAR ADC control logic produces 10-bit at 33.3 MHz system clock and the power consumption is 18mW. For the implementation process level, place and route is used to generate the floor-planning of the SAR ADC control logic on FPGA. This project has been successfully and for the future, this project can be improved.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Hardware Description Language (HDL) is widely used in design flows for modern integrated circuits. There are two types of HDLs which are Verilog HDL and Very High-speed Integrated Circuit (VHIC) HDL or VHDL. Both languages are supported digital design implementation on Field Programmable Gate Array (FPGA). By using behaviour modelling, it can create a behavioural prototype of design, verify it functionality and can be synthesis and map the design into a selected physical technology by using a synthesis tools [7].

Analog-to-Digital Converter (ADC) provides the interface between the analog signals and the binary digital computational domain. Analog signals to be converted to digital can be originate from many types of transducers that convert physical phenomena, temperature, pressure, position, motion, sound, images, and so forth, to electrical signals. The digital signals that provided by ADC will be used in determination of control function [5, 6].

Successive-Approximation-Register (SAR) Analog-to-Digital Converters (ADCs) represent the majority of the ADC market for medium to high resolution ADCs. SAR ADCs provide up to 5Msps sampling rates with resolutions from 8 to 18 bits. Compared to the other ADC architecture, SAR ADC has several advantages. First, power consumption is very low because SAR ADC contains only one comparator. Second, the circuit is simple. The encoder in SAR ADC is inherent. There is no explicit substractor, sample and hold, bias circuitry, and resistor ladder required. Third, the comparator offset does not affect the linearity of the