SIMULATION OF DRAIN INDUCED BARRIER LOWERING (DIBL) IN METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

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ABSTRACT

This paper shows Simulation of Drain Induced Barrier Lowering (DIBL) in Metal Oxide Semiconductor Field Effect Transistor (MOSFET)". The research and study on this is investigated. Using software from SILVACO International, the simulation of the N-channel metal oxide semiconductor (NMOS) can be studied and the study is about DIBL due to short channel. SILVACO technology computer-aided design (TCAD) software is use to do the simulation and to obtain all the results needed. The virtually fabrication of NMOS is done using ATHENA module meanwhile for electrical characterizations of NMOS is done using ATLAS module. Using this software, the structure of MOSFET and I-V curve can be plotted through the TONYPLOT. In this study, the drain voltage, V_D and channel length, L act as the main roles in the results. Therefore, to see the role of drain voltage on DIBL, five different values of drain voltage, V_D which are 0.1 V, 0.2 V, 0.3 V, 0.4 V and 0.5 V are used. Meanwhile, for channel length, L, the values used are 0.20 µm, 0.30 µm, 0.40 µm and 0.50 µm. From drain current, I_D versus gate voltage, V_G (I-V) curve, the value of DIBL is obtained and analyzed to complete the analysis of DIBL. When the drain voltage, V_D increasing, the potential barrier in the channel decreasing which leads to DIBL. As the voltage drain, V_D is increasing, and the barrier height is decreasing while the drain current, I_D is increasing. This project do achieved the objectives of the project.

Keywords-DIBL, SILVACO TCAD, NMOS, TONYPLOT

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

MOSFET is a device which is used to amplify or to switch any kind of electronic signals. Nowadays, we can see that MOSFET technology is one of the most commonly used semiconductor technique, and had become one of the elements in the integrated circuit technology. The power consumptions in integrated circuits can be reduced as MOSFET's has good performance which enables the reduction. A MOSFET has two regions which are mainly named as the source and drain. Both regions are heavily doped and these are implanted in a substrate, which is doped the other way. The current will flow at the gap between the source and drain regions, which spans the substrate. A layer of insulating oxide is placed over this gap, which is well known as the channel. Moreover, on top of that is a gate contact and it is usually made of polysilicon. Figure 1.1 shows the MOSFET structure.

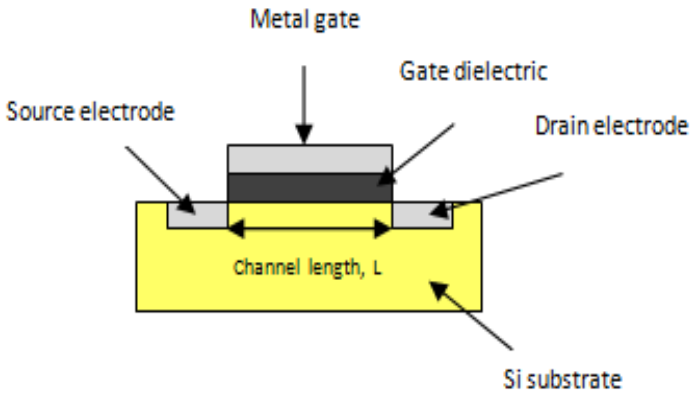

Figure 1.1: MOSFET Structure