DESIGN OF 8T SRAM AND SENSE AMPLIFIER USING 0.18µm CMOS TECHNOLOGY

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Abstract

In this work, an 8T SRAM operation and sense amplifier will be designed for 0.18µm CMOS technology. The operation of SRAM is to retain data content as long as electric power is supplied to the memory devices, and do not process for rewrite or refresh data. Also, the SRAM cell is preferred because of its low power operation. The performance of SRAM is measured by its static noise margin - a measure of the cell's stability to retain it's the data state. While for the sense amplifier, it is used to translate small differential voltage to a full logic signal that can be further used digital logic. The choice and design of a sense amplifier in this work will define the robustness of bit line sensing, so it will impact the read speed and power.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

SRAM is the Static Random Access Memories which retain their data content as long as electric power is supplied to the memory devices, and do not need any rewrite or refresh operation [1]. Static random access memory (SRAM) also is a type of volatile semiconductor memory to store binary logic '1' and '0' bits, and uses bi-stable latching circuitry made of transistors or MOSFETS to store each bit. Hence SRAM works without refreshing, where the data is lost when the memory is not electrically power.

The SRAM also is a faster, more reliable device, and can give access times as low as 10 nanoseconds. Its cycle time is much shorter because it does not need to pause between accesses. Due to its high cost, SRAM is often used only as a memory CACHE. A CACHE is used for temporary storage of instruction and data organized in blocks 32 bytes. Primary CACHE is the fastest form of storage because it is built in to the chip with a zero wait-state (delay) interface to the processor's execution unit, and it is limited in size. The CACHE is implemented using Static SRAM and traditionally is 16 KB in size.

In this project, the design of SRAM comprises of 8T and sense amplifier for CACHE specification of 2 KB N-way set associative. The CACHE holds the write-back data and writes it into main memory when that data line in CACHE is to be replaced. The design